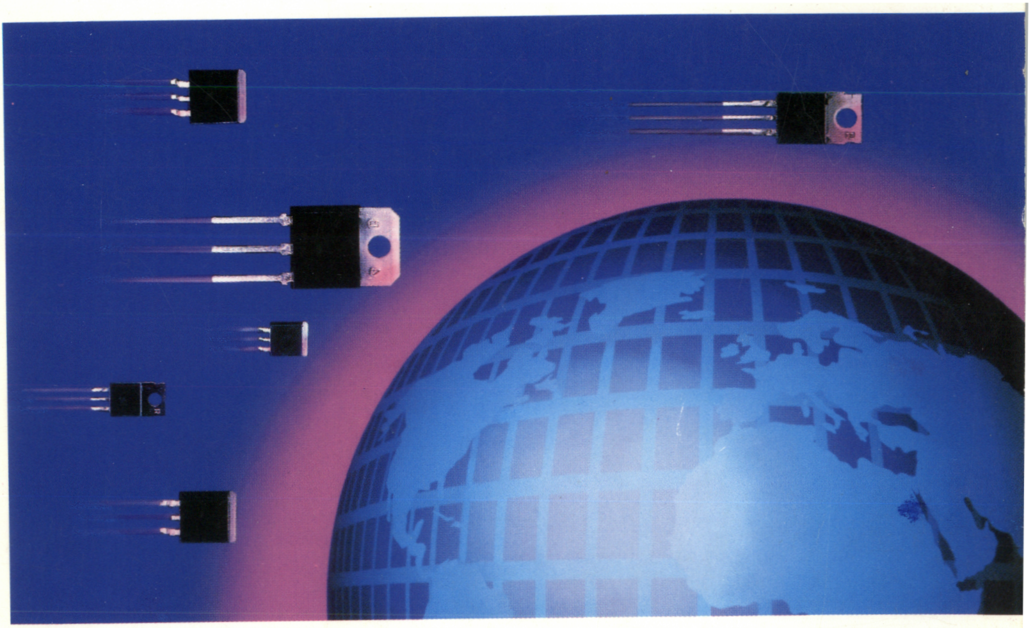
SIEMENS



SIPMOS-Halbleiter

Leistungstransistoren und Dioden

SIPMOS Semiconductors

Power Transistors and Diodes

Datenbuch 1993/94

Data Book 1993/94

Typenübersicht **Alphanumerische Typenliste** **Alphanumerische Bestellnummernliste**	**Selection Guide** **List of Types in Alphanumerical Order** **List of Ordering Codes in Alphanumerical Order**
Technische Angaben **Erläuterungen der Datenblattwerte** **Qualität und Zuverlässigkeit**	**Technical Information** **Explanation of Data Sheet Parameters** **Quality and Reliability**
Verarbeitungsrichtlinien **Gehäusemaßbilder**	**Mounting Instructions** **Package Outlines**
SIPMOS-Leistungstransistoren Datenblätter in alphanumerischer Reihenfolge	**SIPMOS Power Transistors** Data sheets in alphanumerical order
IGBT-Transistoren Datenblätter in alphanumerischer Reihenfolge	**IGBT Transistors** Data sheets in alphanumerical order
FRED-Dioden Datenblätter in alphanumerischer Reihenfolge	**FRED Diodes** Data sheets in alphanumerical order
Anschriften **Literaturhinweise**	**Semiconductors Group-Addresses** **Information on Literature**

Vorwort

Mit diesem neuen Datenbuch stellen wir Ihnen das aktuelle Produktspektrum der SIPMOS-Leistungstransistoren und Dioden vor. Das Buch beinhaltet alle derzeit bekannten Neuerungen, Verbesserungen und Weiterentwicklungen auf diesem Gebiet.

Mit der Herausgabe dieses Buches werden alle vorhergehenden Ausgaben ungültig.

Produktspektrum

- SIPMOS-Leistungstransistoren
- IGBT-Transistoren
- FRED-Dioden

Halbleiterauswahl

Um die Bauelementeauswahl zu erleichtern, haben wir Typenübersichten mit den wichtigsten technischen Eckdaten eingearbeitet. Die Datenblätter sind alphanumerisch sortiert und erleichtern so das Auffinden des gesuchten Halbleiters. Ein Vorspann gibt Auskunft über die wichtigsten Parameter und enthält Angaben zur Qualität und zur Verarbeitung bzw. Verpackung.

Kennzeichen in diesem Datenbuch

® Eingetragenes Warenzeichen

S Schwerpunkttypen:

Sofort lieferbar über "Semiconductor Distribution Center (SDC) Preis- und Lagerliste, Ausgabe April 1993".

Preface

This new edition of our Data Book presents our current range of SIPMOS power transistors and diodes, and includes all the innovations, improvements and further developments in this field.

With the publication of this edition, all previous editions of this Data Book cease to be valid.

Product Range

- SIPMOS power transistors
- IGBT transistors
- FRED diodes

Semiconductor Selection

A selection guide comprising the different types of semiconductors and their most important parameters will help you to find the right components. The individual data sheets are included in alphanumerical order and will further facilitate your type selection. An introduction provides you with information on the most important parameters, on quality as well as mounting and packaging.

Symbols in This Data Book

® Registered trademark

S Preferred type:

Immediately available from the Semiconductor Distribution Center (SDC), price and stock list as at April 1993.

SIEMENS

SIPMOS-Halbleiter

Leistungstransistoren und Dioden

Datenbuch 1993 / 94

SIPMOS Semiconductors

Power Transistors and Diodes

Data Book 1993 / 94

Herausgegeben von
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Mit den Angaben werden die Bauelemente spezifiziert, nicht Eigenschaften zugesichert.

Liefermöglichkeiten und technische Änderungen vorbehalten.

Fragen über Technik, Preise und Liefermöglichkeiten richten Sie bitte an den Ihnen nächstgelegenen Vertrieb Halbleiter in Deutschland oder an unsere Landesgesellschaften im Ausland.

Bauelemente können auf Grund technischer Erfordernisse Gefahrstoffe enthalten. Auskünfte darüber bitten wir unter Angabe des betreffenden Typs ebenfalls über den Vertrieb Halbleiter einzuholen.

Siemens AG ist ein Hersteller von CECC-qualifizierten Produkten.

Verpackung

Bitte benutzen Sie die Ihnen bekannten Verwerter. Wir helfen Ihnen auch weiter – wenden Sie sich an die Vertriebsstelle, die für Sie zuständig ist. Nach Rücksprache nehmen wir Verpackungsmaterial sortiert zurück. Die Transportkosten müssen Sie tragen.

Für Verpackungsmaterial, das unsortiert an uns zurückgeliefert wird oder für das wir keine Rücknahmepflicht haben, müssen wir Ihnen die anfallenden Kosten in Rechnung stellen.

Published by
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As far as patents or other rights of third parties are concerned, liability is only assumed for components per se, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact the Offices of Semiconductor Group in Germany or the Siemens Companies and Representatives worldwide (see address list).

Due to technical requirements components may contain dangerous substances. For information on the type in question please contact your nearest Siemens Office, Semiconductor Group.

Siemens AG is an approved CECC manufacturer.

Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.

For packing material, that is returned to us unsorted or which we are not obliged to accept we shall have to bill you all costs incurred.

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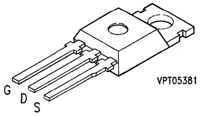
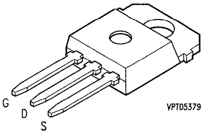
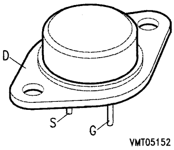
Alphanumerische Bestellnummernliste	**List of Ordering Codes in Alphanumerical Order**

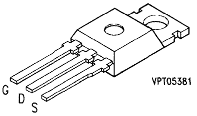
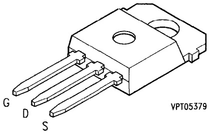
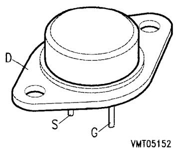
SIPMOS® Power Transistors

N Channel Power Transistors

		 **TO-220 AB**		 **TO-218 AA**		 **TO-204 AA**	
V_{DS} V	$R_{\mathrm{DS(on)}}$ Ω	**Type**	I_{D} **A**	**Type**	I_{D} **A**	**Type**	I_{D} **A**
50	18m	BUZ 100	58.0	BUZ 346	58.0	BUZ 16	48.0
50	28m	BUZ 12	42.0				
50	30m			BUZ 347	45.0	BUZ 15	45.0
50	35m	BUZ 12A	42.0				
50	40m	BUZ 11	30.0				
50	55m	BUZ 11A	26.0				
50	70m	BUZ 10	23.0				
50	0.1	BUZ 71	14.0				
50	0.12	BUZ 71A	13.0				
60	18m			BUZ 346S2	58.0	BUZ 16S2	48.0
60	40m	BUZ 11S2	30.0				
60	70m	BUZ 10S2	23.0				
60	0.10	BUZ 71S2	14.0				
60	0.15	BUZ 70	12.0				
100	35m			BUZ 344	46.0		
100	45m			BUZ 345	41.0		
100	55m	BUZ 22	24.0				
100	60m			BUZ 349	32.0	BUZ 24	32.0
100	85m	BUZ 21	21.0				
100	0.20	BUZ 72	10.0				
100	0.20	BUZ 20	13.5				
100	0.25	BUZ 72A	9.0				
200	70m			BUZ 341	33.0		
200	0.12			BUZ 350	22.0	BUZ 36	22.0
200	0.13	BUZ 30A	21.0				
200	0.20	BUZ 31	13.5				
200	0.60	BUZ 73A	5.8				
200	0.40	BUZ 73	7.0				
200	0.40	BUZ 32	9.5				

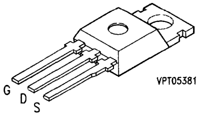
SIPMOS® Power Transistors

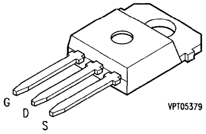
N Channel Power Transistors

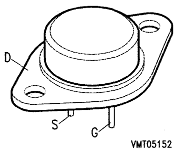
		 **TO-220 AB**		 **TO-218 AA**		 **TO-204 AA**	
V_{DS} V	$R_{DS(on)}$ Ω	**Type**	I_D **A**	**Type**	I_D **A**	**Type**	I_D **A**
250	0.24	BUZ 255	13.0				
400	0.30			BUZ 323	15.0		
400	0.35			BUZ 325	12.5		
400	0.40	BUZ 61	12.5			BUZ 64	11.5
400	0.50	BUZ 61A	11.0	BUZ 326	10.5		
400	1.00	BUZ 60	5.5				
400	1.80	BUZ 76	3.0				
400	2.50	BUZ 76A	2.6				
500	0.40			BUZ 338	13.5		
500	0.50			BUZ 339	11.5	BUZ 45B	10.0
500	0.60			BUZ 330	9.5	BUZ 45	9.6
500	0.80	BUZ 40B	8.0	BUZ 331	8.0	BUZ 45A	8.3
500	1.50	BUZ 41A	4.5				
500	2.00	BUZ 42	4.0				
500	3.00	BUZ 74	2.4				
500	4.00	BUZ 74A	2.1				
600	0.50			BUZ 334	12.0		
600	0.80	BUZ 91	8.0	BUZ 332	8.5		
600	0.90	BUZ 91A	8.0	BUZ 332A	8.0	BUZ 94	7.8
600	1.60	BUZ 90	4.5				
600	2.00	BUZ 90A	4.0				
600	2.50	BUZ 93	3.6				
600	3.00	BUZ 92	3.2				
600	3.50	BUZ 77B	2.9				
600	4.00	BUZ 77A	2.1				

SIPMOS® Power Transistors

N Channel Power Transistors



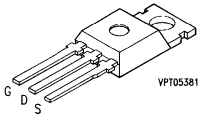




		TO-220 AB		TO-218 AA		TO-204 AA	
V_{DS} V	$R_{DS(on)}$ Ω	Type	I_D A	Type	I_D A	Type	I_D A
800	1.00			BUZ 305	7.5		
800	1.50			BUZ 355	6.0	BUZ 84A	6.0
800	2.00			BUZ 356	5.0	BUZ 84	5.3
800	2.50	BUZ 81	4.0				
800	3.00	BUZ 80A	3.0	BUZ 307	3.0		
800	4.00	BUZ 80	2.6	BUZ 308	2.6		
800	8.00	BUZ 78	1.5				
1000	1.50			BUZ 312	6.0		
1000	2.00			BUZ 357	5.0	BUZ 54	5.1
1000	2.60			BUZ 358	4.5	BUZ 54A	4.5
1000	4.00	BUZ 51	3.4				
1000	5.00	BUZ 50A	2.5	BUZ 310	2.5	BUZ 53A	2.6
1000	6.00	BUZ 50C	2.3	BUZ 311	2.3		
1000	8.00	BUZ 50B	2.0				

SIPMOS® Power Transistors

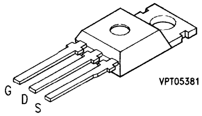
N Channel Logic Level Transistors



TO-220 AB

V_{DS} V	$R_{DS(on)}$ Ω	Type	I_D A
50	35m	BUZ 12AL	42.0
50	55m	BUZ 11AL	26.0
50	70m	BUZ 10L	23.0
50	0.1	BUZ 71L	14.0
50	0.12	BUZ 71AL	13.0
60	0.15	BUZ 70L	12.0
100	85m	BUZ 21L	21.0
100	0.20	BUZ 72L	10.0
100	0.25	BUZ 72AL	9.0
200	0.20	BUZ 31L	13.5
200	0.40	BUZ 73L	7.0
200	0.60	BUZ 73AL	5.8

P Channel Power Transistors



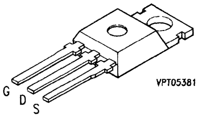
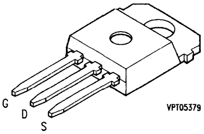
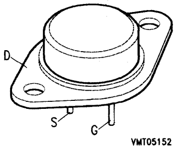
TO-220 AB

V_{DS} V	$R_{DS(on)}$ Ω	Type	I_D A
– 50	0.15	BUZ 271	– 22.0
– 50	0.30	BUZ 171	– 8.0
– 100	0.60	BUZ 172	– 5.0
– 100	0.30	BUZ 272	– 15.0
– 200	1.50	BUZ 173	– 3.0

SIPMOS® Power Transistors

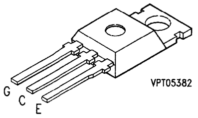
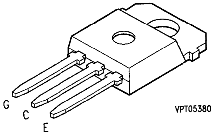
FREDFET

N Channel with High-Speed Reverse
Diode

		 **TO-220 AB**		 **TO-218 AA**		 **TO-204 AA**	
V_{DS} **V**	$R_{DS(on)}$ Ω	**Type**	I_D **A**	**Type**	I_D **A**	**Type**	I_D **A**
400	0.40			BUZ 382	12.5		
400	1.00	BUZ 205	6.0				
500	0.60			BUZ 384	10.5	BUZ 210	10.5
500	0.80			BUZ 385	9.0	BUZ 211	9.0
500	1.50	BUZ 215	5.1				
1000	2.00			BUZ 380	5.5		

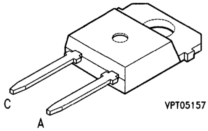
IGBT Transistors

Insulated Gate Bipolar Transistors

	 **TO-220 AB**		 **TO-218 AA**	
V_{CE} **V**	**Type**	I_C **A**	**Type**	I_C **A**
1000	BUP 202	12.0	BUP 302	12.0
1000	BUP 203	21.0	BUP 303	21.0
1000			BUP 304	35.0
1200	BUP 200	5.0	BUP 300	5.0
1200			BUP 307	35.0

FRED Diodes

High-Speed Diodes

		 **TO-218 AD**	
V_{RRM} **V**	t_{rr} **ns**	**Type**	I_{FRMS} **A**
1000	55	BYP 100	5.0
1000	80	BYP 101	25.0
1000	130	BYP 102	50.0
1000	140	BYP 103	75.0
1200	100	BYP 301	20.0
1200	140	BYP 302	40.0
1200	150	BYP 303	60.0

	Typ Type	Bestellnummer Ordering Code	Seite Page
S	BUP 200	C67078-A4400-A2	729
S	BUP 202	C67078-A4401-A2	735
S	BUP 203	C67078-A4402-A2	741
S	BUP 300	C67078-A4203-A2	729
S	BUP 302	C67078-A4205-A2	735
S	BUP 303	C67078-A4202-A2	741
S	BUP 304	C67078-A4200-A2	747
S	BUP 307	C67078-A4201-A2	747
S	BUZ 10	C67078-S1300-A2	137
S	BUZ 10 L	C67078-S1329-A2	144
S	BUZ 10 S2	C67078-S1300-A7	137
S	BUZ 11	C67078-S1301-A2	151
S	BUZ 11 A	C67078-S1301-A3	151
S	BUZ 11 AL	C67078-S1330-A3	159
S	BUZ 11 S2	C67078-S1301-A5	151
S	BUZ 12	C67078-S1331-A2	166
S	BUZ 12 A	C67078-S1331-A3	166
S	BUZ 12 AL	C67078-S1332-A3	174
S	BUZ 15	C67078-S1001-A2	181
S	BUZ 16	C67078-S1020-A2	188
S	BUZ 16 S2	C67078-S1020-A3	188
S	BUZ 20	C67078-S1302-A2	196
S	BUZ 21	C67078-S1308-A2	203
	BUZ 21 L	C67078-S1338-A2	210
S	BUZ 22	C67078-S1333-A2	217
S	BUZ 24	C67078-S1003-A2	224
S	BUZ 30 A	C67078-S1303-A3	231
S	BUZ 31	C67078-S1304-A2	238
S	BUZ 32	C67078-S1310-A2	245
S	BUZ 36	C67078-S1018-A2	252
S	BUZ 40 B	C67078-S1305-A4	259
S	BUZ 41 A	C67078-S1306-A3	266
S	BUZ 42	C67078-S1311-A2	273
S	BUZ 45	C67078-A1008-A8	279
S	BUZ 45 A	C67078-A1008-A9	279
S	BUZ 45 B	C67078-A1008-A10	279
S	BUZ 50 A	C67078-A1307-A3	288
S	BUZ 50 B	C67078-A1307-A4	288
S	BUZ 50 C	C67078-A1307-A5	288
S	BUZ 51	C67078-S1344-A2	297
S	BUZ 53 A	C67078-S1009-A3	304
S	BUZ 54	C67078-S1010-A2	310
S	BUZ 54 A	C67078-S1010-A3	310
S	BUZ 60	C67078-S1312-A2	318
S	BUZ 61	C67078-S1341-A2	325
S	BUZ 61 A	C67078-S1341-A3	325
S	BUZ 64	C67078-S1017-A2	333
S	BUZ 70	C67078-S1334-A2	340
S	BUZ 70 L	C67078-S1325-A2	347
S	BUZ 71	C67078-S1316-A2	354
S	BUZ 71 A	C67078-S1316-A3	354
S	BUZ 71 AL	C67078-S1326-A3	362
S	BUZ 71 L	C67078-S1326-A2	362
S	BUZ 71 S2	C67078-S1316-A9	354
S	BUZ 72	C67078-S1313-A2	370
S	BUZ 72 A	C67078-S1313-A3	370
S	BUZ 72 AL	C67078-S1327-A3	378
S	BUZ 72 L	C67078-S1327-A2	378

Typ Type	Bestellnummer Ordering Code	Seite Page
S BUZ 73	C67078-S1317-A2	386
S BUZ 73 A	C67078-S1317-A3	386
S BUZ 73 AL	C67078-S1328-A3	394
S BUZ 73 L	C67078-S1328-A2	394
S BUZ 74	C67078-S1314-A2	402
S BUZ 74 A	C67078-S1314-A3	402
S BUZ 76	C67078-S1315-A2	410
S BUZ 76 A	C67078-S1315-A3	410
S BUZ 77	C67078-S1320-A3	418
S BUZ 77 B	C67078-S1320-A5	418
S BUZ 78	C67078-S1318-A2	426
S BUZ 80	C67078-A1309-A2	433
S BUZ 80 A	C67078-A1309-A3	433
S BUZ 81	C67078-S1345-A2	441
S BUZ 84	C67078-A1013-A2	448
S BUZ 84 A	C67078-A1013-A3	448
S BUZ 90	C67078-S1321-A2	456
S BUZ 90 A	C67078-S1321-A3	456
S BUZ 91	C67078-S1342-A2	464
S BUZ 91 A	C67078-S1342-A3	464
S BUZ 92	C67078-S1343-A2	472
S BUZ 93	C67078-S1346-A2	472
S BUZ 94	C67078-A1019-A2	480
BUZ 100	C67078-S1348-A2	487
S BUZ 171	C67078-S1450-A2	490
S BUZ 172	C67078-A1451-A2	496
S BUZ 173	C67078-A1452-A2	502
S BUZ 205	C67078-A1401-A2	508
S BUZ 210	C67078-A1102-A2	514
BUZ 211	C67078-A1100-A2	514
S BUZ 215	C67078-A1400-A2	522
S BUZ 255	C67078-S1406-A2	528
S BUZ 271	C67078-S1453-A2	535
S BUZ 272	C67078-S1454-A2	541
S BUZ 305	C67078-S3134-A2	548
S BUZ 307	C67078-A3100-A2	551
S BUZ 308	C67078-A3109-A2	551
S BUZ 310	C67078-A3101-A2	559
S BUZ 311	C67078-A3102-A2	559
S BUZ 312	C67078-S3129-A2	567
S BUZ 323	C67078-S3127-A2	574
S BUZ 325	C67078-S3118-A2	581
S BUZ 326	C67078-S3112-A2	588
S BUZ 330	C67078-S3105-A2	595
S BUZ 331	C67078-S3114-A2	602
S BUZ 332	C67078-S3123-A2	609
S BUZ 332 A	C67078-S3123-A4	609
S BUZ 334	C67078-S3130-A2	617
S BUZ 338	C67078-S3126-A2	624
BUZ 339	C67078-S3133-A2	631
S BUZ 341	C67078-S3128-A2	638
S BUZ 344	C67078-S3132-A2	645
S BUZ 345	C67078-S3121-A2	652
S BUZ 346	C67078-S3120-A2	659
BUZ 346 S2	C67078-S3120-A4	659
S BUZ 347	C67078-S3115-A2	667
S BUZ 349	C67078-S3113-A2	674
S BUZ 350	C67078-S3117-A2	681

Typ Type	Bestellnummer Ordering Code	Seite Page
S BUZ 355	C67078-A3107-A2	688
S BUZ 356	C67078-A3108-A2	688
S BUZ 357	C67078-S3110-A2	696
S BUZ 358	C67078-S3111-A2	696
BUZ 380	C67078-A3205-A2	704
S BUZ 382	C67078-A3207-A2	711
S BUZ 384	C67078-A3209-A2	718
S BUZ 385	C67078-A3210-A2	718

Typ Type	Bestellnummer Ordering Code	Seite Page
S BYP 100	C67047-A2254-A2	755
S BYP 101	C67047-A2072-A2	757
S BYP 102	C67047-A2071-A2	760
S BYP 103	C67047-A2066-A2	763
S BYP 300	C67047-A2250-A2	766
S BYP 301	C67047-A2251-A2	768
S BYP 302	C67047-A2252-A2	771
S BYP 303	C67047-A2253-A2	774

	Bestellnummer Ordering Code	Typ Type	Seite Page
S	C67047-A2066-A2	BYP 103	763
S	C67047-A2071-A2	BYP 102	760
S	C67047-A2072-A2	BYP 101	757
S	C67047-A2250-A2	BYP 300	766
S	C67047-A2251-A2	BYP 301	768
S	C67047-A2252-A2	BYP 302	771
S	C67047-A2253-A2	BYP 303	774
S	C67047-A2254-A2	BYP 100	755
S	C67078-A1008-A8	BUZ 45	279
S	C67078-A1008-A9	BUZ 45 A	279
S	C67078-A1008-A10	BUZ 45 B	279
S	C67078-A1013-A2	BUZ 84	448
S	C67078-A1013-A3	BUZ 84 A	448
S	C67078-A1019-A2	BUZ 94	480
S	C67078-A1100-A2	BUZ 211	514
S	C67078-A1102-A2	BUZ 210	514
S	C67078-A1307-A3	BUZ 50 A	288
S	C67078-A1307-A4	BUZ 50 B	288
S	C67078-A1307-A5	BUZ 50 C	288
S	C67078-A1309-A2	BUZ 80	433
S	C67078-A1309-A3	BUZ 80 A	433
S	C67078-A1400-A2	BUZ 215	522
S	C67078-A1401-A2	BUZ 205	508
S	C67078-A1451-A2	BUZ 172	496
S	C67078-A1452-A2	BUZ 173	502
S	C67078-A3100-A2	BUZ 307	551
S	C67078-A3101-A2	BUZ 310	559
S	C67078-A3102-A2	BUZ 311	559
S	C67078-A3107-A2	BUZ 355	688

	Bestellnummer Ordering Code	Typ Type	Seite Page
S	C67078-A3108-A2	BUZ 356	688
S	C67078-A3109-A2	BUZ 308	551
S	C67078-A3205-A2	BUZ 380	704
S	C67078-A3207-A2	BUZ 382	711
S	C67078-A3209-A2	BUZ 384	718
S	C67078-A3210-A2	BUZ 385	718
S	C67078-A4200-A2	BUP 304	747
S	C67078-A4201-A2	BUP 307	747
S	C67078-A4202-A2	BUP 303	741
S	C67078-A4203-A2	BUP 300	729
S	C67078-A4205-A2	BUP 302	735
S	C67078-A4400-A2	BUP 200	729
S	C67078-A4401-A2	BUP 202	735
S	C67078-A4402-A2	BUP 203	741
S	C67078-S1001-A2	BUZ 15	181
S	C67078-S1003-A2	BUZ 24	224
S	C67078-S1009-A3	BUZ 53 A	304
S	C67078-S1010-A2	BUZ 54	310
S	C67078-S1010-A3	BUZ 54 A	310
S	C67078-S1017-A2	BUZ 64	333
S	C67078-S1018-A2	BUZ 36	252
S	C67078-S1020-A2	BUZ 16	188
S	C67078-S1020-A3	BUZ 16 S2	188
S	C67078-S1300-A2	BUZ 10	137
S	C67078-S1300-A7	BUZ 10 S2	137
S	C67078-S1301-A2	BUZ 11	151
S	C67078-S1301-A3	BUZ 11 A	151
S	C67078-S1301-A5	BUZ 11 S2	151
S	C67078-S1302-A2	BUZ 20	196

Bestellnummer Ordering Code	Typ Type	Seite Page
S C67078-S1303-A3	BUZ 30 A	231
S C67078-S1304-A2	BUZ 31	238
S C67078-S1305-A4	BUZ 40 B	259
S C67078-S1306-A3	BUZ 41 A	266
S C67078-S1308-A2	BUZ 21	203
S C67078-S1310-A2	BUZ 32	245
S C67078-S1311-A2	BUZ 42	273
S C67078-S1312-A2	BUZ 60	318
S C67078-S1313-A2	BUZ 72	370
S C67078-S1313-A3	BUZ 72 A	370
S C67078-S1314-A2	BUZ 74	402
S C67078-S1314-A3	BUZ 74 A	402
S C67078-S1315-A2	BUZ 76	410
S C67078-S1315-A3	BUZ 76 A	410
S C67078-S1316-A2	BUZ 71	354
S C67078-S1316-A3	BUZ 71 A	354
S C67078-S1316-A9	BUZ 71 S2	354
S C67078-S1317-A2	BUZ 73	386
S C67078-S1317-A3	BUZ 73 A	386
S C67078-S1318-A2	BUZ 78	426
S C67078-S1320-A3	BUZ 77	418
S C67078-S1320-A5	BUZ 77 B	418
S C67078-S1321-A2	BUZ 90	456
S C67078-S1321-A3	BUZ 90 A	456
S C67078-S1325-A2	BUZ 70 L	347
S C67078-S1326-A2	BUZ 71 L	362
S C67078-S1326-A3	BUZ 71 AL	362
S C67078-S1327-A2	BUZ 72 L	378
S C67078-S1327-A3	BUZ 72 AL	378

Bestellnummer Ordering Code	Typ Type	Seite Page
S C67078-S1328-A2	BUZ 73 L	394
S C67078-S1328-A3	BUZ 73 AL	394
S C67078-S1329-A2	BUZ 10 L	144
S C67078-S1330-A3	BUZ 11 AL	159
S C67078-S1331-A2	BUZ 12	166
S C67078-S1331-A3	BUZ 12 A	166
S C67078-S1332-A3	BUZ 12 AL	174
S C67078-S1333-A2	BUZ 22	217
S C67078-S1334-A2	BUZ 70	340
S C67078-S1338-A2	BUZ 21 L	210
S C67078-S1341-A2	BUZ 61	325
S C67078-S1341-A3	BUZ 61 A	325
S C67078-S1342-A2	BUZ 91	464
S C67078-S1342-A3	BUZ 91 A	464
S C67078-S1343-A2	BUZ 92	472
S C67078-S1344-A2	BUZ 51	297
S C67078-S1345-A2	BUZ 81	441
S C67078-S1346-A2	BUZ 93	472
S C67078-S1348-A2	BUZ 100	487
S C67078-S1406-A2	BUZ 255	528
S C67078-S1450-A2	BUZ 171	490
S C67078-S1453-A2	BUZ 271	535
S C67078-S1454-A2	BUZ 272	541
S C67078-S3105-A2	BUZ 330	595
S C67078-S3110-A2	BUZ 357	696
S C67078-S3111-A2	BUZ 358	696
S C67078-S3112-A2	BUZ 326	588
S C67078-S3113-A2	BUZ 349	674
S C67078-S3114-A2	BUZ 331	602

Bestellnummer Ordering Code	Typ Type	Seite Page
S C67078-S3115-A2	BUZ 347	667
S C67078-S3117-A2	BUZ 350	681
S C67078-S3118-A2	BUZ 325	581
S C67078-S3120-A2	BUZ 346	659
C67078-S3120-A4	BUZ 346 S2	659
S C67078-S3121-A2	BUZ 345	652
S C67078-S3123-A2	BUZ 332	609
S C67078-S3123-A4	BUZ 332 A	609

Bestellnummer Ordering Code	Typ Type	Seite Page
S C67078-S3126-A2	BUZ 338	624
S C67078-S3127-A2	BUZ 323	574
S C67078-S3128-A2	BUZ 341	638
S C67078-S3129-A2	BUZ 312	567
S C67078-S3130-A2	BUZ 334	617
C67078-S3132-A2	BUZ 344	645
S C67078-S3133-A2	BUZ 339	631
S C67078-S3134-A2	BUZ 305	548

Technische Angaben
Erläuterungen der Datenblattwerte
Qualität und Zuverlässigkeit

Technical Information
Explanation of Data Sheet Parameters
Quality and Reliability

1 Übersicht

1.1 SIPMOS-Leistungstransistoren

Leistungstransistoren im Bereich 50 V ... 1000 V und 10 mΩ ... 8 Ω

Produktpalette

- N-Kanal Anreicherungstypen
- P-Kanal Anreicherungstypen
- FREDFET
- Logik Level

1 Overview

1.1 SIPMOS Power Transistors

Power transistors in the 50 V to 1000 V and 10 mΩ to 8 Ω range

Product range

- N-channel enhancement types
- P-channel enhancement types
- FREDFET
- Logic level

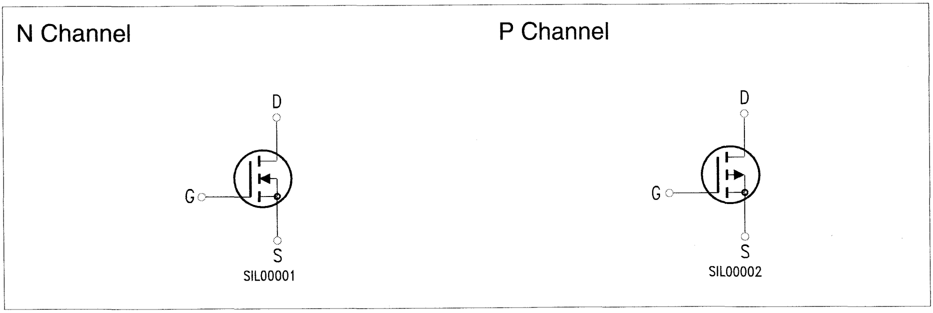


Bild 1
Schaltsymbol

Figure 1
Graphical symbol

Allgemeines

SIPMOS-Transistoren sind selbstsperrende Feldeffekttransistoren mit den Anschlüssen: G ≙ Gate, S ≙ Source und D ≙ Drain. Durch Anlegen einer Spannung zwischen G und S wird der Kanalwiderstand zwischen D und S gesteuert. Wie bei bipolaren Transistoren unterscheidet man N- und P-Kanal-Transistoren. N-Kanal-Typen werden mit einer positiven Gate-Source-Spannung gesteuert und sperren positive Drain-Source-Spannun-

General Remarks

SIPMOS transistors are self-blocking field-effect transistors with G ≙ GATE, S ≙ SOURCE and D ≙ DRAIN connections. The channel resistance between D and S is controlled by applying a voltage across the G and S. As with bipolar transistors, a distinction is made between N- and P-channel transistors. N-channel types are controlled with a positive gate-source voltage and block positive drain-source voltages. In the case of P-channel gen. Bei P-Kanal-Typen sind die Spannungspolaritäten umgekehrt. SIPMOS-Transistoren besitzen ein unsymmetrisches Sperrverhalten, d.h. sie sind nur in der Drain-Source-Richtung sperrfähig. In der Gegenrichtung ist die Inversdiode leitend.

Das Typenspektrum bei N-Kanal ist gegenüber den P-Kanal-Transistoren umfangreicher. Die Ursache liegt in der physikalisch bedingt besseren Leitfähigkeit des N-Kanals. Bei MOS-Transistoren gleicher Sperrspannung und Chipfläche ist der Drain-Source-On-Widerstand $R_{DS(on)}$ eines P-Kanal-Transistors mehr als doppelt so hoch als der eines N-Kanals.

Merkmale

- Spannungsgesteuert
- Hohe Schaltleistung
- Einfaches Parallelschalten
- Kurze Schaltzeiten
- Keine Speicherzeit
- Hohe Grenzfrequenz
- Hohe Strom- und Spannungsfestigkeit
- Überlastsicherheit
  (kein "Second Breakdown")
- Linearer Kennlinienverlauf
- Durchbruchspannungsfest
  (avalanchefest)

types the voltage polarities are the reverse. SIPMOS transistors have an asymmetrical reverse behavior, i.e. they can be rendered reverse-biased only in the drain-source direction. The inverse diode is forward-biased in the opposite direction.

The range of N-channel types is more extensive than that of P-channel transistors. This is due to the better conductivity of the N-channel for physical reasons. In the case of MOS transistors having the same reverse voltage and chip area the drain-source ON resistance $R_{DS(on)}$ of a P-channel resistor is more than twice as high as that of an N-channel.

Features

- Voltage-controlled
- High making and breaking capacity
- Simple parallel connection
- Short switching times
- No carrier storage time
- High cutoff frequency
- High current-carrying capacity and dielectric strength
- Overload protection
  (no second breakdown)
- Linear characteristic
- Avalanche-rated
  (avalanche-resistant)

Einsatzmöglichkeiten (Auswahl)

- Schaltnetzteile
- Gleichspannungswandler
- Wechselrichter
- Motorsteuerungen
- Unterbrechungsfreie Stromversorgungen
- Näherungsschalter
- Ultraschallgeneratoren
- Flimmerfreie Monitore
- NF-Verstärker
- Frequenzumrichter für Drehstromantriebe
- Getaktete Stromversorgungen für Schweißgeräte

Literaturhinweise

Leistungshalbleiter SIPMOS und IGBT Bestell-Nr. B152-B6417-X-X-7400

Anwendungsbeispiele für SIPMOS-Transistoren Bestell-Nr. B152-H6428

Applications (Selected)

- Switched-mode power supply units
- DC converters
- Inverters
- Motor control units
- Uninterruptible power supplies
- Proximity switches
- Ultrasonic generators
- Flicker-free monitors
- AF amplifiers
- Static frequency changers for three-phase drives
- Clocked power supplies for welding equipment

References

Power Semiconductors SIPMOS und IGBT Ordering Code B152-B6417-X-X-7400

Application Notes for SIPMOS Power Transistors Ordering Code B152-H6428-X-X-7600

1.2 IGBT-Transistoren

Hochsperrende spannungsgesteuerte Bipolar-Transistoren

Produktpalette

- IGBT-Transistoren im Bereich 1000 V ... 1200 V und 5 A ... 35 A

1.2 IGBT Transistors

Insulated **G**ate **B**ipolar **T**ransistors

Product range

- IGBT transistors in the 1000 V to 1200 V and 5 A to 35 A range

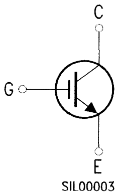


Bild 2
Schaltsymbol

Figure 2
Graphical symbol

Merkmale

- Spannungsgesteuerter MOS-Eingang
- Niedrige Durchlaßspannung
- Hohe Schaltgeschwindigkeit > 20 kHz
- Kleiner Tailstrom
- Geringe Temperaturabhängigkeit
- Kurzschlußfest
- Latch-up-frei
- Durchbruchfest

Features

- Voltage-controlled MOS input
- Low forward voltage
- High switching speed
- Low tail current
- Low temperature dependence
- Short-circuit-proof
- No latch up
- Avalanche-rated

Einsatzmöglichkeiten (Auswahl)

- Frequenzumrichter für Drehstromantriebe
- Getaktete Stromversorgungen für Schweißgeräte
- Unterbrechungsfreie Stromversorgungen
- Schaltnetzteile größerer Leistung
- Kfz-Zündungen

1.3 FRED-Dioden

Fast **R**ecovery **E**pitaxial **D**iode

Schnelle Leistungsdioden für superschnelle Schalter mit "Soft"-Abschaltverhalten.

Produktpalette

- Dioden im Bereich 1000 V ... 1200 V und 55 ns ... 150 ns

Applications (Selected)

- Frequency converters for three-phase drives
- Clocked power supplies for welding equipment
- Uninterruptible power supplies
- High-power switched-mode power supplies
- Automobile ignition systems

1.3 FRED Diodes

Fast **R**ecovery **E**pitaxial **D**iodes

Fast power diodes for extremely fast switches with soft recovery characteristics.

Product range

- Diodes in the 1000 V to 1200 V range and 55 ns to 150 ns

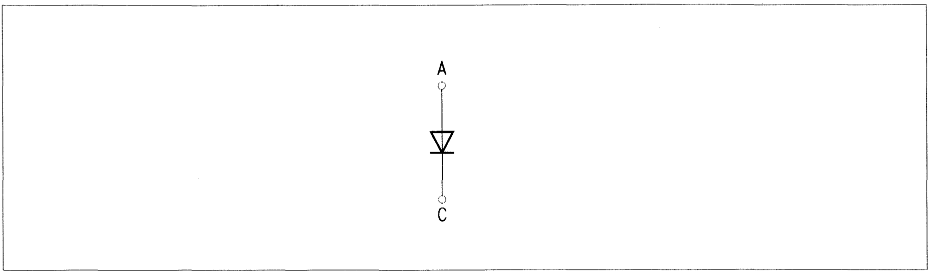


Bild 3
Schaltsymbol

Figure 3
Graphical symbol

Merkmale

- Superschneller Schalter
- Sanftes Abschaltverhalten
- Hohe Sperrspannung
- Geringe Speicherladung (wenige Mikrocoulomb)
- Niedrige Durchlaßspannung

Einsatzmöglichkeiten (Auswahl)

- Wechselrichter
- Motorsteuerungen
- Unterbrechungsfreie Stromversorgungen
- Frequenzumrichter für Drehstrom
- Getaktete Stromversorgungen

1.4 Chips

Siemens liefert auf Anfrage auch SIPMOS-Transistoren ohne Gehäuse.

Features

- Super high-speed switches
- Soft recovery
- High reverse voltage
- Low storage charge (a few microcoulombs)
- Low forward voltage

Applications (Selected)

- Inverters
- Motor control units
- Uninterruptible power supplies
- Static frequency changers for three-phase current
- Clocked power supplies

1.4 Chips

Siemens supplies SIPMOS transistors on request as an unpackaged chip.

2 Technologie

2.1 SIPMOS-Leistungstransistoren

2.1.1 Aufbau und Ersatzschaltbild

SIPMOS-Leistungstransistoren sind vertikal aufgebaut und haben eine doppelt implantierte Kanalstruktur, man spricht daher auch von einem DIMOS-Prozeß (vgl. **Bild 4**).

Bei einem N-Kanal-Transistor dient das n^+-Substrat als Träger mit der darunterliegenden Drainmetallisierung. Über dem n^+-Substrat schließt sich eine n^--Epitaxieschicht an, die je nach Sperrspannung verschieden dick und entsprechend dotiert ist. Das darüberliegende Gate aus n^+-Polysilizium ist in isolierendes Siliziumdioxyd eingebettet und dient als Implantationsmaske für die p-Wanne (Barrierregion) und für die n^+-Sourcezone. Die Sourcemetallisierung überdeckt die gesamte Struktur und schaltet die einzelnen Transistorzellen des Chips parallel.

2 Technology

2.1 SIPMOS Power Transistors

2.1.1 Structure and Equivalent Circuit Diagram

SIPMOS power transistors are vertically structured and have a double-implanted channel structure. We thus also speak of a DIMOS process (cf. **Figure 4**).

In the case of an N-channel transistor the n^+ substrate serves as the carrier with the drain plating below it. A n^- epitaxial layer, of varying thickness and suitably doped depending on the reverse voltage, follows over the n^+ substrate. The gate of n^+ polysilicon above it is embedded in insulating silicon dioxide and acts as an implantation mask for the p-tub (barrier region) and for the n^+ source region. The source plating covers the entire structure and connects individual transistor cells of the chip in parallel.

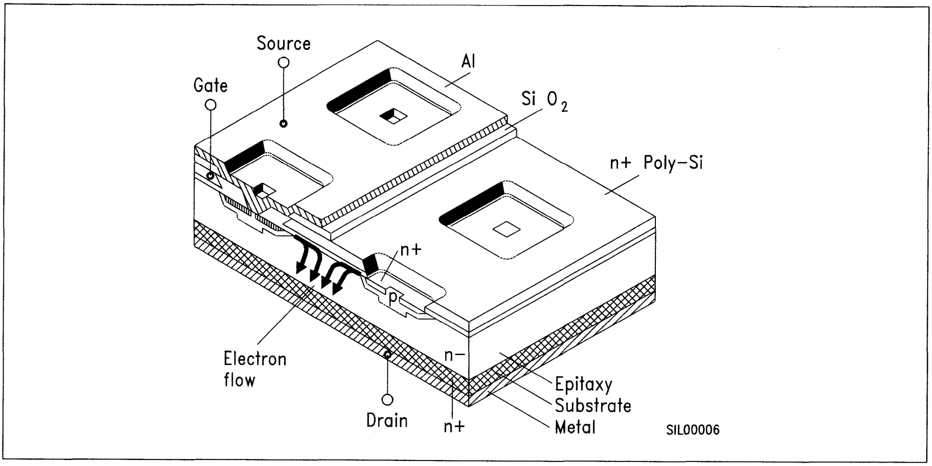


Bild 4
Aufbau eines N-Kanal-SIPMOS-Transistors

Die Sourcemetallisierung bildet einen sicheren Kurzschluß zwischen dem n^+- und p-Sourcegebiet (vgl. **Bild 5**). Dadurch wird die Basis-Emitter-Strecke des parasitären vertikalen n^+pn^--Bipolar-Transistors kurzgeschlossen. Das ist notwendig, um sein Einschalten bei dynamischen Vorgängen zu vermeiden. Selbst durch hohe Spannungsteilheiten zwischen Drain und Source, z.B. in der Größenordnung $> 2 \times 10^4$ V/µs werden die parasitären npn-Transistoren bei reinem Transistorbetrieb durch Ströme über die Drain-Source-Kapazität nicht eingeschaltet. Dieser Effekt muß allerdings dann beachtet werden, wenn in der Inversdiode hohe Kommutierungssteilheiten auftreten. Die Basis-Kollektor-Diode (pn^--Übergang) entspricht dabei der SIPMOS-Inversdiode.

Figure 4
Structure of an N channel SIPMOS Transistor

The source plating forms a reliable short-circuit between the n^+ and p-source region (cf. **Figure 5**). This shorts the base-emitter junction of the parasitic vertical n^+pn^- bipolar transistor. This is essential in order to prevent the transistor from turning on when subject to dynamic processes. In the case of pure transistor operation the parasitic npn-transistors are not turned on by currents resulting from the drain-source capacitance, not even as a result of high rates of voltage rise between the drain and source, e.g. of the order of $> 2 \times 10^4$ V/ s. However, attention should be paid to this effect if high rates of commutation voltage rise occur in the inverse diode. The base-collector diode (pn^- junction) then corresponds to the SIPMOS inverse diode.

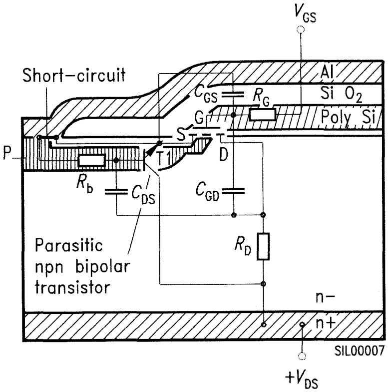


Bild 5
Parasitärer Bipolar-Transistor im Schnittbild eines N-Kanal-Transistors

Figure 5
Parasitic bipolar transistor in the sectional drawing of an N channel transistor

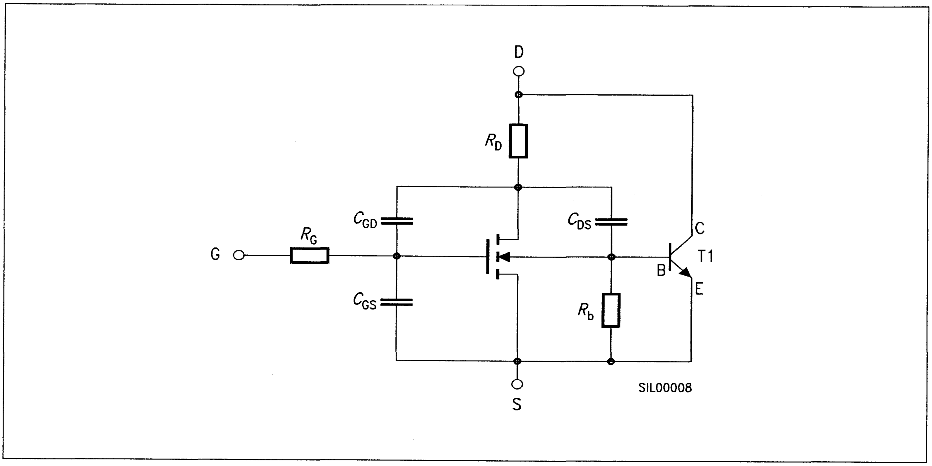


Bild 6
Ersatzschaltbild mit parasitärem Bipolar-Transistor

Der vertikale Transistoraufbau gewährleistet u.a. eine optimale Chipflächen-Ausnutzung, garantiert eine gute Wärmeableitung und ermöglicht hohe Sperrspannungen. Durch die Doppelimplantation mit den extrem kurzen Kanallängen sind sehr hohe Stromsteilheiten möglich.

Bei Leistungstransistoren erfolgt die Montage der Chips in die Gehäuse durch ein speziell erprobtes Weichlot-Verfahren. Das Kontaktieren der Anschlußdrähte auf den Chips wird mittels Ultraschall erreicht. Das Drahtmaterial ist ebenfalls – wie bei der Chip-Metallisierung – Aluminium. Die Drahtdicke wird durch den maximal zulässigen Drainstrom bestimmt.

Figure 6
Equivalent circuit diagram with parasitic bipolar transistor

The vertical transistor structure guarantees, *inter alia,* optimum utilization of the chip area and good heat dissipation, as well as allowing high reverse voltages. Very high rates of current rise are possible as a result of the double implantation with extremely short channel lengths.

With power transistors chips are mounted in their packages by means of a specially tested soft soldering method. The component leads are bonded on the chips by an ultrasonic method. As with the chip plating, the wire is likewise aluminum. The wire gauge is determined by the maximum permissible drain current.

Ersatzschaltbild

Man geht davon aus, daß zwischen den Anschlüssen komplexe Leitwerte und Bahnwiderstände auftreten. Dabei zeigen die Leitwerte zwischen den Anschlüssen bei gesperrtem Transistor kapazitives Verhalten. Die Kapazitäten heißen: Drain-Source-Kapazität C_{DS}, Gate-Source-Kapazität C_{GS} und Gate-Drain-Kapazität C_{GD} (auch Miller-Kapazität C_{Mi}). Der Gate-Bahnwiderstand R_{G} in der Größenordnung von einigen Ohm ist stark von der Chipgeometrie abhängig. In der Drain-Source-Strecke befindet sich im eingeschalteten Zustand der Drain-Source-Widerstand $R_{\mathrm{DS(on)}}$, der sich im wesentlichen aus der Summe des n^--Epitaxieschicht-Widerstandes R_{D} und dem Kanalwiderstand R_{K} zusammensetzt (vgl. **Bild 7**).

Equivalent Circuit Diagram

It is assumed that complex conductances and bulk resistances occur between the connections, the conductances exhibiting capacitive behavior when the transistor is reverse-biased. The capacitances are the drain-source capacitance C_{DS}, the gate-source capacitance C_{GS} and the gate-drain capacitance C_{GD} (also called Miller capacitance C_{Mi}). The gate bulk resistance R_{G} of the order of several ohms is strongly dependent on chip geometry. At the drain-source junction there is the drain-source resistance $R_{\mathrm{DS(on)}}$ at ON state which consists essentially of the sum of the n^--epitaxial layer resistance R_{D} and the channel resistance R_{K} (cf. **Figure 7**).

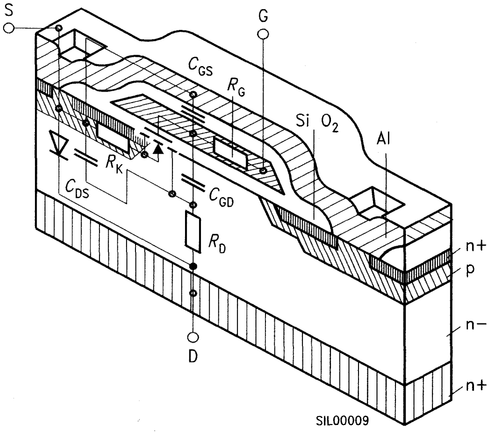


Bild 7
Schnittbild eines N-Kanal-Transistors mit dargestellten Leitwerten des Ersatzschaltbildes

Figure 7
Sectional drawing of an N channel SIPMOS transistor showing the conductances of the equivalent circuit diagram

Bei Niederspannungs-Transistoren ($V_{DS} \leq 100$ V) dominiert der Kanalwiderstand R_K, bei höher sperrenden Typen ($V_{DS} > 100$ V) ist es der Epitaxieschicht-Widerstand R_D. Damit gelangt man zu den vereinfachten **Ersatzschaltbildern 8 und 9**. Bei den gezeigten Ersatzschaltbildern handelt es sich um Näherungen, da auf einem Chip bis zu 6000-Transistor-Einzelzellen parallelgeschaltet sind. Man hat es also mit verteilten Kapazitäten und Bahnwiderständen zu tun, und diese ändern sich (größtenteils) in Abhängigkeit der Drain-Source-Spannung.

In low-voltage transistors ($V_{DS} \leq 100$ V) the channel resistance R_K predominates, whereas in higher blocking types ($V_{DS} > 100$ V) the epitaxial layer resistance R_D predominates. In this way we arrive at the simplified equivalent circuit diagrams shown in **Figures 8 and 9**. The equivalent circuit diagrams in the figures are approximations, since up to 6000 transistor individual cells are connected in parallel on a chip. Distributed capacitances and bulk resistances are therefore involved, and these vary, for the most part, as a function of drain-source voltage.

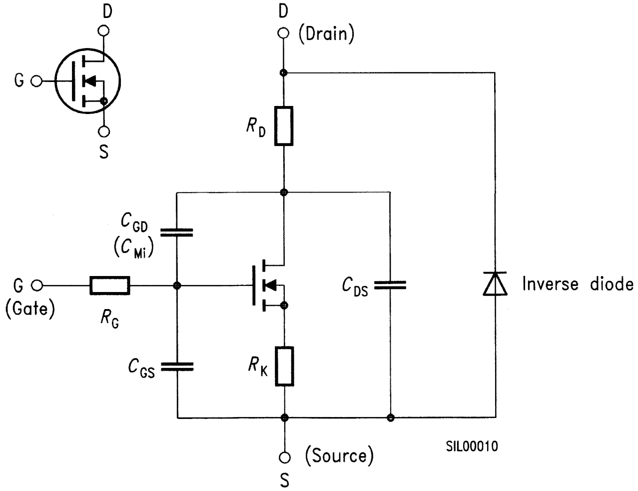


Bild 8
Schaltsymbol und Ersatzschaltbild eines N-Kanal-SIPMOS-Transistors

Figure 8
Graphical symbol and equivalent circuit diagram of an N channel SIPMOS transistor

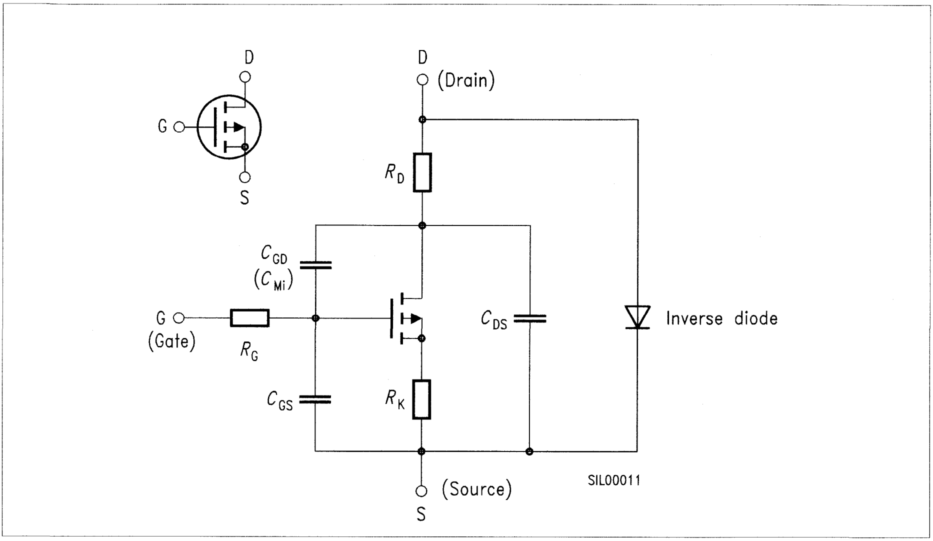


Bild 9
Schaltsymbol und Ersatzschaltbild eines P-Kanal-SIPMOS-Transistor

Gravierende Auswirkungen auf das Schaltverhalten hat die Spannungsabhängigkeit der Gate-Drain- bzw. Miller-Kapazität.

Bei einer vereinfachten Darstellung ergibt sich bei Drain-Source-Spannungen kleiner gleich der Gate-Source-Einsatzspannung eine sprunghafte Erhöhung der Miller-Kapazität um etwa den Faktor 10 (vgl. **Bild 10**). Tatsächlich setzt die Kapazitätserhöhung schon etwas früher ein und nimmt zur idealisierten Sprungstelle hin exponentiell zu (vgl. Kurven im Datenblatt).

Die im Ersatzschaltbild angegebenen Kapazitäten sind nicht einzeln meßbar, sie

Figure 9
Graphical symbol and equivalent circuit diagram of a P channel SIPMOS transistor

Serious effects on switching response are produced by the voltage dependence of the gate-drain and Miller capacitances.

In a simplified representation the Miller capacitance soars by a factor of approximately ten at drain-source voltages less than or equal to the gate-source threshold voltage (cf. **Figure 10**). In actual fact, the increase in capacitance commences somewhat earlier and rises exponentially to the idealized point at which it soars (cf. curves on data sheet).

The capacitances in the equivalent circuit diagram cannot be measured individusind nur als verknüpfte Größen zu betrachten (vgl. **Bild 11**). Zwischen ihnen besteht unter Vernachlässigung der Bahnwiderstände folgender Zusammenhang:

ally; they should be regarded as associated magnitudes (cf. **Figure 11**). Ignoring the bulk resistances, they are interrelated as follows:

Eingangskapazität/Input capacitance $C_{iss} \sim C_{GS} + C_{GD}$

Rückwirkungskapazität/Reverse transfer capacitance $C_{rss} \sim C_{GD}$ $(C_{GD} = C_{Mi})$

Ausgangskapazität/Output capacitance $C_{oss} \sim C_{DS} + C_{Mi}$

Dabei beziehen sich die tabellierten Datenbuchangaben auf einen bestimmten Arbeitspunkt.

The details listed in the Data Book tables relate to a certain operating point.

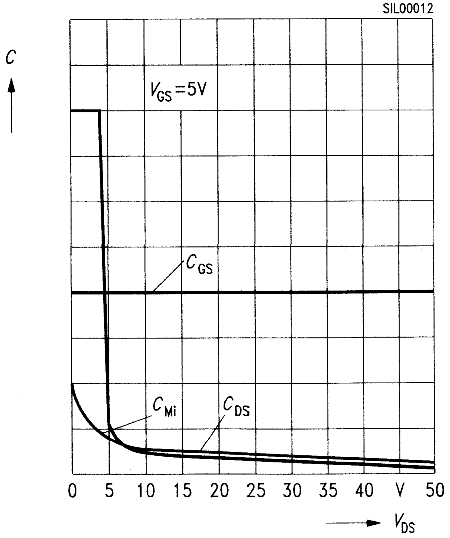


Bild 10
Spannungsabhängigkeit Kapazitäten des Ersatzschaltbildes

Figure 10
Voltage dependence of equivalent circuit diagram capacitances

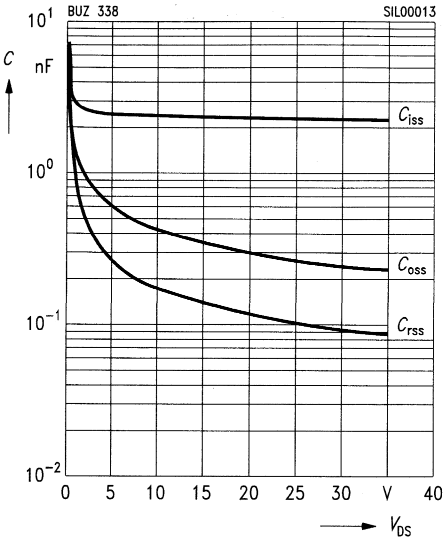


Bild 11
Spannungsabhängigkeit der verknüpften Kapazitäten
(Beispiel: BUZ 338 Parameter:
V_{GS} = 0 V, f = 1 MHz)

2.1.2 Kennlinienfeld

Liegt an einem N-Kanal-Transistor positive Drain-Source-Spannung bei Steuerspannung $V_{GS} = 0$ V, so fließt ein temperatur- und spannungsabhängiger Sperrstrom. Dieser Sperrstrom-Grenzwert ist in den Datenblättern spezifiziert und beträgt typisch – bei 25 °C – wenige nA. Steigert man die Gate-Source-Steuerspannung, bleibt der Transistor gesperrt bis die Gate-Source-Einsatzspannung (Gate-Source-Schwellenspannung) $V_{GS(th)}$ erreicht ist. Erhöht man die Steuerspannung über die Einsatzspannung hinaus, nimmt der Drain-

Figure 11
Voltage dependence of associated capacitances
(example: BUZ 338; parameters:
V_{GS} = 0 V, f = 1 MHz)

2.1.2 Family of Characteristics

If positive drain-source voltage is applied to an N-channel transistor with a control voltage $V_{GS} = 0$ V, a temperature- and voltage-dependent reverse current will flow. The limiting value of this reverse current is specified in the data sheets and is typically a few nA at 25 °C. If the gate-source control voltage is increased, the transistor will remain reverse-biased until the gate-source threshold voltage $V_{GS(th)}$ is reached. If the control voltage is raised above the threshold voltage, the drain current increases in accordance with the strom entsprechend der Transfer-Kennlinie zu (vgl. Übertragungscharakteristik **Bild 12**). Die Übertragungssteilheit g_{fs} ist nicht linear, sie liegt in einem Bereich zwischen 1 S und 30 S und hängt von der Chipfläche, dem Design und von der max. Sperrspannung V_{DSS} des Transistors ab (vgl. Datenblatt).

transfer characteristic (cf. **Figure 12**). The transconductance g_{fs} is non-linear, lying in a range between 1 S and 30 S, and depends on the chip area, design and maximum reverse voltage V_{DSS} of the transistor (cf. data sheet).

$$g_{fs} = \left. \frac{dI_D}{dV_{GS}} \right| T_j$$

Der Schnittpunkt der Übertragungskennlinie im kalten und warmen Zustand (vgl. **Bild 12**) bewirkt eine thermische Eigenstabilität bei hohen Strömen (kein Second Breakdown).

Die Gate-Source-Schwellenspannung $V_{GS(th)}$ liegt bei Leistungs-MOSFET zwischen 2,1 V ... 4,0 V (bei $I_D = 1$ mA) und hat einen negativen Temperaturkoeffizienten von ca. 5 mV/K

The intersection of the transfer characteristic in the cold and warm states (cf. **Figure 12**) causes a thermal inherent stability at high currents (no second breakdown).

With power MOSFETs the gate-source threshold voltage $V_{GS(th)}$ is between 2.1 and 4.0 V (when $I_D = 1$ mA) and has a negative temperature coefficient of approximately -5 mV/K.

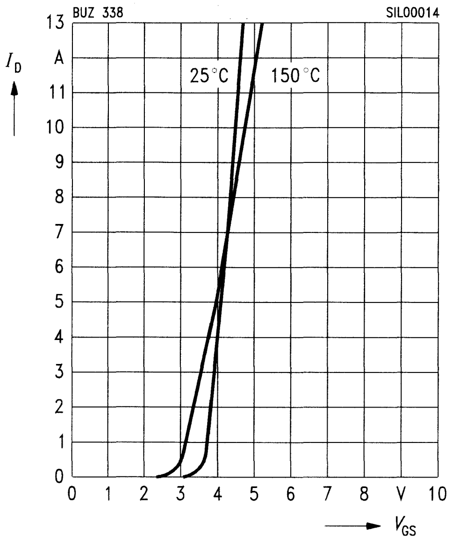


Bild 12
Typische Übertragungscharakteristik (Beispiel: BUZ 338, Parameter: 80-µs-Pulstest, V_{DS} = 25 V, T_j = 25 °C und 150 °C)

Bei einer Gate-Spannung unterhalb der Einsatzspannung ist der Transistor gesperrt. Eine negative Gate-Source-Spannung erhöht die Sperrfähigkeit nicht, d.h. daß mit Steuerspannungen einer Polarität das gesamte Kennlinienfeld durchfahren werden kann.
Der Maximalwert der Gate-Source-Spannung beträgt ± 20 V, bei Logik Level-Transistoren ± 10 V, und ist durch die Oxyddicke begrenzt. Dieser Wert darf nicht, auch nicht kurzfristig, überschritten werden, da sonst eine Beschädigung auftreten kann, und der Transistor dann nicht mehr steuerbar ist.

Figure 12
Typical transfer characteristic (example: BUZ 338, parameters: 80 µs pulse test, V_{DS} = 25 V, T_j = 25 °C and 150 °C)

The transistor is reverse-biased in the case of a gate voltage lower than the threshold voltage. A negative gate-source voltage does not increase the blocking ability, i.e the entire family of characteristics can be obtained with control voltages of one polarity.
The maximum value of the gate-source voltage is ± 20 V and with logic level transistors it is ± 10 V; it is limited by the thickness of the oxide. This value must not be exceeded, not even briefly, since damage may otherwise occur and the transistor can then no longer be controlled.

Mißt man den Drainstrom in Abhängigkeit der Drain-Source-Spannung mit dem Parameter Gate-Source-Steuerspannung, so erhält man das Ausgangskennlinienfeld (vgl. **Bild 13**).

Im "Ein-Zustand" verhält sich der Transistor wie ein ohmscher Widerstand, d.h. es können auch negative Drainströme fließen: Im III. Quadranten des Kennlinienfeldes tritt natürlich nur soweit ein ohmsches Verhalten auf, wie die Schwellenspannung der Inversdiode noch nicht überschritten ist (vgl. **Bild 14**). Dieses Verhalten ist besonders dann wichtig, wenn Gleichrichterschaltungen mit extrem niedrigen Durchlaßspannungen realisiert werden sollen oder wenn die Inversdioden-Sperrverzögerungszeit durch das Aufsteuern des Transistors verkürzt werden muß.

If the drain current is measured as a function of the drain-source voltage with the gate-source control voltage as a parameter, we obtain the family of output characteristics (cf. **Figure 13**).

At ON state the transistor behaves in the same way as an ohmic resistance, i.e. negative drain currents can also flow. In the third quadrant of the family of characteristics an ohmic behavior does, of course, occur only to such an extent as the threshold voltage of the inverse diode has not yet been exceeded (cf. **Figure 14**). This behavior is particularly important if rectifier circuits having extremely low forward-biased state voltages are to be implemented or if the inverse diode reverse recovery time is to be shortened by biasing the transistor.

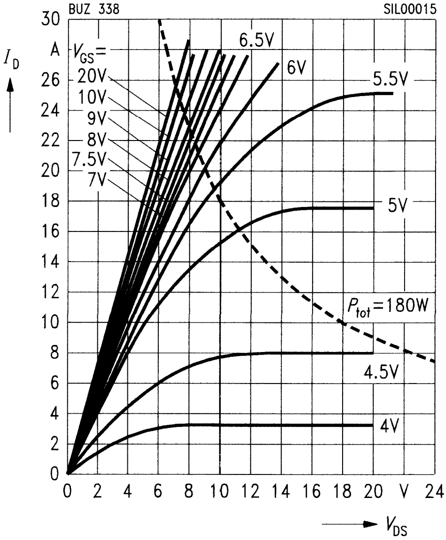
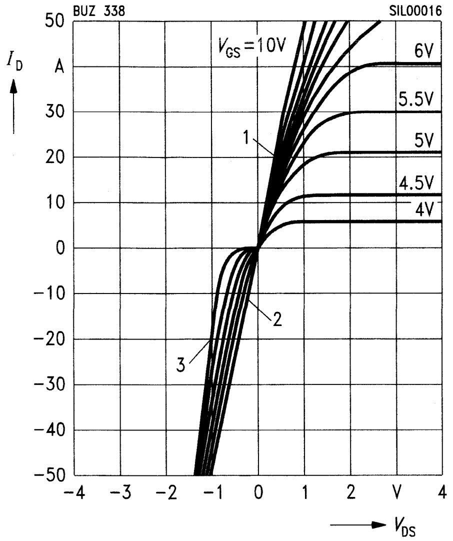


Bild 13
Typ. Ausgangscharakteristik
(Beispiel: BUZ 338, Parameter: 80-µs-Pulstest, T_C = 25 °C)

Figure 13
Typical output characteristic
(example: BUZ 338, parameters: 80 µs pulse test, T_C = 25 °C)



1) Transistor output characteristics
2) Inverse transistor output characteristics
3) Inverse diode forward characteristics

Bild 14
Ausgangscharakteristik mit Inversdioden-Verhalten

Figure 14
Output characteristic with inverse diode behavior

2.1.3 Schaltvorgänge

SIPMOS-Transistoren sind spannungsgesteuert und benötigen daher im stationären Betriebszustand keine Steuerleistung. Bei jeder Betriebszustandsänderung entstehen jedoch Umladeströme der Eingangskapazitäten. Während diese Ströme im NF-Bereich (Analogbetrieb) kaum von Bedeutung sind, müssen sie bei HF-Anwendungen im Schaltbetrieb beachtet werden. Da SIPMOS-Transistoren vornehmlich als Schalter eingesetzt werden, wird das Schaltverhalten besonders erläutert. Die Schaltzeit eines SIPMOS-Transistors wird nur durch das Umladen der Eingangs- und Millerkapazität sowie von dem inneren Gatebahnwiderstand bestimmt. Durch die freie Wahl des Innenwiderstandes R_i der Ansteuerschaltung läßt sich die Schaltzeit in einem weiten Bereich einstellen. Die Grenze für einen hochohmigen Innenwiderstand ist infolge erhöht auftretender Schaltverluste durch die thermische Belastbarkeit gegeben. Bei einer niederohmigen Ansteuerschaltung ergibt sich eine Begrenzung des Umladestroms der Kapazitäten durch den Gate-Bahnwiderstand und der Induktivität des Steuerkreises.

Schalten bei ohmscher Last

Zum Einsatz kommt ein Ansteuergenerator mit definiertem Innenwiderstand R_i, der eine Rechteckausgangsspannung liefert (vgl. Meßschaltung für Schaltzeiten).

Einschaltvorgang

Zum Zeitpunkt t_0 wird der Transistor angesteuert (vgl. **Bild 15**). Die Gate-Source-

2.1.3 Switching Operations

SIPMOS transistors are voltage-controlled and therefore require no gate power in the steady operating state. Each change in operating state, however, causes charge-reversal currents of the input capacitances. While hardly significant in the VF range (analog operation), the currents must not be ignored in the case of RF applications in switching operations. Since SIPMOS transistors are primarily used as switches, their switching response will be described in detail. The switching time of a SIPMOS transistor is determined only by charge reversal of the input and Miller capacitances, and by the internal gate bulk resistance. The switching time can be set over a wide range by freely selecting the internal resistance R_i of the drive circuit. The limit for a high internal resistance is set by the thermal load rating owing to the occurrence of higher switching losses. With a low-resistance drive circuit the charge-reversal current of the capacitances is limited by the gate bulk resistance and the inductance of the control circuit.

Switching with Resistive Load

A control generator of defined internal resistance R_i is used for supplying a square-wave output voltage (cf. test circuit for switching times).

Turn-On

The transistor is triggered at t_0 (cf. **Figure 15**). The gate-source voltage V_{GS}

Spannung V_{GS} steigt entsprechend dem Ladevorgang, der durch die Eingangskapazität C_{iss} und den Innenwiderstand R_i der Steuerschaltung entsteht.

Sobald die Einsatzspannung im Zeitpunkt t_1 erreicht ist, beginnt der Transistor Strom zu führen. Die Drain-Source-Spannung V_{DS} sinkt entsprechend dem zunehmenden Spannungsabfall am Lastwiderstand.

rises in accordance with the charging process resulting from the input capacitance C_{iss} and the internal resistance R_i of the control circuit.

As soon as the threshold voltage is reached at t_1, the transistor starts conducting current. The drain-source voltage V_{DS} falls in accordance with the increasing voltage drop at the load resistor.

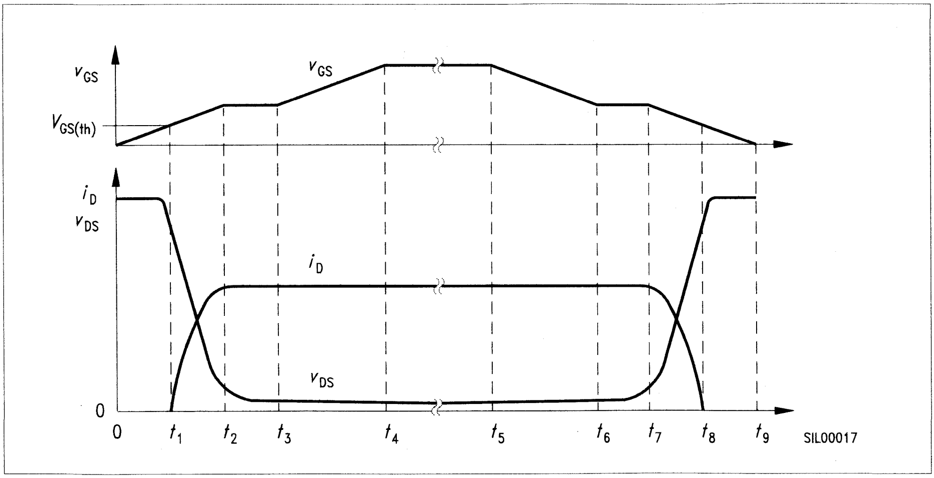


Bild 15
Schaltvorgang bei ohmscher Last

Figure 15
Switching operation with resistive load

Im Zeitabschnitt t_1 bis t_2 steigt der Drainstrom I_D. Dabei wird die zu diesem Zeitpunkt kleine Miller-Kapazität mit dem Drain-Source-Spannungshub entladen, und gleichzeitig nimmt die Gate-Source-Spannung V_{GS} entsprechend der Transfer-Kennlinie zu (vgl. **Bild 12**). Im Zeitpunkt t_2 ist die Drain-Source-Spannung V_{DS} gleich der Gate-Source-Spannung V_{GS}. Nun wirkt die stark erhöhte Miller-Kapazität. Im Zeit-

The drain current I_D rises between t_1 and t_2. The currently low Miller capacitance is discharged with the drain-source voltage excursion and the gate-source voltage V_{GS} rises simultaneously in accordance with the transfer characteristic (cf. **Figure 12**). The drain-source voltage V_{DS} equals the gate-source voltage V_{GS} at t_2. The Miller capacitance, now far higher, then takes effect. The transistor operates as a Miller abschnitt t_2 bis t_3 arbeitet der Transistor als Miller-Integrator, d.h. die Gate-Source-Spannung bleibt konstant, während der Gate-Ladestrom über die Miller-Kapazität fließt und zu einer weiteren Drain-Source-Spannungsabsenkung führt.

Im Zeitpunkt t_3 hat die Drain-Source-Spannung das Bereichsende des Ausgangs-Kennlinienfeldes und die Miller-Kapazität ihren größten Wert erreicht. Im Verlauf t_3 bis t_4 wird die Eingangskapazität C_{iss} auf das Niveau der angelegten Steuerspannung geladen. Dabei verringert sich der Kanalwiderstand weiter. Dies ist im Kennlinienfeld an der Kurvenscharscherung im ohmschen Bereich zu erkennen.

Im Zeitpunkt t_4 hat der Transistor seinen niedrigsten Durchlaßwiderstand (Einschaltwiderstand $R_{DS(on)}$ erreicht (entspricht der Drain-Source-Restspannung dividiert durch den Drainstrom).

Abschaltvorgang

Der Abschaltvorgang wird im Zeitpunkt t_5 durch das Ausschalten der Steuerspannung eingeleitet. Die zu diesem Zeitpunkt höchste Eingangskapazität C_{iss} entlädt sich über den Innenwiderstand R_i des Ansteuergenerators. Die Gate-Source-Spannung sinkt auf einen Wert, bei dem der momentane Drainstrom gerade noch im ohmschen Bereich des Kennlinienfeldes gehalten werden kann.

Dies ist im Zeitpunkt t_6 erreicht, wobei der Durchlaßwiderstand geringfügig zugenommen hat.

Im Zeitabschnitt t_6 bis t_7 wirkt der Transistor wiederum als Miller-Integrator, d.h.

integrator between t_2 and t_3, i.e. the gate-source voltage remains constant while the gate charging current flows across the Miller capacitance and results in a further drop in drain-source voltage.

At t_3 the drain-source voltage has reached the end of the range of the family of characteristics, and the Miller capacitance has reached its highest value. The input capacitance C_{iss} is charged to the level of the applied control voltage between t_3 and t_4. The channel resistance is reduced further. This can be seen in the family of characteristics at the shear of the family of curves in the ohmic region.

The transistor has reached its lowest forward resistance (ON resistance $R_{DS(on)}$ at t_4 (corresponding to the drain-source saturation voltage divided by the drain current).

Turn-Off

Turn-off is initiated at t_5 by switching off the control voltage. The input capacitance C_{iss}, which is at its highest at this point in time, is discharged via the internal resistance R_i of the drive generator. The gate-source voltage falls to a value at which the instantaneous drain current can just be maintained in the ohmic region of the family of characteristics.

This is achieved at t_6, the forward resistance having increased slightly.

Between t_6 and t_7 the transistor again acts as a Miller integrator, i.e. the gate-source die Gate-Source-Spannung bleibt konstant, während der Gate-Steuerstrom vollständig über die noch immer erhöhte Miller-Kapazität fließt und zu einem Drain-Source-Spannungsanstieg führt. Im Zeitpunkt t_7 herrscht Spannungsgleichheit zwischen der momentanen Gate-Source-Spannung und der Drain-Source-Spannung, d.h. die Miller-Kapazität sinkt auf einen kleinen Wert.

Im Zeitabschnitt t_7 bis t_8 erfolgt die Ladung der nun kleineren Miller-Kapazität entsprechend der rasch ansteigenden Drain-Source-Spannung. Gleichzeitig nimmt der Drainstrom entsprechend dem sinkenden Spannungsabfall am Lastwiderstand ab, ebenso die Gate-Source-Spannung.

Im Zeitpunkt t_8 ist die Einsatzspannung erreicht und der Transistor vollständig gesperrt. Danach folgt die Entladung der Eingangskapazität auf das Steuerspannungsniveau im Zeitabschnitt t_8 bis t_9.

2.1.4 Sicherer Arbeitsbereich (SOA)

Safe **O**perating **A**rea

Der SIPMOS-Transistor ist aufgrund seiner Technologie ein überaus robustes Bauelement. Die Zellenstruktur bewirkt eine vorteilhafte Verlustwärmeverteilung im Chip; der positive Temperaturkoeffizient aller an der Stromführung beteiligten Bereiche sorgt für eine Eigenstabilisierung. Die Source-Metallisierung bildet einen sicheren Kurzschluß für die Basis-Emitter-Strecke des im Transistor enthaltenen parasitären Bipolar-Transistors. Auf diese Weise wird ein *Aufsteuern* die-

voltage remains constant while the gate control current flows completely across the Miller capacitance, which is still high, and results in a rise in the drain-source voltage. The instantaneous gate-source voltage and the drain-source voltage are at equilibrium at t_7, i.e. the Miller capacitance falls to a low value.

Between t_7 and t_8 the Miller capacitance, now lower, is charged in accordance with the rapidly rising drain-source voltage. At the same time the drain current falls at the load resistor in accordance with declining voltage drop, and the gate-source voltage likewise.

The threshold voltage is reached at t_8, and the transistor is completely reverse-biased. This is followed by discharging of the input capacitance to control voltage level between t_8 and t_9.

2.1.4 Safe Operating Area (SOA)

Safe **O**perating **A**rea

By virtue of its technology, the SIPMOS transistor is an extremely robust device. Its cellular structure ensures advantageous dissipation-heat distribution over the chip; the positive temperature coefficient of all current-conducting areas ensures inherent stabilization. The source plating forms a reliable short-circuit for the base-emitter junction of the parasitic bipolar transistor contained in the transistor. In this way *biasing* of this bipolar transistor, with the possible consequence of ses Bipolar-Transistors mit der möglichen Folge eines zweiten Durchbruchs in allen Betriebsfällen verhindert (Ausnahme: bei zu hohen Kommutierungssteilheiten des Inversdiodenstroms).

Besonders erwähnenswert ist die hohe Strombelastbarkeit eines SIPMOS-Transistors. So ist z.B. ein gepulster Drainstrom in vierfacher Höhe zulässig (bezogen auf den zulässigen DC-Drainstrom).

Kurzzeitig darf dieser Pulsdrainstrom sogar bei maximaler Sperrspannung geführt werden (vgl. **Bild 16**). Dabei darf die Sperrspannung jedoch nicht, auch nicht kurzzeitig, überschritten werden. Neben den im Datenblatt angegebenen Grenzwerten für die Draingleichstrom ist der gesamte thermische Widerstand $R_{\mathrm{(th)JA}}$ (Chip-Umgebung) maßgebend für den zulässigen Drainstrom im Betrieb.

second breakdown in all operating cases, is prevented. (An exception to this occurs at high rates of commutation current rise of the inverse diode current.)

Particular mention should be made of the high current-carrying capacity of a SIPMOS transistor. A fourfold pulsed drain current (relative to the permissible DC drain current) is permissible, for example.

In the short term this pulsed drain current can even be conducted at maximum reverse voltage (cf. **Figure 16**). In this case the reverse voltage must not be exceeded, not even briefly. Apart from the maximum ratings for the DC drain current shown in the data sheet, the total thermal resistance $R_{\mathrm{(th)JA}}$ (chip to ambient air) is decisive for the drain current permissible in operation.

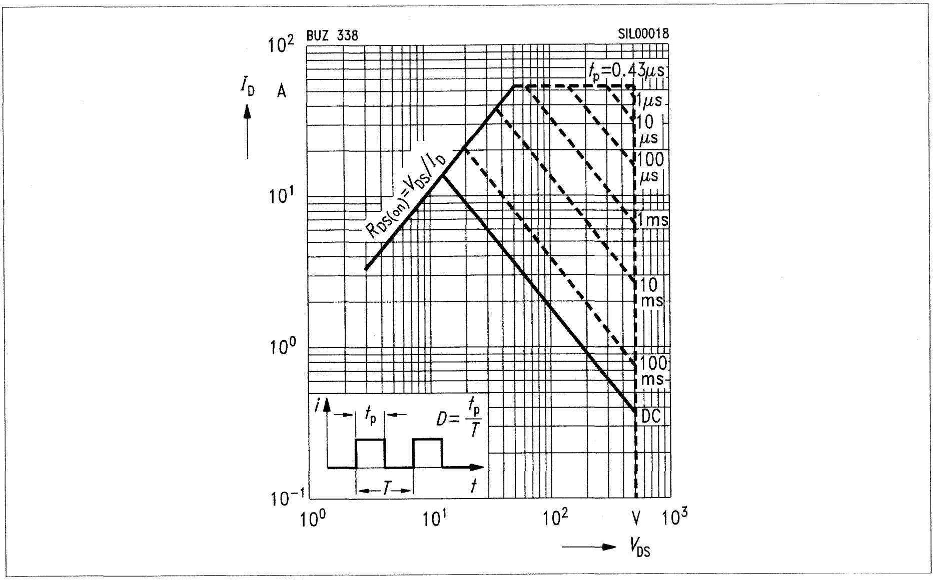


Bild 16
Sicherer Arbeitsbereich
(Beispiel: BUZ 338,
Parameter: D = 0,01, T_C = 25 °C)

2.1.5 Inversdiode

Bedingt durch den Transistoraufbau fließt bei negativer Drain-Source-Spannung ein Strom über den pn-Übergang von Source zu Drain. Diese Diodenfunktion ist ein integraler Bestandteil und wird in den Datenblättern spezifiziert. Die Durchlaßspannung der Inversdiode beträgt 1 ... 1,5 V. Die Sperrverzögerungszeit ist typabhängig und beträgt bei 50-V-Typen ca. 150 ns und steigt mit höher werdender Transistor-Sperrspannung bis ca. 1800 ns an.

Beim Einsatz in Halb- oder Vollbrücken-

Figure 16
Safe operating area
(example: BUZ 338,
parameters: D = 0.01, T_C = 25 °C)

2.1.5 Inverse Diode

The transistor structure causes a current to flow across the pn-junction from source to drain with negative drain-source voltage. This diode function is an integral component and is specified in the data sheets. The forward voltage of the inverse diode is 1 to 1.5 V. The reverse recovery time depends on the type concerned, and for 50 V types it is approximately 150 ns, rising to about 1800 ns with increasing reverse voltage of the transistor.

When used in half-bridge or full-bridge circuits with an inductive load, it is advisschaltungen mit induktiver Last liegt es nahe, die vorhandene Inversdiode als Freilaufdiode zu verwenden. Das kann bei Sperrspannungen > 200 V auf Grund der relativ hohen Sperrverzögerungszeiten während der Kommutierung zu Problemen führen. Erfolgt die Kommutierung zu schnell (großes di_F/dt) kann es bei Standard-Transistoren zum Einschalten des parasitären Bipolar-Transistors und damit zur Zerstörung des MOSFET kommen.

FREDFET

Fast-**R**ecovery-**E**pitaxial-**D**ioden-**F**eldeffekt-**T**ransistor

Um das Projektieren zu vereinfachen, wurde der FREDFET entwickelt. **Bild 17** zeigt eine Halbbrückenschaltung. Mit FREDFET ist diese Schaltung ohne zusätzliche Schutzbauelemente voll funktionsfähig. Durch eine Schwermetalldotierung werden der FET-Inversdiode FRED-Eigenschaften gegeben, ohne andere Parameter des Transistors zu beeinflussen.

Durch die superschnelle Inversdiode wird die Rückstromladung um Größenordnungen reduziert. Damit verringert sich die maximale Rückstromspitze von i_2 während der Kommutierung entsprechend (vgl. **Bild 18**). Das Einschalten des parasitären Bipolar-Transistors kann somit nicht mehr auftreten und gleichzeitig wird ein Überlasten von T_2 verhindert.

able to use the integrated inverse diode as a free-wheeling diode. At reverse voltages above 200 V this may result in problems during commutation due to the relatively high reverse recovery times. If commutation is performed too quickly (high di_F/dt), it might result in the parasitic bipolar transistor being turned on, and thus in the MOSFET being destroyed, in the case of standard transistors.

FREDFET

Fast **R**ecovery **E**pitaxial **D**iode **F**ield-Effect **T**ransistor

The FREDFET was developed to simplify designing. **Figure 17** shows a half-bridge circuit. With FREDFET this circuit is fully capable of functioning without additional protective devices. Heavy-metal doping provides the FET inverse diode with FRED characteristics without other parameters of the transistor being affected.

The super-high-speed inverse diode reduces reverse current charging by several orders of magnitude. Consequently the maximum reverse current peak of i_2 is decreased accordingly during commutation (cf. **Figure 18**). Turn-on of the parasitic bipolar transistor can thus not recur, and overloading of T_2 is prevented at the same time.

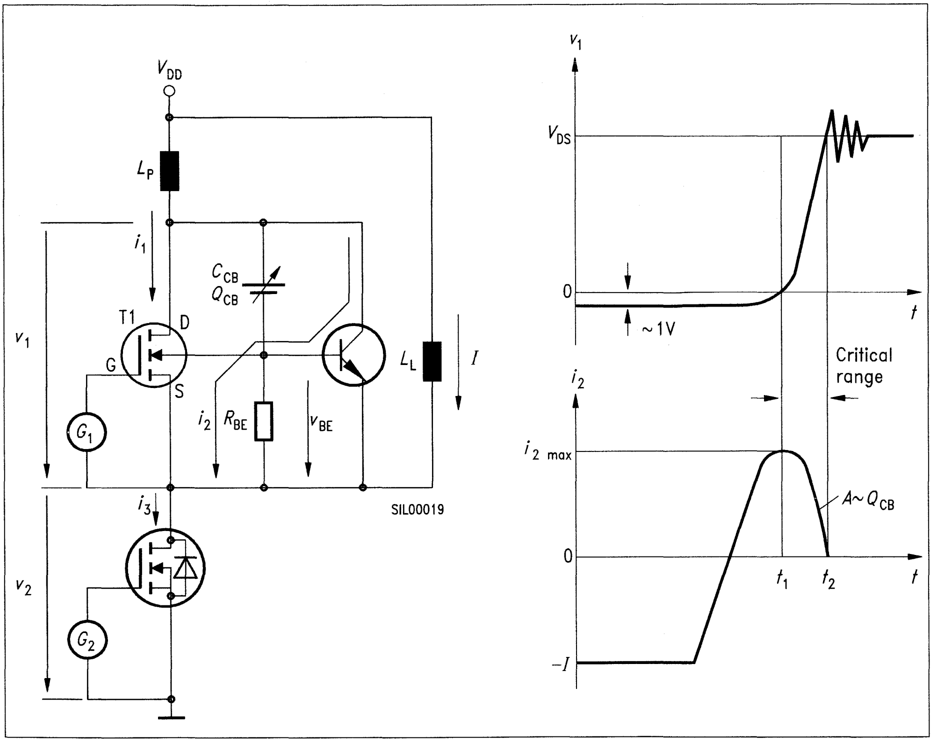


Bild 17
SIPMOS-Ersatzschaltbild einer Halbbrücke

Figure 17
SIPMOS equivalent circuit diagram of a half bridge

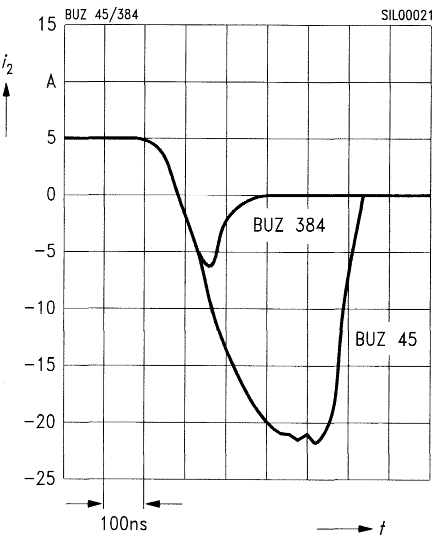


Bild 18
Rückstromverlauf FREDFET BUZ 384 verglichen mit einem BUZ 45 (Standard), d*i*/d*t* = 100 A/µs

2.1.6 Durchbruchfestigkeit (Avalanchefestigkeit)

Ein Maß für die Robustheit von MOSFET ist die Überspannungsfestigkeit. Durch die unvermeidlichen parasitären Induktivitäten L_p, die sich in einem auch sehr sorgfältigen Schaltungsaufbau befinden, kommt es beim Abschalten von Transistoren zum Auftreten von Überspannung.
SIPMOS Leistungstransistoren sind mit wenigen Ausnahmen avalanchefest. Man erkennt die Avalanchefestigkeit an dem Balken des Bauteilstempelbildes über dem Herstellercode, z.B. V245.

Figure 18
Reverse current curve of the FREDFET BUZ 384 compared with a BUZ 45 (standard), d*i*/d*t* = 100 A/µs

2.1.6 Breakdown Strength (Avalanche Resistance)

A criterion for the robustness of MOSFETs is their surge strength. Owing to the inevitable parasitic inductances L_p which occur even in very carefully designed circuits, an overvoltage is caused whenever transistors are turned off.
SIPMOS power transistors are, with a few exceptions, avalanche resistent. Avalanche resistance is identified by the bar shown on the module symbol that is placed above the manufacturer code, e.g. V245.

$$V = L_p \times \mathrm{d}i/\mathrm{d}t$$

Bedingt durch die kurzen Schaltzeiten von MOSFET wird das beim Schalten hoher Ströme besonders kritisch, denn die beim Abschalten auftretenden Spannungsspitzen können die Durchbruchsspannung $V_{BR(DSS)}$ des Transistors überschreiten.

Der Transistor geht dabei in den Durchbruch (Avalanche). Das wird verhindert durch ein sorgfältiges Transistordesign, das die parasitäre, bipolare Struktur am Einschalten hindert und damit den Transistor zerstört.

Alle avalanche spezifizierten Transistoren werden einem 100-%-Durchbruchtest unterzogen. **Bild 19** zeigt das Prinzipschaltbild der Testschaltung. Der Prüfling befindet sich in Serie mit einer ungeklemmten Induktivität L, und nachdem er eingeschaltet wird, steigt der Strom linear an, bis er seinen spezifizierten Nennstrom erreicht hat.

Wenn der Transistor abgeschaltet wird, bildet sich über dem Prüfling – abhängig von der Induktivität – eine Drain-Source-Spannung aus, die auf die Durchbruchspannung $V_{BR(DSS)}$ des Bauelements begrenzt wird. Dabei wird im Bauteil die Energie E_A, die in der Spule gespeichert ist, und ein Anteil aus der Spannungsquelle umgesetzt.

As a result of the very short switching times of MOSFETs, this becomes particularly critical upon switching high currents since the glitches occurring upon turn-off may exceed the breakdown voltage $V_{BR(DSS)}$ of the transistor.

The transistor then breaks down (avalanche). This is prevented by careful transistor design, which keeps the parasitic bipolar structure from turning on and thus not destroing the transistor.

All avalanche specify transistors are subjected to a 100 % breakdown test. **Figure 19** illustrates the basic circuit diagram of the test circuit. The device under test is in series with an unclamped inductance L, and once it has been turned on, the current rises linearly until it reaches its specified rated current.

When the transistor is turned off, a drain-source voltage is formed, depending on the inductance, over the device under test, being limited to the breakdown voltage $V_{BR(DSS)}$ of the device. In this case the energy E_A stored in the coil is converted in the device together with part of the source voltage.

$$E_A = 1/2\, L \times I_D^2 \times V_{BR(DSS)} / (V_{BR(DSS)} - V_{DD})$$

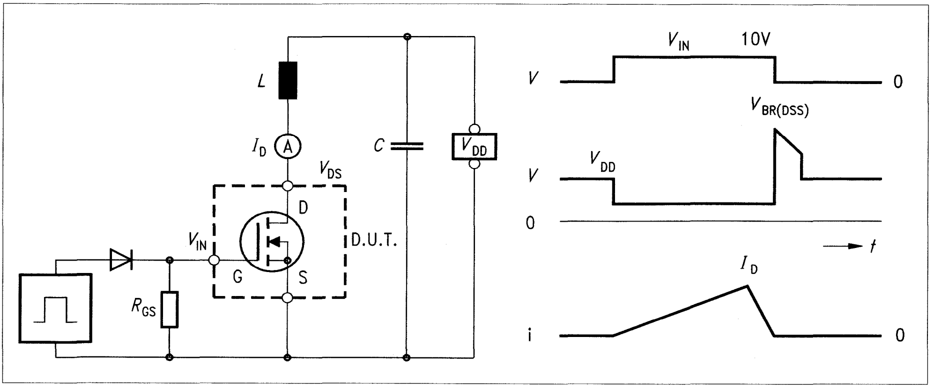


Bild 19
Schaltung zur Messung der Durchbruchfestigkeit

Die Energie, die im Transistor umgesetzt werden kann, ist durch die maximal zulässige Chiptemperatur T_j begrenzt. **Bild 20** zeigt die maximal zulässige Durchbruchenergie in Abhängigkeit von der Chiptemperatur.

In der Anwendung muß berücksichtigt werden, daß die im Durchbruch verursachten Verluste zusätzlich zu den Schaltverlusten und Durchlaßverlusten auftreten.

Figure 19
Circuit for measuring breakdown strength

The energy that can be converted in the transistor is limited by the maximum permissible chip temperature T_j. **Figure 20** shows the maximum permissible breakdown energy as a function of chip temperature.

In practice, account must be taken of the fact that losses caused by breakdown occur in addition to switching losses and forward power losses.

$$P_{tot} = P_{sw} + P_F + P_A$$
$$P_A = E_A \times f$$

Deshalb muß das Ziel einer sorgfältigen Schaltungsauslegung immer in einer Minimierung der parasitären Induktivität liegen und damit in einer Reduzierung der dadurch entstehenden Durchbruchverluste.

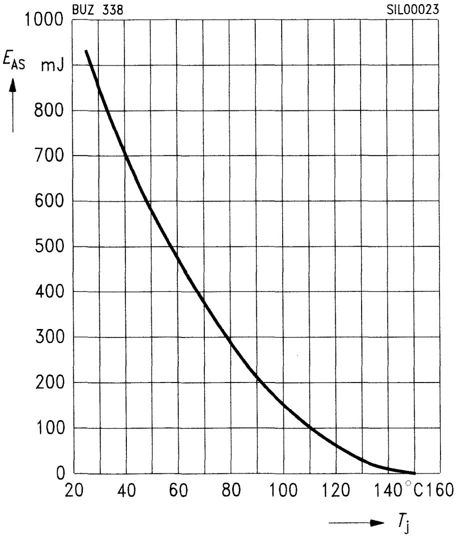
For this reason the objective of careful circuit design must always be a minimization of parasitic inductance, and consequently a reduction of the resulting breakdown losses.

Nutzen

- Keine Ausfälle durch transiente Überspannungen innerhalb der spezifizierten Daten.
- Die Beschaltung gegen Spannungsspitzen, verursacht durch Streuinduktivitäten, kann entfallen.
- Eine spannungsmäßige Überdimensionierung der Transistoren ist nicht notwendig.

Benefits

- No failures due to transient overvoltages within the specified ranges
- Protective circuitry against glitches caused by stray inductances is not required
- Overdimensioning of the transistors with respect to voltage is not necessary



Parameters:
$I_D = 13.5$ A
$R_{GS} = 25\ \Omega$
$V_{DD} = 50$ V
$L = 9.09$ mH

Bild 20
Avalanche Energie $E_{AS} = f(T_j)$
(Beispiel: BUZ 338)

Figure 20
Avalanche energy
$E_{AS} = f(T_j)$ (example: BUZ 338)

2.2 IGBT-Transistoren

Im wesentlichen ist der IGBT-Transistor ein modifizierter SIPMOS. Wie im **Bild 4** dargestellt, ist der MOSFET auf einem N^+N^--Substrat aufgebaut. Der IGBT (vgl. **Bild 21**) dagegen hat ein homogenes Substrat mit einem speziell ausgebildeten PN-Übergang auf der Rückseite. Dieser PN-Übergang bewirkt im eingeschalteten Zustand die Reduzierung der Durchlaßspannung durch Ladungsträgerinjektion.

2.2 IGBT Transistors

The IGBT is basically a modified SIPMOS transistor. As **Figure 4** shows, the MOSFET is designed as an n^+n^- substrate. An IGBT (cf. **Figure 21**), on the other hand, has a homogeneous substrate with a specially formed pn junction on the rear. This pn junction causes the conducting-state voltage to be reduced on account of charge-carrier injection at ON state.

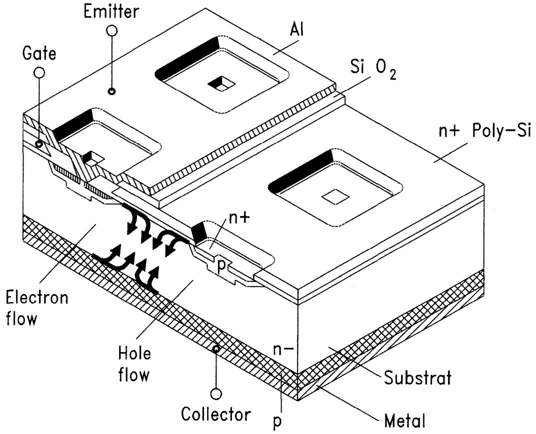


Bild 21
Aufbau eines N-Kanal-IGBT-Transistors

Figure 21
Design of an N channel IGBT transistor

Schaltverhalten

Das Schaltverhalten eines SIPMOS bzw. eines IGBT unterscheidet sich hauptsächlich durch den Spannungsabfall im eingeschalteten Zustand und durch den Tailstrom beim Abschalten des IGBT, wie dies im **Bild 22** dargestellt ist.

Switching response

The switching response of a SIPMOS differs from that of an IGBT mainly by the voltage drop at ON state and by what is called the tail current of an IGBT upon turn-off, as shown in **Figure 22**.

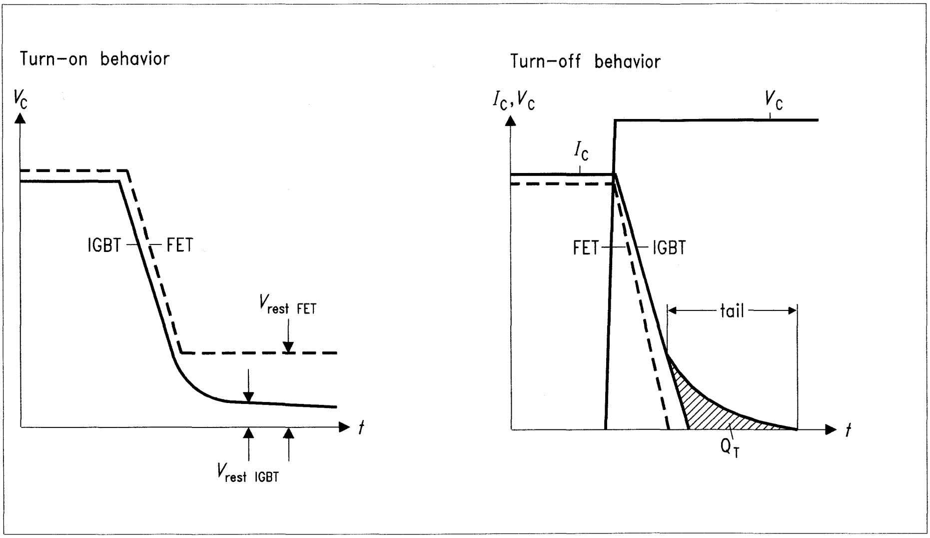


Bild 22
Typ. Schaltverhalten FET/IGBT

Figure 22
Typical FET/IGBT switching waveforms

In der Praxis müssen bei höheren Taktfrequenzen die Tailverluste berücksichtigt werden müssen. Das ist der Preis für die deutlich geringere Sättigungsspannung des IGBT gegenüber des MOSFET. Der Tailstrom ist nahezu temperaturunabhängig. Der Strom- und Spannungsverlauf verändern sich nicht mit der Temperatur.

In practical terms it means that tail losses have to be taken into account at higher switching frequencies. This is the price for the substantially smaller saturation voltage of an IGBT compared to a MOSFET. The tail current is virtually temperature-dependent. The current and voltage curves do not vary with temperature.

Kurzschlußfestigkeit

Beim Kurzschluß stellt sich der maximale Kollektorstrom durch die Transistorcharakteristik und die Steuerspannung ein. Die Steilheit des Transistors ist so vorgegeben, daß bei der vollen Steuerspannung (+15 V) der Kurzschluß im sicheren Bereich liegt. Der Transistor begrenzt den Kurzschlußstrom. Während der Kurzschlußzeit nimmt der Strom wegen der Erwärmung des IGBT ab.

Short-Circuit Strength

When a short-circuit occurs, the maximum collector current is determined by the transistor characteristic and the control voltage. The mutual admittance of the transistor is predefined in such a manner that the short-circuit is in the safe range at full control voltage g (+15 V). The transistor limits the short-circuit current. For the duration of the short-circuit, the current falls on account of the IGBT temperature rise.

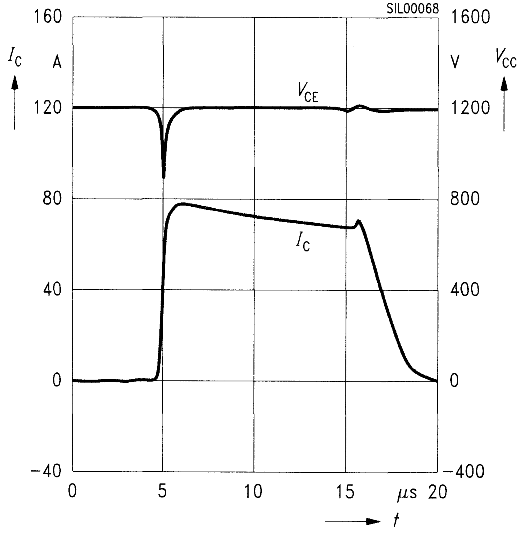


Bild 23
IGBT-Kurzschlußfestigkeit
(Beispiel: BUP 307)

Figure 23
IGBT-short-circuit strength
(Example: BUP 307)

Latch-up-Festigkeit

Wie das **Ersatzschaltbild 24** zeigt, bilden der PNP-Transistor und der parasitäre NPN-Transistor eine Thyristorstruktur. Bei hohem Strom und hoher Abschaltgeschwindigkeit (d*i*/d*t*) kann die Thyristorstruktur einrasten, der IGBT verliert seine Steuerbarkeit. Durch die beim Siemens IGBT gewählte Technologie wurde der Latch-up-Effekt eliminiert. Selbst bei Überstrom, Kurzschluß und extrem schnellem Schalten bleibt die Steuerbarkeit über den ganzen Temperaturbereich erhalten.

Latch-Up Strength

As shown in the equivalent circuit diagram (cf. **Figure 24**), the PNP transistor and the parasitic NPN transistor form a thyristor structure. The thyristor structure can latch up at high current and high turn-off rate (d*i*/d*t*), and the IGBT becomes uncontrollable. The technology selected for the Siemens IGBT has resulted in the latch-up effect being eliminated. Controllability is maintained over the whole temperature range even in the event of an overcurrent, a short-circuit or extremely rapid switching.

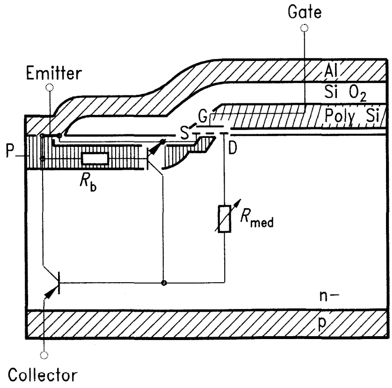


Bild 24
Schnittbild eines N-Kanal-IGBT mit dargestelltem Ersatzschaltbild

Figure 24
Sectional drawing of an N channel IGBT with equivalent circuit diagram

IGBT-Schaltverhalten

IGBT switching behaviour

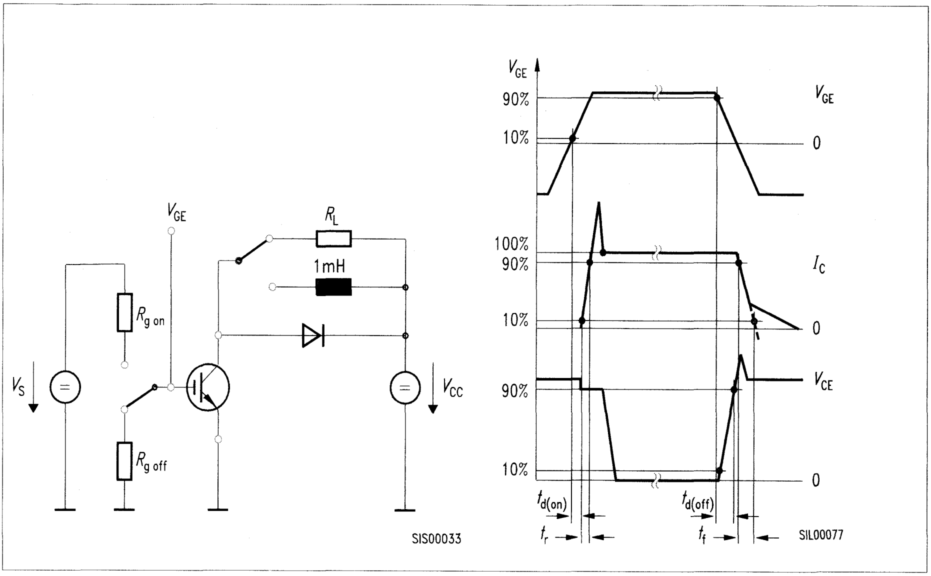


Bild 25
Schaltzeitmessung

Figure 25
Measurement of switching times

2.3 FRED-Dioden

Dieser Diodentyp wurde speziell für Anwendungen als Freilaufdiode in induktiven Lastkreisen mit superschnellen Schaltern entwickelt. Möglichst geringe Schalt- und Durchlaßverluste sowie ein sanftes Abschaltverhalten sind die besonderen Anforderungen die hier gestellt sind. Die den gewünschten Eigenschaften zugrunde liegenden Dioden-Parameter, wie Durchlaßspannung, Ladungsträgerlebensdauer und Sperrspannung, sind prinzipiell miteinander verknüpft. Für die Dioden-Herstellung werden Epitaxial-Sili-

2.3 FRED Diodes

This type of diode has been developed specifically for free-wheeling diode applications in inductive load circuits with super-high-speed switches. The particular specifications for these diodes were minimum dissipation and switching losses, combined with soft recovery. In principle, the diode parameters, such as forward voltage, carrier lifetime and reverse voltage, that are based on the desired characteristics are interlinked. They are manufactured from epitaxial silicon wafers. In this way a relatively thin ziumscheiben verwendet. Damit läßt sich ein vergleichweise dünnes Mittelgebiet mit gewünschtem Dotierungsprofil realisieren und die Diodenparameter können optimal für die Freilaufanwendungen abgestimmt werden. Nachfolgend werden die Begriffe, die das Kommutierungsverhalten einer Freilaufdiode charakterisieren, anhand einer Strom- und Spannungsfunktions-Darstellung während der Kommutierung bei Chopperbetrieb erläutert (vgl. **Bild 26**).

Speicherladung Q_{rr}

Die Speicherladung ist die Menge der gespeicherten Ladungsträger, die nach dem Nulldurchgang des abkommutierten Freilaufstroms aus der Diode in Sperrichtung abfließt. Die Ladung setzt sich zusammen aus der Nachlaufladung Q_S und der Restladung Q_F, die im wesentlichen die Schaltverluste der Diode erzeugen. Der Grad der Ladungsträgerspeicherung kann durch Einbau von Rekombinationszentren in die Diodenstruktur eingestellt werden, wobei berücksichtigt werden muß, daß ein Vermindern der Speicherladung, d.h. ein Reduzieren der Ladungsträger-Lebensdauer mit einer Erhöhung der Durchlaßverluste verbunden ist. Die im Betriebsfall aus einer Freilaufdiode jeweils abzuführende Speicherladung steigt mit der Höhe von Durchlaßstrom I_F, Strom-Abkommutierungssteilheit (di_F/dt) Junction-Temperatur T_j und Betriebsspannung V_B.

central region can be created with the desired doping profile, and optimum tuning of the diode parameters for free-wheeling diode applications is possible. An explanation is given below of the terms that characterize the commutation behaviour of a free-wheeling diode using a functional representation of current and voltage during commutation in chopper operation (cf. **Figure 26**).

Reverse Recovery Q_{rr}

The reverse recovery charge is the quantity of stored charge carriers that is discharged from the diode in the reverse direction after the switched-off free-wheeling current passes through zero. The charge comprises the lag charge Q_S and the residual charge Q_F which essentially generate the switching losses of the diode. The degree of carrier storage may be set by including recombination centers in the diode structure; it must be remembered that a reduction of the reverse recovery charge, i.e. a reduction of carrier lifetime, is associated with a rise in dissipation. The reverse recovery charge that has to be bled off a free-wheeling diode in operation rises with the magnitude of the forward current I_F, the rate of current decay upon switch-off commutating di_F/dt, the junction temperature T_j and the operating voltage V_B.

$$Q_{rr} = Q_s + Q_F = \int i_R \, dt$$

Kommutierungsverhalten

Commutations behaviour

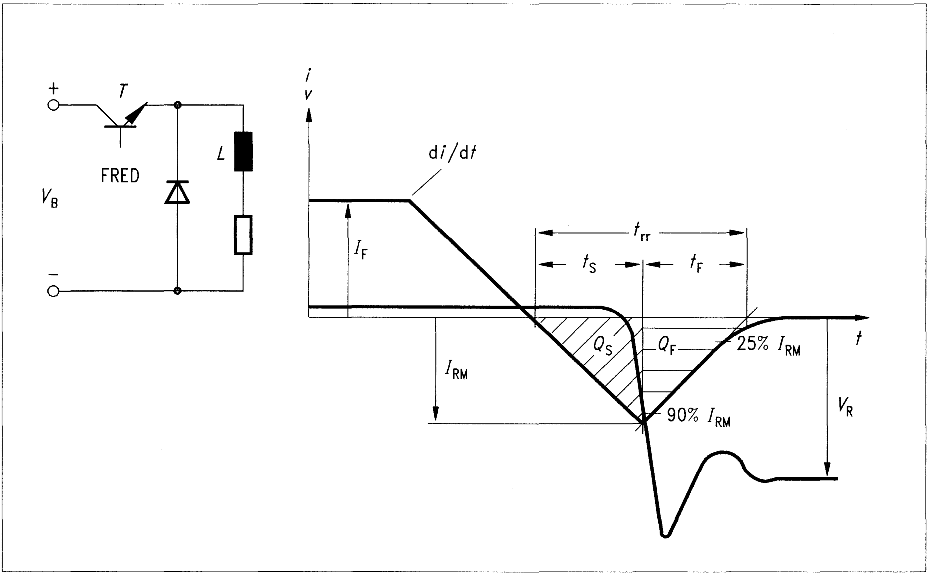


Bild 26
Chopper-Betrieb
Diodenstrom- und Spannungsfunktion während der Kommutierung

Schaltverluste

Die Schaltverluste entstehen im wesentlichen durch den Übergang der Diode von dem Leitendzustand in den Sperrzustand während des Kommutierungsvorganges. Sie ergeben sich aus dem Produkt der Transienten von Rückstrom und Rückwärtsspannung. Damit werden diese Schaltverluste hauptsächlich von der Restladung Q_F und der in diesem Zeitabschnitt an der Diode anliegenden Spannung bestimmt. Diese Spannung ist wiederum eine Funktion der Abfallsteilheit des Rückstromes.

Figure 26
Chopper operation
Functional representation of current and voltage during commutation

Switching Losses

Switching losses are caused essentially by the transition of the diode from the forward-biased to the blocking state during the commutation process. They result from the product of the reverse-current and reverse-voltage transients. These switching losses are therefore determined primarily by the residual charge Q_F and the voltage applied during this period across the diode. This function is again a function of the rate of reverse-current decay.

S-Faktor

Der S-Faktor ergibt sich aus dem Zeitverhältnis der aus einer Diode abfließenden Rest und Nachlaufladung: $S = t_f / t_s$. Der S-Faktor liefert damit ein Kriterium zur Beurteilung des Sperrerhol- bzw. Abschaltverhalten von schnellen Dioden. Je größer der S-Faktor ist, desto sanfter verläuft der Abschaltvorgang. Gängige Werte für S liegen zwischen 0,6 und 1,2. Wegen der Abhängigkeit von den Betriebsverhältnissen der Diode muß der S-Faktor durch die Angaben von I_F , $-di_F/dt$, V_B und Junktiontemperatur definiert werden.

Abkommutierungssteilheit $-di_F/dt$

Die Steilheit kann durch die Einschaltzeit des Schalters T (vgl. **Bild 31**) bestimmt werden oder sie ergibt sich aus der Kreis-Induktivität, sofern deren Zeitkonstante größer ist als die Einschaltzeit von T.

Sperrerholverhalten

Nach Ausräumen der Nachlaufladung Q_s beginnt die Diode Sperrspannung aufzunehmen. Der Dioden-Rückstrom erreicht den Scheitelwert I_{RM}. Mit der abfließenden Restladung fällt der Rückstrom in einer gewissen Steilheit ab. Eine zu geringe Restladung führt zum Rückstromabriß (snap off), der in Verbindung mit einer parasitären Kreis-Induktivität eine hohe Überspannung erzeugt. Ohne entsprechende Beschaltung kann dadurch die Diode zerstört werden; außerdem entstehen unerwünschte Störfelder. Die Dioden-Struktur muß deshalb so gestaltet

S Factor

The S factor results from the time ratio of the residual and lag charges draining off a diode, $S = t_f / t_s$. The S factor thus provides a criterion for assessing the reverse recovery and recovery responses of fast-recovery diodes. The higher the S factor, the softer will be the recovery process. Common values of S are 0.6 to 1.2. Owing to the dependence on operating conditions of the diode, the S factor has to be defined by specifying I_F , $-di_F/dt$, V_B and the junction temperature.

Rate of Current Decay upon Switch-Off $-di_F/dt$

The rate may be determined by the turn-on time of the switch T (cf. **Figure 31**) or results from the circuit inductance, provided that the time constant of the latter is greater than the turn-on time of T.

Reverse Recovery Response

After ridding itself of the lag charge Q_S, the diode begins consuming reverse voltage. The diode reverse current attains its peak value I_{RM}. With the residual charge being discharged, the reverse current falls at a certain rate. If the residual charge is too low, the reverse current will snap off, causing a high overvoltage in conjunction with a parasitic circuit inductance. It may destroy the diode if suitable circuitry is not present; in addition, spurious interference fields may be generated. The diode structure must therefore be designed in such a manner that the ratio sein, daß das Verhältnis von Nachlauf- und Restladung einen mäßigen Rückstromabfall gewährleistet. Besonders sanftes Abschalten ergibt sich, wenn der Rückstrom mit einem leichten Tail abklingt. Mit steigender Betriebsspannung wird der Rückstromabfall steiler.

Sperrverzögerungszeit t_{rr}

Ihre Definition ist aus der Abbildung der Dioden-Stromfunktion beim Kommutierungsvorgang zu ersehen. Während dieser dynamische Parameter das Schaltverhalten von schnellen Dioden für HF-Gleichrichtung und Signalübertragung gut charakterisiert, kann daraus für schnelle Freilaufdioden kein eindeutiges Beurteilungskriterium abgeleitet werden. Speicherladung und S-Faktor sind für die Kennzeichnung der Dioden-Funktion im Freilaufbetrieb wesentlich aussagekräftiger.

3 Wärmewiderstände

Zum Erzielen besserer Wärmeableitungen können die Leistungstransistoren auf Kühlbleche oder Kühlkörper bzw. Kühlprofile montiert werden. Bei Kühlkörper und -profilen wird der Wärmewiderstand vom Zubehörlieferanten angegeben.

Der Gesamt-Wärmewiderstand ist vom Chip über das Kühlmedium zur Umgebung anzusetzen.

of lag to residual charge ensures a moderate decrease in reverse current. Extremely soft recovery results if the reverse current decays with a slight tail. The decrease in reverse current becomes greater with rising operating voltage.

Reverse Recovery Time t_{rr}

Its definition can be seen from the representation of the diode current function during the commutation process. While this dynamic parameter properly characterizes the switching response of fast-recovery diodes for RF rectification and signal transmission, no unambiguous criterion may be deduced from it for fast-recovery free-wheeling diodes. Reverse recovery charge and S factor are far more significant for identifying the diode function in free-wheeling operation.

3 Thermal Resistance

Power transistors can be mounted on cooling plates or heat sinks or shaped heat dissipators to improve heat dissipation. In the case of heat sinks and shaped heat dissipators the thermal resistance is specified by the supplier.

The total thermal resistance has to be expelled from the chip via the cooling medium to the ambient air.

Es gilt generell die Bestimmungsgleichung:

The following defining equation generally applies:

$$R_{\mathrm{thJA}} = R_{\mathrm{thJC}} + R_{\mathrm{thCH}} + R_{\mathrm{thHA}}$$

Da die Berührungsoberflächen des Transistors (Drain-, bzw. Kollektoranschluß) und des Kühlbleches nicht vollkommen plan sind, muß ein sog. Übergangswiderstand R_{thCH} berücksichtigt werden, der ohne Isolierscheibe bis zu 1 K/W betragen kann. Durch Wärmeleitpasten oder -scheiben kann dieser Widerstand, je nach Gehäuseart, Chipfläche und Kühlblechbeschaffenheit, auf ca. 0,3 bis 0,5 K/W reduziert werden.

Der Wärmewiderstand des Kühlbleches R_{thHA} wird nach folgender Näherungsformel berechnet (nicht gültig für Kühlkörper):

Since the contacting surfaces of the transistor (drain and collector connections) and of the cooling plate are not completely plane, a "junction resistance" R_{thCH} has to be taken into account which may be as high as 1 K/W without an insulating washer. Depending on the type of case, the chip area and the structure of the cooling plate, this resistance may be reduced to about 0.3 to 0.5 K/W by using thermally conductive pastes or washers.

The thermal resistance of the cooling plate R_{thHA} is calculated in accordance with the following approximation formula (not applicable to heat sinks):

$$R_{\mathrm{thHA}} = \frac{3{,}3}{\sqrt{\lambda \times d}} \times C^{0.25} + 650C/A$$

d = Dicke des Kühlbleches in mm
A = Oberfläche des Kühlbleches in cm^2
C = Korrekturfaktor für Lage und Oberflächenbeschaffenheit des Kühlbleches
λ = Wärmeleitwert des Kühlbleches

d = thickness of the coolinplate in mm
A = area of the cooling plate in cm^2
C = correction factor for the position and surface finish of the cooling plate
λ = thermal conductance of the cooling plate material

Kühlblech-Wärmeleitwert λ **Cooling Sheet Thermal Conductance**		**Korrekturfaktor-Tabelle C** **Correction Factor Table C**		
Material **Material**	**Wärmeleitwert** **Thermal conductance**	**Lage** **Position**	**Oberfläche blank** **Surface bare**	**geschwärzt** **black**
Aluminium Aluminium	2,1 W/K cm 2.1 W/K cm	senkrecht vertical	0,85 0.85	0,43 0.43
Kupfer Copper	3,8 W/K cm 3.8 W/K cm	waagerecht horizontal	1 1	0,5 0.5
Messing Brass	1,1 W/K cm 1.1 W/K cm			
Stahl Steel	0,46 W/K cm 0.46 W/K cm			

Die Formel gilt für angenähert quadratisch geformte Kühlbleche, wenn der Transistor in der Mitte montiert ist und die einzige Wärmequelle auf dem Kühlblech darstellt. Die Werte der Konstanten und des Korrekturfaktors gelten in ruhender Luft bis zu einer Umgebungstemperatur von etwa 45 °C, sofern keine heißen, wärmestrahlenden Teile in der Nähe sind.

The formula applies to approximately square-shaped cooling plates when the transistor is mounted at the center and is the sole source of heat on the cooling plate. The values of the constants and of the correction factor apply to still air up to an ambient temperature of approximately 45 °C, provided no hot, heat-radiating parts are nearby.

Wärmeübergangswiderstand R_{thCH} einer Glimmerscheibe

Heat-Transfer Resistance R_{thCH} of a Mica Washer

Gehäuse **Package**	**Dicke der Scheibe trocken** **Thickness of dry washer**		**Kontaktfett,** beidseitig aufgetragen, reduziert den Wärmewiderstandswert um: **Contact grease** applied on both sides reduces thermal resistance by:
	50 µm	**75 µm**	
TO-220 (TO3)	1.25 K/W	1.5 K/W	1.8 K/W
TO-218 (TOP3)	1.4 K/W	1.8 K/W	0.7 K/W
TO-220	1.5 K/W	1.2 K/W	0.7 K/W

Isolierende Wärmeleitscheiben ergeben bessere Wärmeübergangswiderstände als Glimmerscheiben.

Temperaturmeßmethoden der Bauelementanschlüsse

- **Messen mit Thermoelement**
  Das Messen erfolgt mittels Miniatur-Mantel-Thermoelement mit niedriger Wärmekapazität. Das Thermoelement ist mit Wärmeleitpaste überzogen und wird gegen den Kollektoranschluß gedrückt. Der Einfluß des Meßobjektes ist äußerst gering, und der Meßfehler beträgt nur wenige Prozent.
- **Messen mit Temperaturindikatoren (z.B. Thermopapier)**
  Beim Messen mit Temperaturindikatoren kann die Temperatur ohne zusätzliche Wärmeableitung und somit fast fehlerfrei bestimmt werden. Der entsprechende Fehler ist praktisch nur durch die Abstufung und der Toleranz der Temperaturin-

Insulating heat-conducting washers produce better heat-transfer resistance values than mica washers.

Temperature Measuring Methods of Device Connections

- **Measuring with a thermocouple**
  Measurements are made with a miniature clad thermocouple of low thermal capacity. The thermocouple is coated with a thermally conductive paste and pressed against the collector connection. The influence of the device under test is extremely slight, and the measuring error is only a few percent.
- **Measuring with temperature indicators (e.g. temperature-sensitive paper)**
  When temperature indicators are used for measuring purposes, the temperature can be determined without additional heat dissipation and thus virtually without error. The associated error is due nearly entirely to the gradation and the tolerance of the

dikatoren gegeben. Diese Methode ist einfach durchzuführen und dabei ausreichend genau. Sie eignet sich besonders für Messungen auf Platinen.

4 Verarbeitungsrichtlinien

- Die maximal zulässigen Gate-Source-Spannungen sind:

  – MOS-Logik-Leveltransistoren: ± 10 V
  – MOS-Standard-Transistoren: ± 20 V

  Ein Überschreiten dieser V_{GS}-Spannungen kann die Transistorparameter verändern. Das heißt jedoch nicht, daß bei diesen Spannungen die Durchbruchfeldstärke und damit die Zerstörgrenze erreicht ist, sondern das sind die Grenzen, bei denen die Langzeitstabilität durch Freigabetests abgesichert ist. Bei der 100-%-Bauteil-Parameterprüfung werden die Transistoren zwischen den Gate-Source-Anschlüssen mit einer wesentlich höheren Spannung kurzzeitig belastet, um die Gateoxid-Qualität zu testen.

- Beim Schaltungsaufbau ist darauf zu achten, daß der Transistor nicht mit offenen Gate-Source-Anschlüssen betrieben oder gemessen wird.

- Thermische Beanspruchung
  Jeder Halbleiter ist empfindlich gegen Überschreiten der höchstzulässigen Sperrschichttemperatur. Bei der Konstruktion der Geräte ist deshalb zu beachten, daß der Halbleiter nicht von anderen Wärmeerzeugern aufgeheizt wird.

temperature indicators. This method is simple to implement, and sufficiently accurate at the same. It is particularly suitable for measurements on printed circuit boards.

4 Mounting Instructions

- The maximum permissible gate-source voltages are:

  – MOS logic level transistors: ± 10 V
  – MOS standard transistors : ± 20 V

  Values above these V_{GS} voltages can change transistor parameters. But this does not mean that the breakdown field strength, and thus the limit with regard to destruction, are reached at these voltages, but these are the limits at which long-term stability is assured by approval testing. In the 100 % device parameter test transistors are briefly stressed across the gate-source connections with a considerably higher voltage in order to test the quality of the gate oxide.

- Make sure, when designing a circuit, that the transistor is not operated or measured with open gate-source connections.

- Thermal stressing
  Every semiconductor device is sensitive to the maximum permissible junction temperature being exceeded. Care should therefore be taken at the equipment design stage to ensure that the semiconductor device is not heated by other heat-generating components.

5 MOS-Handhabung

Elektrostatisch **g**efährdetes **B**auelement (EGB)

SIPMOS-Halbleiter sind elektrostatisch gefährdete Bauelemente, bei deren Handhabung besondere Maßnahmen zu erfüllen sind: Unkontrollierte Ladungen und Spannungen von nicht geerdeten Geräten oder Personen, Entladung statischer Elektrizität oder ähnliche Einflüsse können das Bauelement zerstören. Empfindlich ist beim MOSFET die Gate-Source-Strecke, da diese eine sehr dünne (kleiner als 100 nm) Silizium-Dioxid-Schicht (Glas) darstellt.

Ein Maß für die Empfindlichkeit der Transistoren gegen elektrostatische Entladung **ESD** = **E**lectro**s**tatic **D**ischarge, ist die Gate-Source-Kapazität C_{GS} bzw. die Eingangskapazität C_{iss}.

Bauelemente mit größerer Eingangskapazität sind unempfindlicher. Das bedeutet, daß Transistoren mit großen Chipflächen bzw. großen Eingangskapazitäten im Sinne der MIL-STD 883C, Methode 3015.6 (Prüfmethode nach dem Human Body Model) bereits als weniger empfindlich oder robust gelten.

SIPMOS-Halbleiter haben im Vergleich zu HF-MOSFET größere Eingangskapazitäten und sind damit unempfindlicher, trotzdem sind die entsprechenden Handhabungs-Richtlinien für elektrostatisch gefährdete Bauelemente zu beachten.

Um die Transistoren während des Transports vor statischer Aufladung zu schützen, werden sie in antistatischer Verpak-

5 MOS Handling

Electro**s**tatic-**s**ensitive (ESD) **d**evices

SIPMOS semiconductors are electrostatic-sensitive devices requiring special handling techniques. Uncontrolled charges and voltages from ungrounded equipment and persons, as well as the discharging of static electricity or similar influences can destroy these devices. The sensitive part of a MOSFET is the gate-source junction, a very thin (< 100 nm) silicon dioxide film (glass).

A criterion for the sensitivity of transistors to **e**lectro**s**tatic **d**ischarge (ESD) is the gate-source capacitance C_{GS} and the input capacitance C_{iss}.

Devices having a higher input capacitance are less sensitive. This means that transistors having large chip areas and high input capacitances as defined in MIL-STD 883C, Method 3015.6 (Human Body Model Test Method), are already regarded as less sensitive or robust.

Compared to RF MOSFETs, SIPMOS semiconductors have higher input capacitances and are therefore less sensitive; nevertheless, the corresponding handling instructions for electrostatic-sensitive devices must be observed.

To protect transistors from static charges during shipping, they are supplied in antistatic packing. When inserting transiskung geliefert. Beim Einbau der Transistoren sind die Vorschriften für MOS-Bauelemente zu beachten.

tors, follow the instructions for MOS devices.

Verpackungsaufkleber für SIPMOS-Halbleiter

Packing sticker for SIPMOS semiconductors

Achtung
Nur geschultes Personal
darf die Verpackung öffnen
Elektrostatisch gefährdete
Bauelemente (EGB)
Attention
Observe Precautions for Handling
Electrostatic Sensitive
Devices

Normen

- SIEMENS QS-Verfahrensanweisung und MIL-STD 883C, Methode 3015.6 für Prüfung und Klassifizierung
- SIEMENS Norm SN 73257 für Grundlagen, Test und sichere Handhabung
- DIN VDE 0843 T2 identisch mit IEC 801-2
- CECC - Grundspezifikation CECC 00015

Standards

- Siemens QA Process Instructions and MIL-STD 883C, Method 3015.6 for Testing and Classification.
- Siemens Standard SN 73257 for Principles, Testing and Safe Handling.
- DIN VDE 0843 T2, identical with IEC 801-2.
- CECC Basic Specification CECC 00015.

Wichtige Punkte für die Handhabung

- Bis zur Verarbeitung müssen die Bauelemente in einer EGB-gerechten Verpackung bleiben.
- Eingangsprüfung und Weiterverarbeitung nur an speziell eingerichteten Arbeitsplätzen (hochohmige Masseverbindung, leitende Ablage, Handgelenkband etc.).

Important Points on Handling

- Until they are processed, the devices must be kept in suitable ESD device packing.
- Incoming inspections and subsequent processing may be performed only at specially equipped workstations (high-impedance ground connection, conductive working top, wrist strap, etc.).

- Alle Transporteinheiten und Leiterplatten müssen vor der Verarbeitung von EGB-Bauteilen auf gleiches Potential gebracht werden.

Empfindlichkeit nach MIL-STD-883

- **H**uman **B**ody **M**odel
  HBM ist ein Modell, das den menschlichen Körper durch einen aufladbaren Kondensator mit einem Entladewiderstand simuliert.

- All transport devices and printed circuit boards must be brought to the same potential before ESD devices are processed.

Sensitivity as per MIL-STD 883

- **H**uman **B**ody **M**odel
  HBM is a model for simulating the human body by a chargeable capacitor with a bleeder resistor.

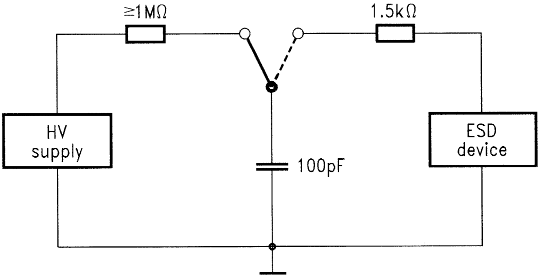


Bild 27
Testschaltung

Figure 27
Test circuit

- Empfindlichkeitsklassen nach MIL-STD-883 und SIEMENS QS-Verfahrensanweisung

- Sensitivity classes as per MIL-STD 883 and Siemens QA Process Instructions

Klasse **Class**	**Prüfspannung** Zerstörung bei: **Test Voltage** Destroys at:	**Bezeichnung** **Description**
1a	0 ... 499 V	extrem empfindlich extremely sensitive
1b	500 ... 999 V	sehr empfindlich very sensitive
1c	1000 ... 1999 V	empfindlich sensitive
2	2000 ... 3999 V	weniger empfindlich less sensitive
3	≥ 4000 V	robust robust

Die Klassen 1, 2 und 3 entsprechen MIL-STD-883, die Unterklassen 1a, 1b und 1c sind von SIEMENS eingeführt worden.

Classes 1, 2 and 3 correspond to MIL-STD 883; sub-classes 1a, 1b and 1c have been introduced by SIEMENS.

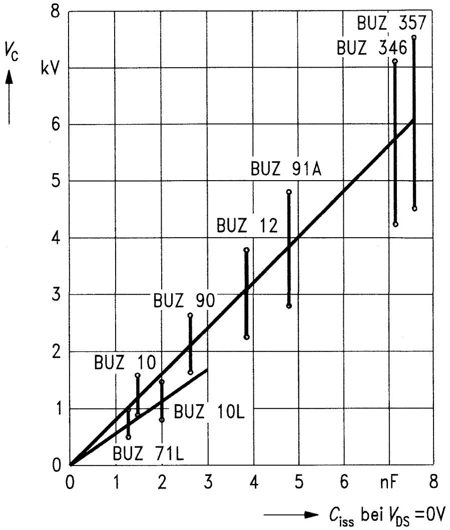


Bild 28
Empfindlichkeit von SIPMOS-Leistungstransistoren

Figure 28
Sensivity of SIPMOS Power Transistors

1 Symbole, Begriffe, Normen

Symbole und Begriffe der verwendeten Größen

1 Symbols, Terms, Standards

Symbols and Terms of Magnitudes Used

Symbole Symbols	**Begriffe**	**Terms**
A	Anode	Anode
C	Kapazität; Kollektor	Capacitance, collector
C_{ISS}	Eingangskapazität	Input capacitance
C_{OSS}	Ausgangskapazität	Output capacitance
C_{rss}	Rückwirkungskapazität	Reverse transfer capacitance
C_{DS}	Drain-Source Kapazität	Drain-source capacitance
C_{GD}	Gate-Drain Kapazität	Gate-drain capacitance
C_{GS}	Gate-Source Kapazität	Gate-source capacitance
C_{Mi}	Millerkapazität	Miller capacitance
D	Tastverhältnis/Tastgrad $D = t_p/T$; Drain	Pulse duty factor/duty cycle $D = t_p/T$; drain
$d_{iF/dt}$	Dioden-Stromsteilheit	Rate of diode current rise
E	Energie	Energy
E_A	Avalanche-Energie	Avalanche energy
E_{AR}	Avalanche-Energie, periodisch	Avalanche energy, repetitive
E_{AS}	Avalanche-Energie, Einzelpuls	Avalanche energy, single pulse
E_{off}	Abschaltverlust-Energie	Turn-off loss energy
f	Frequenz	Frequency
G	Gate	Gate
g_{fs}	Übertragungssteilheit	Transconductance
I	Strom	Current
i	Strom Augenblickswert	Current, instantaneous value
I_{AR}	Avalanche-Strom, periodisch	Avalanche current, repetitive
I_C	Kollektor-Gleichstrom	DC collector current
I_{CES}	Kollektor-Reststrom	Collector cutoff current

Symbole Symbols	Begriffe	Terms
I_{Cpuls}	Kollektor-Gleichstrom, gepulst	DC collector current, pulsed
I_{D}	Drain-Gleichstrom	DC drain current
I_{Dpulse}	Drain-Gleichstrom, gepulst	DC drain current, pulsed
I_{DSS}	Drain-Reststrom	Drain cutoff current
I_{DSV}	Drain-Reststrom mit anliegender Gate-Spannung	Drain cutoff current with gate voltage applied
I_{F}	Dioden Durchlaßstrom (allgemein)	Diode forward current (general)
I_{FAV}	Dioden Durchlaßstrom , Mittelwert	Diode forward current, average value
I_{FRMS}	Dioden Durchlaßstrom , Effektivwert	Diode forward current, rms value
I_{FRM}	Periodischer Dioden-Spitzenstrom	Repetitive diode peak current
I_{FSM}	Dioden-Stoßstromscheitelwert (50Hz-Sinus)	Diode current surge crest value (50-Hz sinusoidal)
I_{GES}	Gate-Emitter-Leckstrom	Gate-emitter leakage current
I_{GSS}	Gate-Source-Leckstrom	Gate-source leakage current
I_{L}	Strom durch Induktivität	Current through inductance
I_{R}	Dioden-Sperrstrom	Diode reverse current
I_{RRM}	Sperrverzögerungsrückstromspitze	Reverse recovery peak return current
I_{S}	Inversdioden-Dauergleichstrom	Inverse diode continuous forward current
I_{SM}	Inversdioden-Gleichstrom, gepulst	Inverse diode direct current, pulsed
K	Kathode	Cathode
L	Induktivität	Inductance
L_{L}	Last-Induktivität	Load inductance
L_{p}	Parasitäre Induktivität (z.B. Leitungen)	Parasitic inductance (e.g. lines)
P_{A}	Avalanche-Verlustleistung	Avalanche power loss

Symbole Symbols	Begriffe	Terms
P_F	Dioden-Verlustleistung, Durchlaßverlustleistung	Diode power loss, forward power loss
P_{sw}	Schaltverlustleistung	Switching power loss
P_{tot}	Gesamtverlustleistung	Power dissipation
Q_{Gate}	Gate-Ladung	Gate charge
Q_{GS}	Ladung der Gate-Source-Kapazität	Charge of gate-source capacitance
Q_{GD}	Ladung der Gate-Drain-Kapazität	Charge of gate-drain capacitance
$Q_{Gate\ tot}$	Gesamt-Gateladung	Total gate charge
Q_{rr}	Sperrverzögerungsladung	Recovered charge
R_b	Basis-Emitter-Widerstand des parasitären Bipolartransistors	Base-emitter resistance of parasitic bipolar transistor
R_D	Drainwiderstand (Widerstand der Epitaxieschicht)	Drain resistance (resistance of epitaxial layer)
$R_{DS(on)}$	Drain-Source-Einschaltwiderstand	Drain-source ON resistance
R_G	Gate-Bahnwiderstand	Gate bulk resistance
R_{GS}	Gate-Source-Widerstand	Gate-source resistance
R_i	Innenwiderstand (Pulsgenerator)	Internal resistance (pulse generator)
R_K	Kanalwiderstand	Channel resistance
R_L	Lastwiderstand	Load resistance
R_{thCH}	Wärmewiderstand, Gehäuse-Kühlkörper	Thermal resistance, case to heat sink
R_{thHA}	Wärmewiderstand, Kühlkörper-Umgebung	Thermal resistance, heat sink to ambient air
R_{thJA}	Wärmewiderstand, Chip-Umgebung	Thermal resistance, chip to ambient air
R_{thJC}	Wärmewiderstand, Chip-Gehäuse	Thermal resistance, chip to case
S	Source	Source
T	Periodendauer; Temperatur	Cycle time; temperature
T_A	Umgebungstemperatur	Ambient temperature
T_C	Gehäusetemperatur	Case temperature

Symbole Symbols	Begriffe	Terms
t	Zeit allgemein	Time, general
t_1	Zeitpunkt	Instant
t_{doff}	Ausschaltverzögerungszeit	Turn-off delay time
t_{don}	Einschaltverzögerungszeit	Turn-on delay time
t_{f}, t_{F}	Fallzeit	Fall time
t_{p}	Pulsdauer bzw. Einschaltdauer	Pulse duration or turn-on time
T_{j}	Chip- bzw. Betriebstemperatur	Chip or operating temperature
$T_{\mathrm{j(max)}}$	Maximal zulässige Chip- bzw. Betriebstemperatur	Maximum permissible chip or operating temperature
$t_{\mathrm{d(off)}}$	Ausschaltzeit	Turn-off time
$t_{\mathrm{d(on)}}$	Einschaltzeit	Turn-on time
t_{p}	Pulszeit	Pulse time
t_{r}	Anstiegszeit	Rise time
t_{rr}	Sperrverzögerungszeit	Reverse recovery time
T_{stg}	Lagertemperatur	Storage temperature
T_{sold}	Löttemperatur	Soldering temperature
V	Spannung Augenblickswert	Voltage, instantaneous value
V_{in}	Ansteuerspannung	Drive voltage
$V_{\mathrm{(BR)CES}}$	Kollektor-Emitter-Durchbruchspannung	Collector-emitter breakdown voltage
$V_{\mathrm{(BR)DSS}}$	Drain-Source-Durchbruchspannung	Drain-source breakdown voltage
V_{DD}	Versorgungsspannung	Supply voltage
V_{CE}	Kollektor-Emitter-Spannung	Collector-emitter voltage
V_{CEsat}	Kollektor-Emitter-Sättigungsspannung	Collector-emitter saturation voltage
V_{CGR}	Kollektor-Gate-Spannung	Collector-gate voltage
V_{DGR}	Drain-Gate-Spannung	Drain-gate voltage
V_{DS}	Drain-Source-Spannung	Drain-source voltage
V_{F}	Dioden-Durchlaßspannung	Diode forward voltage

Symbole Symbols	Begriffe	Terms
V_{GE}	Gate-Emitter-Spannung	Gate-emitter voltage
$V_{GE(th)}$	Gate-Schwellenspannung (IGBT)	Gate threshold voltage (IGBT)
V_{GS}	Gate-Source-Spannung	Gate-source voltage
$V_{GS(th)}$	Gate-Schwellenspannung (SIPMOS)	Gate threshold voltage (SIPMOS)
V_R	Dioden-Sperrspannung	Diode reverse voltage
V_{RRM}	Periodische Spitzensperrspannung	Repetitive peak reverse voltage
V_{RSM}	Stoßspitzensperrspannung	Surge peak reverse voltage
V_{SD}	Inversdioden-Durchlaßspannung	Inverse diode forward voltage
Z_{thJC}	Transienter Wärmewiderstand, Chip-Gehäuse	Transient thermal resistance, chip to case

Normen

Folgende Normen wurden in diesem Datenbuch verwendet. Spezielle Einzelheiten können nachfolgenden Unterlagen entnommen werden:

Standards

The following standards were used for this Data Book. Specific details can be taken from the documents listed below:

Normen, Begriffe und Definitionen
Standards, Terms and Definitions

DIN 40 900 T5	Halbleiter, Schaltzeichen	Semiconductors, Graphical Symbols
DIN 41 781	Diodenbegriffe	Diode Terms and Definitions
DIN 41 785 T3	Leistungshalbleiter, Kurzzeichen	Power Semiconductors, Letter Symbols
DIN 41 854	Bipolare Transistoren, Begriffe	Bipolar Transistors, Terms and Definitions
DIN 41 858	Feldeffekttransistoren, Begriffe	Field Effect Transistors, Terms and Definitions
IEC 148 B	Halbleiterbauelemente, Symbole allgemein	Semiconductor Devices, Symbols, General

Angaben in Datenblättern, Meßverfahren
Details in Data Sheets, Test Procedures

DIN 41 791	T1	Allgemeines zu Datenblättern	General Remarks on Data Sheet Details
	T5	Datenblattangaben, Leistungstransistoren	Data Sheet Details, Power Transistors
	T6	Datenblattangaben, Schalttransistoren	Data Sheet Details, Switching Transistors
DIN 41 792	T1	Meßverfahren, Transistoren	Test Procedures, Transistors
	T2	Meßverfahren, Dioden	Test Procedures, Diodes
	T3	Meßverfahren, Wärmewiderstand	Test Procedures, Thermal Resistance
DIN IEC 747	T1	Allgemeines zu Grenz- und Kenndaten, Meßverfahren	General Remarks on Maximum Ratings and Characteristics, Test Procedures
	T2	Dioden	Diodes
IEC 747	T7	Bipolare Schalttransistoren	Bipolar Switching Transistors
DIN IEC 747	T8	Feldeffekttransistoren	Field Effect Transistors

Zuverlässigkeit
Reliability

DIN 41 794 T3 T8	Transistoren Dioden	Transistors Diodes
DIN IEC 68 ..	Tests	Tests
MIL-STD 883C	Testmethoden, z.B. Methode 3015.6 für ESD [1]	Test Methods, e.g. Method 3015.6 for ESD [1]
MIL-STD 19500	Ausfallkriterien	Failure Criteria
SN 73 257	ESD	ESD
A66762-A4013-A58	Verfahrensanweisung für ESD	QA Process Instructions for ESD

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[1] **ESD** ≙ **E**lectro**s**tatic **d**ischarge / Elektrostatische Entladung

1.1 Anordnung des Indizes

Spannungen

Es werden zwei Indizes verwendet, die die Punkte bezeichnen, zwischen denen die Spannung gemessen wird. Positiven Zahlenwerten der Spannungen entsprechen positive Potentiale des mit dem ersten Index bezeichneten Punkt (Bezugspunkt), z.B. V_{GS}.

Ströme

Mindestens ein Index wird verwendet. Positiven Zahlenwerten des Stroms entsprechen positive Ströme, die an dem mit dem ersten Index bezeichneten Anschluß in das Bauelement eintreten, z.B. I_{GS}.

Ein zusätzlicher 3. Index gibt den Beschaltungszustand zwischen dem 2. Index und dem nicht bezeichneten 3. Anschluß an.

Beispiele

$V_{(BR)DSS}$ = Durchbruchspannung zwischen Drain- und Sourceanschluß mit kurzgeschlossenem Gate-Source-Anschluß.

I_{DSV} = Strom in Drain-Source-Richtung mit Spannungsbeschaltung zwischen Gate-Source-Anschluß.

3. Buchstabe
S = kurzgeschlossen
R = Widerstandsbeschaltung
V = Spannungsbeschaltung
X = Widerstands- und Spannungsbeschaltung

1.1 Arrangement of Subscripts

Voltages

Two subscripts are used to designate the points between which the voltage is measured. Positive numerical values of the voltages equate to positive potentials of the point specified by the first subscript (reference point), e.g. V_{GS}.

Currents

At least one subscript is used. Positive numerical values of the current equate to positive currents entering the component at the connection specified by the first subscript, e.g. I_{GS}.

An additional, third subscript indicates the circuit status between the second subscript and the unspecified third connection.

Examples

$V_{(BR)DSS}$ = Breakdown voltage between drain and source connections with shorted gate-source connection.

I_{DSV} = Current in drain-source direction with voltage connected across the gate-source connection.

Third letter
S = Shorted
R = Resistive connection
V = Voltage connection
X = Resistive and voltage connection

2 Grenzwerte

Die in den Datenblättern angegebenen Grenzwerte sind absolute Werte. Wird einer dieser Grenzwerte überschritten, so kann das zur Zerstörung des Halbleiters führen, auch wenn nicht alle anderen Grenzwerte ausgenutzt werden. Wenn nicht anders angegeben, gelten die Werte bei einer Temperatur von 25 °C.

2.1 Drain-Source-Spannung V_{DS}

Maximal zulässiger Wert der Spannung zwischen den Drain-Source-Anschlüssen bei kurzgeschlossener Gate-Source. Ausgenommen sind Spannungsspitzen bei avalanchefesten Transistoren.

2.2 Drain-Gate-Spannung V_{DGR}

Maximal zulässiger Wert der Spannung zwischen dem Drain- und dem Gate-Anschluß bei Überbrückung der Gate-Source-Anschlüsse mit einem vorgegebenen Widerstand.

2.3 Drain-Gleichstrom I_D

Maximal zulässiger Wert des Gleichstroms über den Drain-Anschluß.

2.4 Drain-Strom, gepulst I_{Dpuls}

Maximal zulässiger Scheitelwert des Stroms über den Drain-Anschluß bei Pulsbetrieb. Die Pulsbreite und das Puls-Pausenverhältnis ist aus dem Diagramm "Zulässiger Betriebsbereich" zu entnehmen. Für Einzelpulse bei maximaler Aufsteuerung des Transistors sind höhere Werte zulässig. Werte auf Anfrage.

2 Maximum Ratings

The maximum ratings presented in the data sheets are absolute values. If one of these maximum ratings is exceeded, it may result in breakdown of the semiconductor, even if the other maximum ratings are not all used to their limits. Unless specified to the contrary, the values apply at a temperature of 25 °C.

2.1 Drain-Source Voltage V_{DS}

The maximum permissible value of the voltage across the drain-source connections with shorted Gate and Source. Glitches relating to avalanche-resistant transistors are excluded.

2.2 Drain-Gate Voltage V_{DGR}

The maximum permissible value of the voltage across the drain and gate connections when the gate-source connections are bridged by a specified resistance.

2.3 DC Drain Current I_D

The maximum permissible value of the direct current across the drain connection.

2.4 Drain Current, Pulsed I_{Dpuls}

The maximum permissible crest value of the current across the drain connection in pulsed operation. The pulse width and pulse spacing can be taken from the "Safe Operating Area" diagram. Higher values are permissible for single pulses at maximum biasing of the transistor. Values supplied on request.

2.5 Gate-Source-Spannung V_{GS}

Maximal zulässiger Wert der Spannung zwischen den Gate-Source-Anschlüssen.

2.6 Gate-Source-Spitzenspannung V_{gs}

Maximal zulässiger, nicht periodischer Spitzenwert zwischen den Gate-Source-Anschlüssen bei Logik-Level-Transistoren. Für den Störfall darf diese Spannung max. 1 s anliegen.

2.7 Maximale Verlustleistung P_{tot}

Der maximal zulässige Wert der Verlustleistung, die der Transistor abführen kann.

2.8 Betriebstemperaturbereich T_j

Bereich der zulässigen Chiptemperatur, innerhalb dessen der Transistor dauernd betrieben werden darf.

2.9 Lagertemperaturbereich T_{stg}

Temperaturbereich, innerhalb dessen der Transistor ohne elektrische Beanspruchung gelagert oder transportiert werden darf.

2.10 Maximale Löttemperatur T_{sold}

Die maximal zulässige Löttemperatur an den Anschlüssen des Halbleiters bei einem spezifizierten Abstand vom Gehäuse und für eine spezifizierte Zeit (siehe Kapitel Montage- und Löthinweise).

2.5 Gate-Source Voltage V_{GS}

The maximum permissible value of the voltage across the gate-source connections.

2.6 Gate-Source Peak Voltage V_{GS}

The maximum permissible non-repetitive peak value across the gate-source connections in logic level transistors. In the event of a malfunction, this voltage must not be applied for longer than 1 s.

2.7 Maximum Power Dissipation P_{tot}

The maximum permissible power loss that can be dissipated by the transistor.

2.8 Operating Temperature Range T_j

The range of the permissible chip temperature within which the transistor may be continuously operated.

2.9 Storage Temperature Range T_{stg}

The temperature range within which the transistor may be stored or transported without electrical stressing.

2.10 Maximum Soldering Temperature T_{sold}

The maximum permissible soldering temperature at the connections of the semiconductor, at a specified spacing from the package and for a specified time (refer to "Notes on Mounting and Soldering").

2.11 Avalanche-Energie, Einzelpuls E_{AS}

Maximal zulässige Pulsenergie beim Auftreten einer einmaligen Sperrspannungs-Durchbruchbelastung. Die Parameter: I_{D}, V_{DD}, R_{GS}, L, T_{j} sind spezifiziert.

2.12 Avalanche-Energie im Dauerbetrieb E_{AR}

Maximal zulässige Sperrspannungs-Durchbruchenergie in Dauerbetrieb bei Einhaltung der maximal zulässigen Chiptemperatur.

2.13 Avalanche Drainstrom im Dauerbetrieb I_{AR}

Maximal zulässiger Drainstrom-Scheitelwert bei periodischer Sperrspannungs-Durchbruchbelastung unter Einhaltung der maximal zulässigen Chiptemperatur.

2.14 Wärmewiderstand Chip-Gehäuse R_{thJC} oder R_{thJA}

Quotient aus der Differenz zwischen der Chip- und der Bezugstemperatur am Gehäuse, oder der Umgebung einerseits und der abgeführten Verlustleistung andererseits, bei thermischem Gleichgewicht.

2.15 Feuchteklasse

Die Angaben sind nach DIN 40040 spezifiziert.

2.16 Prüfklasse

Die Angaben sind nach DIN IEC 68-1 spezifiziert.

2.11 Avalanche Energy, Single Pulse E_{AS}

The maximum pulse-energy occurring with a unique reverse voltage breakdown load. The parameters I_{D}, V_{DD}, R_{GS}, L and T_{j} are specified.

2.12 Avalanche Energy in Continuous Operation E_{AR}

The maximum permissible reverse-voltage breakdown energy in continuous operation while observing the maximum permissible chip temperature.

2.13 Avalanche Drain Current in Continuous Operation I_{AR}

The maximum permissible drain current crest value at repetitive reverse-voltage breakdown loading while observing the maximum permissible chip temperature.

2.14 Chip to Case Thermal Resistance R_{thJC} or R_{thJA}

Quotient from the difference between the chip temperature and the reference temperature at the case or ambient air on the one hand and the dissipated power on the other, at thermal equilibrium.

2.15 Humidity Class

Details are specified in accordance with DIN 40040.

2.16 Test Class

Details are specified in accordance with DIN IEC 68-1.

3 Kennwerte

Die angegebenen Werte sind als Mittelwerte aufzufassen. In vielen Fällen werden sie durch Angabe des Streubereichs ergänzt.

3.1 Drain-Source-Durchbruchspannung $V_{\text{(BR)DSS}}$

Die Spannung zwischen den Drain-Source-Anschlüssen, gemessen bei spezifiziertem Drain-Strom und kurzgeschlossenen Gate-Source-Anschlüssen.

3.2 Gate-Schwellenspannung $V_{\text{GS(th)}}$ (Einsatzspannung)

Der Wert der Gate-Source-Spannung, gemessen bei spezifiziertem Drain-Strom und spezifizierter Drain-Source-Spannung.

3.3 Drain-Reststrom I_{DSS}

Der Wert des Drain-Stroms bei einer spezifizierten Drain-Source-Spannung und kurzgeschlossenen Gate-Source-Anschlüssen. Angegeben werden Werte bei 25 °C und einer spezifizierten höheren Chiptemperatur.

3.4 Gate-Source-Leckstrom I_{GSS}

Der Wert des Gate-Leckstroms bei einer spezifizierten Gate-Source-Spannung und kurzgeschlossenen Drain-Source-Anschlüssen.

3.5 Drain-Source-Einschaltwiderstand $R_{\text{DS(on)}}$

Der Wert des Widerstandes zwischen

3 Characteristics

Specified values should be regarded as average values. In many cases the variation range is given as well.

3.1 Drain-Source Breakdown Voltage $V_{\text{(BR)DSS}}$

The voltage across the drain-source connections measured at the specified drain current and shorted gate-source connections.

3.2 Gate Threshold Voltage $V_{\text{GS(th)}}$

The value of the gate-source voltage measured at the specified drain current and the specified drain-source voltage.

3.3 Drain Cutoff Current I_{DSS}

The value of the drain current at a specified drain-source voltage and shorted gate-source connections. The details shown are values at 25 °C and a specified, higher chip temperature.

3.4 Gate-Source Leakage Current I_{GSS}

The value of the gate leakage current at a specified gate-source voltage and shorted drain-source connections.

3.5 Drain-Source ON Resistance $R_{\text{DS(on)}}$

The value of the resistance across the

dem Drain- und Source-Anschluß bei spezifizierten Werten der Gate-Source-Spannung und des Drain-Stroms.

3.6 Übertragungssteilheit g_{fs}

Quotient aus der Änderung des Drain-Stroms und der Gate-Source-Spannung und spezifiziertem Drainstrom.

3.7 Eingangskapazität C_{iss}

Die Kapazität gemessen zwischen dem Gate- und Source-Anschluß bei für Wechselspannung kurzgeschlossenen Drain-Source-Anschlüssen. Die Werte der Gleichspannung zwischen den Gate-Source- und den Drain-Source-Anschlüssen sowie die Meßfrequenz sind spezifiziert.

3.8 Ausgangskapazität C_{oss}

Die Kapazität gemessen zwischen dem Drain- und Source-Anschluß bei für Wechselspannung kurzgeschlossenen Gate-Source-Anschlüssen. Die Werte der Gleichspannung zwischen den Gate-Source- und den Drain-Source-Anschlüssen sowie die Meßfrequenz sind spezifiziert.

3.9 Rückwirkkapazität C_{rss}

Die Kapazität gemessen zwischen dem Drain- und dem Gate-Anschluß bei Verbinden des Source-Anschlusses mit dem Schutzschirm der Meßbrücke (dreipolig). Die Werte der Gleichspannung zwischen den Gate-Source- und den Drain-Source-Anschlüssen sowie die Meßfrequenz sind spezifiziert.

drain and source connections at specified values of the gate-source voltage and the drain current.

3.6 Transconductance g_{fs}

Quotient from the variation in drain current and gate-source voltage and the specified drain current.

3.7 Input Capacitance C_{iss}

The capacitance measured across the gate and source connections with drain-source connections shorted for AC voltage. The values of the DC voltage across the gate-source and drain-source connections are specified together with the test frequency.

3.8 Output Capacitance C_{oss}

The capacitance measured across the drain and source connections with gate-source connections shorted for AC voltage. The values of the DC voltage across the gate-source and drain-source connections are specified together with the test frequency.

3.9 Reverse Transfer Capacitance C_{rss}

The capacitance measured across the drain and gate connections, the source connection being connected to the protective screen of the bridge (three-pole). The values of the DC voltage across the gate-source and drain-source connections are specified together with the test frequency.

3.10 Einschaltzeit $t_{(on)} = t_{d(on)} + t_f$

Summe aus Einschaltverzögerungszeit $t_{d(on)}$, gemessen zwischen dem 10-%-Wert der Gate-Source-Spannung und dem 90-%-Wert der Drain-Source-Spannung und der Anstiegszeit t_r, gemessen zwischen dem 90-%-Wert und dem 10-%-Wert der Drain-Source-Spannung. Schaltung und Parameter sind spezifiziert.

3.11 Ausschaltzeit $t_{off} = t_{d(off)} + t_f$

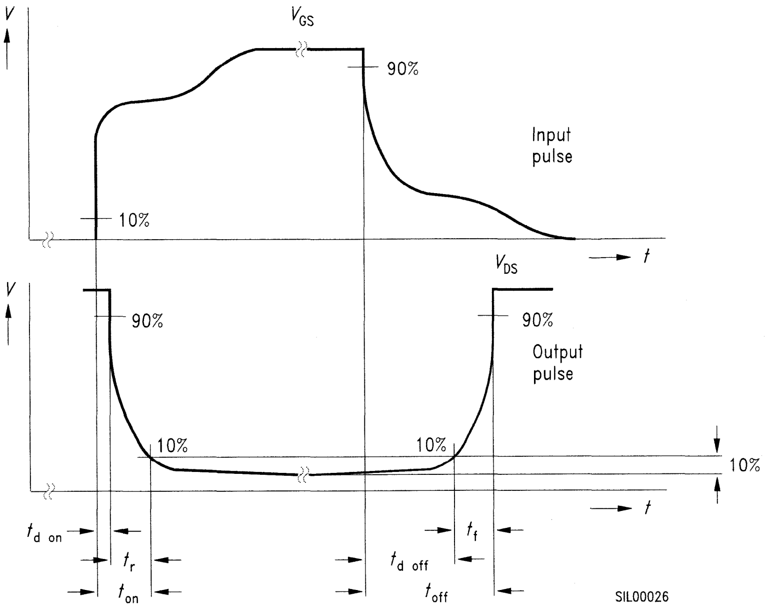
Summe aus Ausschaltverzögerungszeit $t_{d(off)}$, gemessen zwischen dem 90-%-Wert der Gate-Source-Spannung und dem 10-%-Wert der Drain-Source-Spannung und der Fallzeit t_f, gemessen zwischen dem 10-%-Wert und dem 90-%-Wert der Drain-Source-Spannung. Schaltung und Parameter sind spezifiziert.

3.10 Turn-On Time $t_{(on)} = t_{d(on)} + t_f$

Sum of the turn-on delay time $t_{d(on)}$ measured between the 10 % value of the gate-source voltage and the 90 % value of the drain-source voltage and the rise time t_r measured between the 90 % value and the 10 % value of the drain-source voltage. The circuit and parameters are specified.

3.11 Turn-Off Time $t_{off} = t_{d(off)} + t_f$

Sum of the turn-off delay time $t_{d(off)}$ measured between the 90 % value of the gate-source voltage and the 10 % value of the drain-source voltage and the fall time t_f measured between the 10 % value and the 90 % value of the drain-source voltage. The circuit and parameters are specified.



t	Times axis
$t_{d(off)}$	Turn-off delay time
$t_{d(on)}$	Turn-on delay time
t_f	Fall time
t_{on}	Turn-on time
t_{off}	Turn-off time
t_r	Rise time
V	Voltage axis
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage

Bild 29
Definition der Schaltzeit

Figure 29
Definition of switching time

3.12 Inversdioden Gleichstrom I_S

Maximal zulässiger Durchlaßgleichstrom der Inversdioden bei spezifizierter Gehäusetemperatur T_C bzw. Umgebungstemperatur T_A.

3.13 Inversdioden Gleichstrom, gepulst I_{SM}

Maximal zulässiger Scheitelwert des Stroms der Inversdiode bei Pulsbetrieb. Die Gehäusetemperatur bzw. die Umgebungstemperatur ist angegeben. Das Puls-Pausen-Verhältnis entspricht dem des Transistorpulsstroms.

3.14 Durchlaßspannung V_{SD}

Typischer Wert und obere Streugrenze der im Durchlaßzustand zwischen Source und Drain liegenden Spannung. Der Durchlaßstrom I_F, die Spannung V_{GS} und die Chiptemperatur T_j sind spezifiziert.

3.12 Inverse Diode Continuous Forward Current I_S

The maximum permissible forward current of the inverse diode at the specified case temperature T_C or ambient temperature T_A.

3.13 Inverse Diode Direct Current, Pulsed I_{SM}

The maximum permissible crest value of the inverse diode current in pulsed operation. The case temperature or the ambient temperature is presented. The pulse spacing is that of the transistor pulse current.

3.14 Forward Voltage V_{SD}

A typical value and upper limit of scattering of the voltage at ON state across the source and the drain. The forward current I_F, the voltage V_{GS} and the chip temperature T_j are specified.

3.15 Sperrverzögerungszeit t_{rr} und Sperrverzögerungsladung Q_{rr}

Angegeben ist jeweils ein typischer Wert für die im Datenblatt spezifizierten Meß- und Nebenbedingungen (siehe **Bild 30** nach DIN IEC 747 T2). Für FREDFET und FRED sind Maximalwerte angegeben.

3.16 Rückstromspitze I_{RRM}

Bei FREDFET und FRED wird ein typischer Wert der Rückstromspitze angegeben.

3.15 Reverse Recovery Time t_{rr} and Recovered Charge Q_{rr}

A typical value is presented in each case for the test and secondary conditions specified on the data sheet (refer to **Figure 30** conforming with DIN-IEC 747 T2). Maximum values are presented for FREDFETs and FREDs.

3.16 Peak reverse Current I_{RRM}

A typical value of the peak return current is presented for FREDFETs and FREDs.

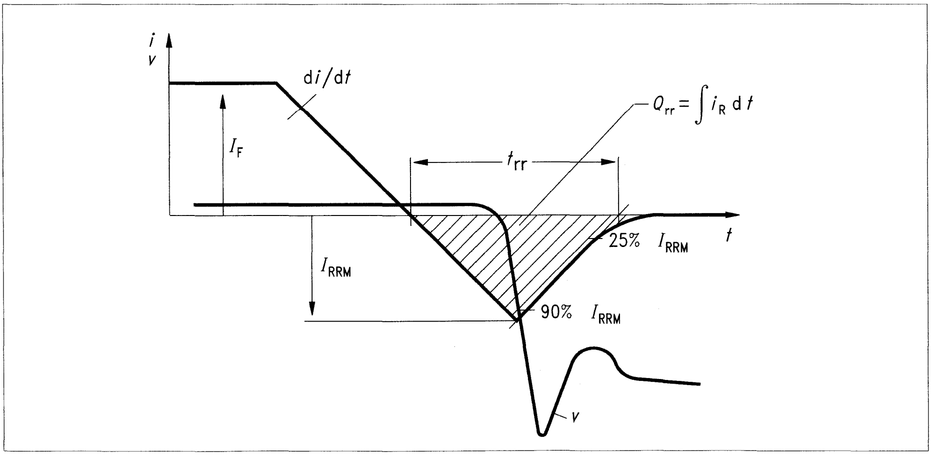


Bild 30
Sperrverzögerungszeit t_{rr}, Sperrverzögerungsladung Q_{rr} und Rückstromspitze I_{RRM}

Figure 30
Reverse recovery time t_{rr}, recovered charge Q_{rr} and peak return current I_{RRM}

4 Diagramme

4.1 Verlustleistung $P_{tot} = f(T)$

Angegeben ist die maximal zulässige Verlustleistung, abhängig von der Gehäusetemperatur T_C bzw. Umgebungstemperatur T_A.

4.2 Typische Ausgangscharakteristik $I_D = f(V_{DS})$

Aufgetragen ist die typische Abhängigkeit des Drain-Stroms I_D von der Drain-Source-Spannung V_{DS} bei vorgegebener Gate-Source-Spannung V_{GS}. Chiptemperatur T_j und Pulsbreite sind spezifiziert.

4.3 Zulässiger Betriebsbereich $I_D = f(V_{DS})$, (SOA-Diagramm)

Dargestellt ist der maximal zulässige Drain-Strom I_D abhängig von der Drain-Source-Spannung V_{DS} für Belastung mit Dauergleichstrom und mit Impulsen unterschiedlicher Breite bei spezifiziertem Puls-Pausen-Verhältnis. Die maximal zulässige Gehäusetemperatur ist spezifiziert. Innerhalb dieses Bereiches sind alle Werte von I_D und V_{DS} erlaubt, wenn der Transistor dabei thermisch nicht überlastet wird. Die $R_{DS(on)}$-Grenzlinie ist nur mit Gate-Spannungen ≥ 10 V erreichbar.

4.4 Typische Übertragungscharakteristik $I_D = f(V_{GS})$

Das Diagramm zeigt die typische Abhängigkeit des Drainstromes I_D von der Gate-Source-Spannung V_{GS}, wobei die Chiptemperatur T_j, die Pulsbreite und die Drain-Source-Spannung V_{DS} spezifiziert sind.

4 Diagrams

4.1 Power Dissipation $P_{tot} = f(T)$

The maximum permissible power dissipation is presented as a function of case temperature T_C or ambient temperature T_A.

4.2 Typical Output Characteristic $I_D = f(V_{DS})$

A plot is made of the typical dependence of the drain current I_D on the drain-source voltage V_{DS} at a given gate-source voltage V_{GS}. The chip temperature T_j and pulse width are specified.

4.3 Safe Operating Area $I_D = f(V_{DS})$, (SOA Diagram)

The maximum permissible drain current I_D is shown as a function of the drain-source voltage V_{DS} for loading with continuous direct current and with pulses of varying width at the specified pulse duty factor. The maximum permissible case temperature is specified. All values of I_D and V_{DS} are allowed within this operating area if the transistor is not thermally overloaded as a result. The $R_{DS(on)}$ boundary line can only be reached at gate voltages ≥10 V.

4.4 Typical Transfer Characteristic $I_D = f(V_{GS})$

The diagram shows the typical dependence of the drain current I_D on the gate-source voltage V_{GS}; the chip temperature T_j, the pulse width and the drain-source voltage V_{DS} are specified.

4.5 Typischer Einschaltwiderstand $R_{DS(on)} = f(I_D)$

Aufgetragen ist der typische Einschaltwiderstand $R_{DS(on)}$ in Abhängigkeit vom Drainstrom I_D bei $T_j = 25$ °C und unterschiedlichen Gate-Source-Spannungen.

4.6 Einschaltwiderstand $R_{DS(on)} = f(T_j)$

Dargestellt ist der Einschaltwiderstand in Abhängigkeit von der Chiptemperatur über den zulässigen Betriebsbereich, bei spezifiziertem Drainstrom I_D und Gate-Spannung V_{GS}. Die 98-%- und 2-%-Kurven stellen *keine* garantierten Grenzen dar, sondern nur Erfahrungswerte.

Die Temperaturabhängigkeit des Einschaltwiderstandes ist hauptsächlich abhängig von der Nennsperrspannung des Transistors, sie ist bei 50-V-Typen flacher als bei 1000-V-Typen und erklärbar durch die unterschiedliche Dotierung des Silizium-Grundmaterials.

Der Einschaltwiderstand bei Erwärmung kann nach folgender Formel berechnet werden:

4.5 Typical Turn-On Resistance $R_{DS(on)} = f(I_D)$

A plot is made of the typical turn-on resistance $R_{DS(on)}$ as a function of the drain current I_D at $T_j = 25$ °C and different gate-source voltages.

4.6 Turn-On Resistance $R_{DS(on)} = f(T_j)$

Turn-on resistance is shown as a function of chip temperature over the safe operating area at a specified drain current I_D and gate voltage V_{GS}. The 98 % and 2 % curves *do not* represent guaranteed limits but are merely empirical values.

The temperature dependence of the turn-on resistance depends primarily on the rated reverse voltage of the transistor; its slope is flatter for 50 V types than for 1000 V types and can be explained by the different doping of the silicon basic material.

Turn-on resistance during heating may be calculated from the following formula:

$$R_{DS(on)T2} = R_{DS(on)T1} \times \left(1 + \frac{Alpha}{100}\right)^{(T2 - T1)}$$

Tabelle für den Temperaturfaktor Alpha siehe Seite 92.

Table for the temperature factor Alpha see page 92.

V_{DS}	Alpha	Typ / Type
50 V	0,43	Standard SIPMOS
60 V	0,45	
100 V	0,53	
200 V	0,62	
400 V	0,69	
500 V	0,70	
600 V	0,72	
800 V	0,75	
1000 V	0,77	
250 V	0,42	FREDFET
400 V bis/to 800 V	0,52	
1000 V	0,56	

Tabelle für den Temperaturfaktor Alpha

Table for the Temperature factor Alpha

4.7 Drain-Source-Durchbruchspannung $V_{(BR)DSS}$ (Bild 31)

Angegeben ist eine Konstante "b" in Abhängigkeit von der Chiptemperatur über den zulässigen Betriebstemperaturbereich, wobei folgender mathematischer Zusammenhang gilt:

4.7 Drain-Source Breakdown Voltage $V_{(BR)DSS}$ (Figure 31)

A constant, b, is shown as a function of chip temperature over the permissible operating temperature range; the following mathematical relationship applies:

$$\boxed{V_{(BR)DSS(T_j)} = \mathbf{b} \times V_{(BR)DSS(25°C)}}$$

Die Spannung $V_{(BR)DSS\ (25°C)}$ ist der angegebene Datenblattwert.

The voltage $V_{(BR)DSS\ (25°C)}$ is the value presented on the data sheet .

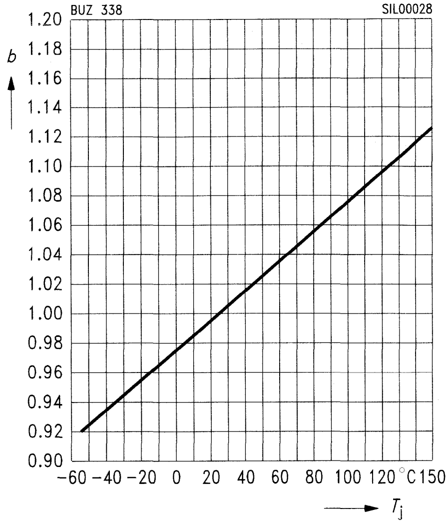


Bild 31
Drain-Source-Durchbruchspannung

Figure 31
Drain-source breakdown voltage

4.8 Typische Übertragungssteilheit $g_{fs} = f(I_D)$

Angegeben ist der typische Verlauf der Übertragungssteilheit abhängig vom Drain-Strom. Die Pulszeit, die Drain-Source-Spannung V_{DS} und die Chiptemperatur T_j sind spezifiziert.

4.8 Typical Transconductance $g_{fs} = f(I_D)$

The typical variation of conductance is presented as a function of drain current. The pulse time, the drain-source voltage V_{DS} and the chip temperature T_j are specified.

4.9 Gate-Schwellenspannung $V_{GS(th)} = f(T_j)$

Das Diagramm zeigt die Abhängigkeit des Streubereiches der Gate-Schwellenspannung $V_{GS(th)}$ von der Chiptemperatur T_j bei folgenden Parametern: $V_{DS} = V_{GS}$ und I_D.

4.9 Gate Threshold Voltage $V_{GS(th)} = f(T_j)$

The diagram shows the dependence of the variation range of the gate threshold voltage $V_{GS(th)}$ on the chip temperature T_j for the following parameters: $V_{DS} = V_{GS}$ and I_D.

4.10 Typische Kapazitäten $C = f(V_{DS})$

Dargestellt sind die typischen Kennlinien der Eingangskapazität C_{ISS}, Ausgangskapazität C_{OSS} und Rückwirkungskapazität C_{rss} in Abhängigkeit von der Drain-Source-Spannung V_{DS} bei einer Frequenz $f = 1$ MHz und einer Gate-Source-Spannung $V_{GS} = 0$ V.

4.11 Typische und maximale Durchlaßkennlinie "Inversdiode" $I_{SM} = f(V_{SD})$

Dargestellt ist die Abhängigkeit des gepulsten Inversdioden-Gleichstroms I_{SM} von der Inversdioden-Durchlaßspannung V_{SD}. Die Pulsbreite t_p und die Chiptemperatur T_j sind spezifiziert.

4.12 Drainstrom $I_D = f(T)$

Gezeigt wird der maximal zulässige Draingleichstrom in Abhängigkeit von der Gehäusetemperatur T_C bzw. Umgebungstemperatur T_A bei durchgeschaltetem Transistor, d.h. bei V_{GS} 10 V

4.13 Avalanche Energie $E_{AS} = f(T_j)$

Das Diagramm zeigt den Verlauf der maximalen Einzelpuls-Avalanche-Energie E_{AS} in Abhängigkeit der Chiptemperatur bei Nennstrom und spezifizierter Versorgungsspannung V_{DD}, Gate-Source-Widerstand R_{GS} sowie der Induktivität L (siehe auch **Abschnitt 2.1.6**).

4.10 Typical Capacitances $C = f(V_{DS})$

The typical characteristics of the input capacitance C_{ISS}, the output capacitance C_{OSS} and the reverse transfer capacitance C_{rss} are shown as a function of the drain-source voltage V_{DS} at a frequency $f = 1$ MHz and a gate-source voltage $V_{GS} = 0$ V.

4.11 Typical and Maximum "Inverse Diode" Forward Characteristic $I_{SM} = f(V_{SD})$

The dependence is shown of the pulsed inverse diode direct current I_{SM} on the inverse diode forward voltage V_{SD}. The pulse width t_p and the chip temperature T_j are specified.

4.12 Drain Current $I_D = f(T)$

The maximum permissible DC drain current is shown as a function of the case temperature T_C or ambient temperature T_A for a through-connected transistor, i.e. at $V_{GS} \geq 10$ V.

4.13 Avalanche Energy $E_{AS} = f(T_j)$

The diagram shows the variation of the maximum single-pulse avalanche energy E_{AS} as a function of chip temperature at rated current and the specified supply voltage V_{DD}, the gate-source resistance R_{GS}, as well as the inductance L (refer also to **Section 2.1.6**).

4.14 Transienter Wärmewiderstand

$Z_{\text{thJC}} = f\,(t_{\text{p}})$

Das Diagramm zeigt den Verlauf des transienten Wärmewiderstandes Z_{thJC} bei spezifiziertem Tastverhältnis $D = t_{\text{p}} / T$ in Abhängigkeit von der Belastungszeit t_{p} (Pulsbreite).

4.15 Typische Gate Ladung

$V_{\text{GS}} = t\,(Q_{\text{Gate}})$

Das Diagramm zeigt den typischen Verlauf der erforderlichen Gate-Ladung bei gegebener Gate-Source- und Drain-Source-Spannung, um einen Transistor mit dem spezifizierten Strom einzuschalten.

Die Gate-Ladung setzt sich zusammen aus der Ladung Q_{GS}, die benötigt wird, um die Gate-Source-Kapazität C_{GS} aufzuladen. Während dieser Phase – nach Erreichen der Gate-Schwellenspannung $V_{\text{GS(th)}}$ – steigt der Drainstrom auf seinen spezifizierten Wert an, und die Drain-Source-Spannung sinkt anschließend ab. Bis jedoch diese Spannung V_{DS} auf ihren eigentlichen Restwert abgesunken ist, muß die Gate-Drain-Kapazität (Millerkapazität) entladen werden. Dieser Ladungsanteil ist als Gate-Drain-Ladung Q_{GD} definiert.

Die Ladung $Q_{\text{G}} = Q_{\text{GS}} + Q_{\text{GD}}$ reicht noch nicht aus, den Transistor voll einzuschalten, da die Restspannung bzw. der Drain-Source-Einschaltwiderstand noch nicht minimiert ist. Erst bei einer Ladung entsprechend einer Gate-Source-Spannung von V_{GS} = 10 V wird der Einschaltwiderstand und damit die statischen Verluste optimiert. Diese Gesamtladung Q_{Gtot} ist

4.14 Transient Thermal Resistance

$Z_{\text{thJC}} = f\,(t_{\text{p}})$

The diagram shows the variation of the transient thermal resistance Z_{thJC} for the specified pulse duty factor $D = t_{\text{p}} / T$ as a function of the loading time t_{p} (pulse width).

4.15 Typical Gate Charge

$V_{\text{GS}} = t\,(Q_{\text{Gate}})$

The diagram shows the typical variation of the requisite gate charge at the given gate-source and drain-source voltages for turning on a transistor with the specified current.

The gate charge comprises the charge Q_{GS}, which is required for charging the gate-source capacitance C_{GS}. During this phase, after the gate threshold voltage $V_{\text{GS(th)}}$ has been reached, the drain current rises to its specified value, and the drain-source voltage then falls. But until this voltage V_{DS} has fallen to its actual residual value, the gate-drain capacitance (Miller capacitance) has to be discharged. This charge component is defined as the gate-drain charge Q_{GD}.

The charge $Q_{\text{G}} = Q_{\text{GS}} + Q_{\text{GD}}$ is not sufficient fully to turn on the transistor since the residual voltage and the drain-source turn-on resistance have not yet been minimized. Only with a charge corresponding to a gate-source voltage of V_{GS} = 10 V are turn-on resistance, and thus static losses, optimized. This whole charge Q_{Gtot} depends on the drain-source voltage that von der zu schaltenden Drain-Source-Spannung abhängig, die Höhe des zu schaltenden Drainstroms hat auf die notwendige Gesamtladung nur geringen Einfluß.

Das Diagramm wurde meßtechnisch nach dem **Prinzipschaltbild 40** bei einem Konstant-Ladestrom 1,5 mA ermittelt. Das gibt dem Anwender die Möglichkeit, nach $Q = i \times t$ den Ladestrom oder die Einschaltzeit entsprechend den Anforderungen einzustellen bzw. eine Ansteuerschaltung entsprechend zu dimensionieren.

Beispiel

Ein Schaltnetzteil soll mit einem BUZ 71 A Transistor mit 100 kHz getaktet werden.

Gegeben:	Gesucht:
Spannung $V_{\mathrm{DS}} = 40$ V	Steuerstrom I_{Steuer}
Schaltzeit $t_{\mathrm{(on)}} = 100$ ns	Steuerleistung P_{Steuer}
Frequenz $f = 100$ kHz	
Drainstrom $I_{\mathrm{Dpuls}} = 18$ A	
Steuerspannung $V_{\mathrm{GS}} = 10$ V	

has to be switched; the magnitude of the drain current that has to be switched has little influence on the requisite overall charge.

The diagram was determined by measurement in keeping with the basic **circuit diagram 40** at a constant charging current of 1.5 mA. This makes it possible for the user to adjust the charging current or turn-on time according to $Q = i \times t$, depending on the requirements, and to dimension his drive circuit accordingly.

Example

A switched-mode power supply is to be switched with a BUZ 71 A transistor at 100 kHz:

Given:	Sought:
Voltage $V_{\mathrm{DS}} = 40$ V	Drive current I_{drive}
Switching time $t_{\mathrm{(on)}} = 100$ ns	Drive power P_{drive}
Frequency $f = 100$ kHz	
Drain current $I_{\mathrm{Dpulse}} = 18$ A	
Drive Voltage $V_{\mathrm{GS}} = 10$ V	

1. Rechnung: Steuerstrom

Calculation 1: Drive current

$$Q_{\text{Gate tot}} = 24.5\ \text{nC}$$
$$I_{\text{drive}} = 24.5\ \text{nC}/100\ \text{ns}$$
$$I_{\text{drive}} = 245\ \text{mA}$$

Die Ansteuerung muß mindestens für I_{drive} = 245 mA ausgelegt sein.

The drive circuit must be designed for at least I_{drive} = 245 mA.

2. Rechnung: Steuerleistung

Calculation 2: Drive power

$$P_{\text{drive}} = Q_{\text{Gate tot}} \times V_{\text{GS}} \times f = 24.5\ \text{nC} \times 10\ \text{V} \times 100\ \text{kHz}$$
$$P_{\text{drive}} = 24.5\ \text{mW}$$

Für den Einschaltvorgang beträgt dann die mittlere Steuerleistung P_{Steuer} = 24,5 mW.

The average Drive power for turn-on is then P_{drive} = 24.5 mW.

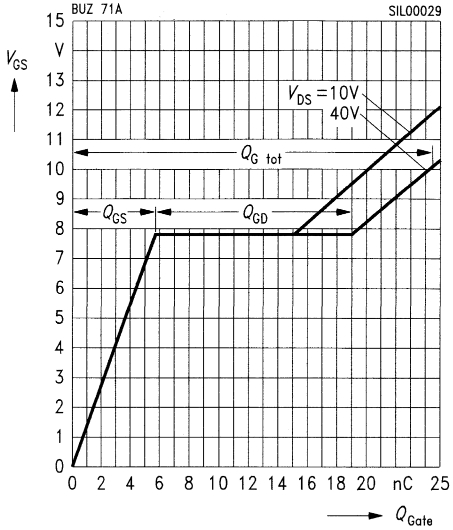


Bild 32
Typische Gate-Ladung $V_{GS} = f\,(Q_{Gate})$
(Beispiel: BUZ 71 A,
Parameter: I_{Dpulse} = 18 A)

Figure 32
Typical gate charge $V_{GS} = f\,(Q_{Gate})$
(example: BUZ 71 A,
parameter: I_{Dpulse} = 18 A)

5 Meßschaltungen (entsprechend DIN IEC 747 T8)

Die in den Datenblättern für die spezifizierten Parameter angegebenen Temperaturwerte sind bei den jeweiligen Messungen einzuhalten.

5.1 Drain Strom I_D, I_{DSS}

5 Test Circuits (Conforming with DIN IEC 747 T8)

The temperature values presented in the data sheets for the specified parameters must be observed in the measurements concerned.

5.1 Drain Current I_D, I_{DSS}

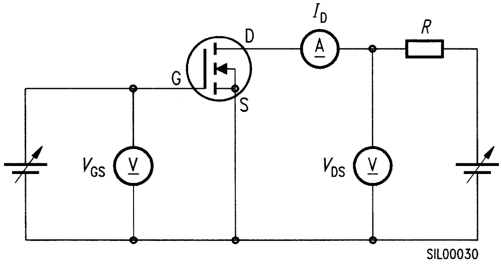


Bild 33
Prinzipschaltbild zum Messen des Drainstromes I_D und des Drain-Reststromes I_{DSS}

Figure 33
Basic circuit diagram for measuring the drain current I_D and the drain cutoff current I_{DSS}

Der Widerstand R dient als Schutz. Die spezifizierte Gate-Source-Spannung V_{GS} wird eingestellt. Ist $V_{GS} = 0$ V spezifiziert, so muß die Gate-Source-Strecke kurzgeschlossen werden.

The resistor R is used for protection. The specified gate-source voltage V_{GS} is set. If $V_{GS} = 0$ V is specified, the gate-source junction must be shorted.

5.2 Drain-Source-Einschaltwiderstand $R_{DS(on)}$

5.2 Drain-source ON Resistance $R_{DS(on)}$

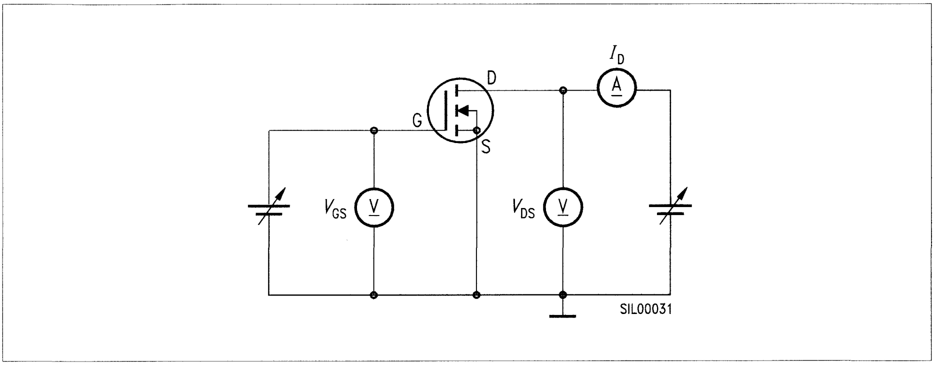


Bild 34
Prinzipschaltbild zum Messen des Einschaltwiderstandes $R_{DS(on)}$

Figure 34
Basic circuit diagram for measuring the ON resistance $R_{DS(on)}$

Allgemein wird der Einschaltwiderstand $R_{DS(on)}$ im Bereich der Sättigung gemessen. Der Innenwiderstand des Voltmeters V_{DS} muß wesentlich größer sein als der zu messende Einschaltwiderstand $R_{DS(on)}$.

The ON resistance, $R_{DS(on)}$, is generally measured within the saturation range. The internal resistance of the voltmeter V_{DS} must be considerably higher than the ON resistance to be measured, $R_{DS(on)}$.

5.3 Gate-Schwellenspannung $V_{GS(th)}$

5.3 Gate-Source Threshold Voltage $V_{GS(th)}$

(Siehe **Prinzipschaltbild 33** zum Messen des Drainstromes I_D). Die Gate-Source-Spannung, betragsgleich Drain-Source-Spannung V_{DS}, wird vom Wert Null ausgehend langsam erhöht, bis der spezifizierte Drain-Strom I_D erreicht ist.

(Refer to the basic **circuit diagram 33** for measuring the drain current I_D). The gate-source voltage, equal in magnitude to the drain-source voltage V_{DS}, is increased slowly, starting from zero, until the specified drain current I_D is reached.

5.4 Gate-Source-Leckstrom I_{GSS}

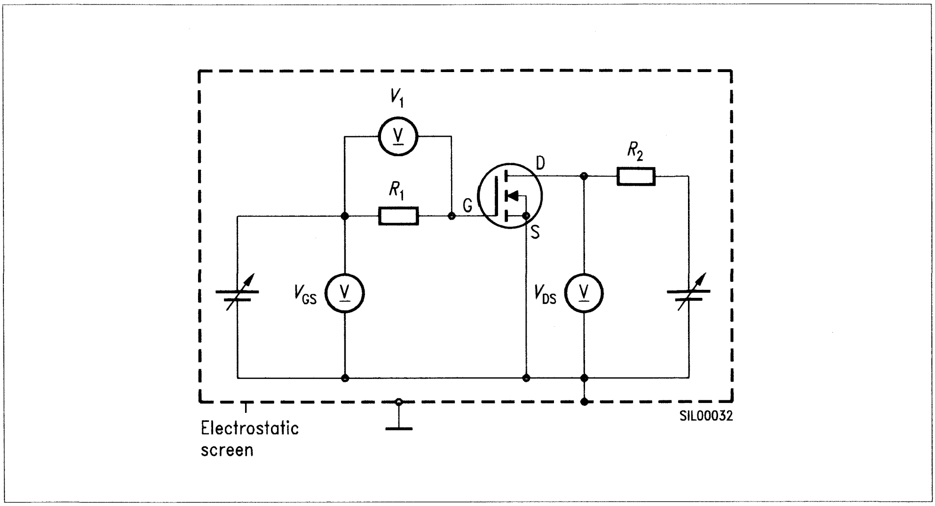


Bild 35
Prinzipschaltbild zum Messen des Gate-Source-Leckstromes I_{GSS}

R_1 und R_2 als Schutzwiderstände. R_1 soll kleiner sein als $V_{GS}/100 \times I_{GSS}$. V_1 ist ein sehr empfindliches Voltmeter mit einem Innenwiderstand von mindestens $100 \times R_1$. Der Leckstrom ist gegeben durch $I_{GSS} = V_1/R_1$. Die Schaltung muß elektrostatisch abgeschirmt werden. Außerdem ist darauf zu achten, daß die Messung nicht durch Leckströme verfälscht wird, die eventuell durch die Schaltungsanordnung entstehen.

5.4 Gate-Source Leakage Current I_{GSS}

Figure 35
Basic circuit diagram for measuring the gate-source leakage current I_{GSS}

R_1 and R_2 are used as protective resistors. R_1 should be lower than $V_{GS}/100 \times I_{GSS}$. V_1 is a very sensitive voltmeter having an intrinsic resistance of at least $100 \times R_1$. The leakage current is given by $I_{GSS} = V_1/R_1$. The circuit must be electrostatically screened. In addition, care must be taken to ensure that the measurement is not falsified by leakage currents which might possibly occur on account of the circuit arrangement.

5.5 Transistor Schaltzeit

5.5 Transistor Switching Time

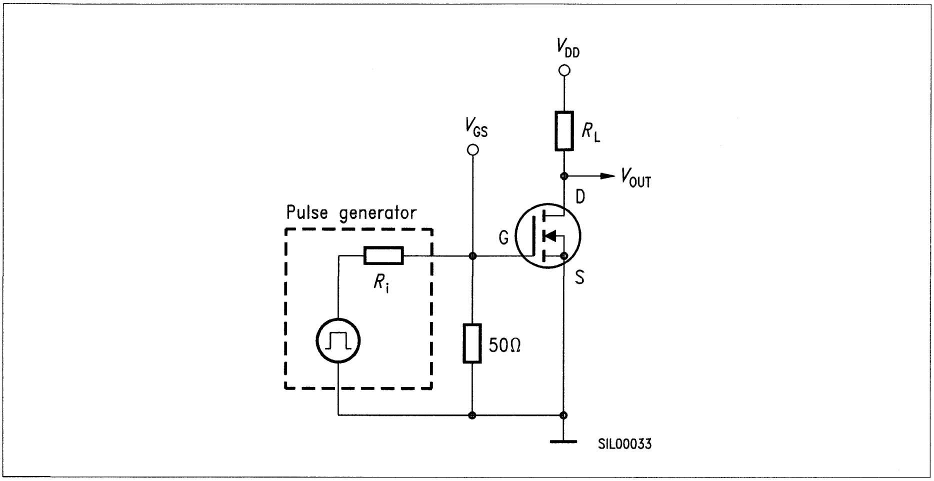


Bild 36
Prinzipschaltbild für die Messung der Transistor-Ein- und Ausschaltzeit, Definition der Schaltzeit nach Bild 29

Figure 36
Basic circuit diagram for measuring transistor turn-on and turn-off times, definition of switching time, as Figure 29

Die Schaltzeiten sind vor allem vom Gatewiderstand R_{GS}, Innenwiderstand der Ansteuerung R_i (Pulsgenerator), Versorgungsspannung V_{DD}, Lastwiderstand R_L sowie der Steuerspannung V_{GS} abhängig. Wegen meßtechnischen und Vergleichsgründen wurde die oben skizzierte Einheitsschaltung verwendet.

The switching times depend primarily on the gate resistance R_{GS}, the intrinsic resistance of the drive R_i (pulse generator), the supply voltage V_{DD}, the load resistance R_L and the control voltage V_{GS}. The standard circuit shown above was used for testing and for comparative reasons.

5.6 Eingangskapazität C_{ISS}

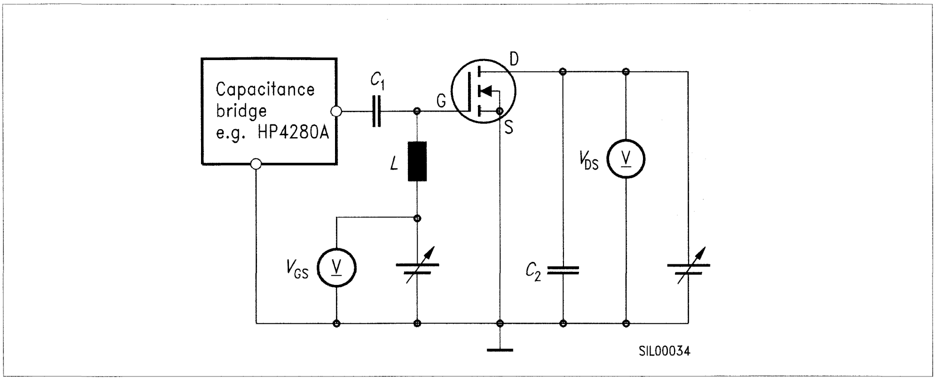


Bild 37
Prinzipschaltbild zum Messen der Eingangskapazität C_{ISS} beim Verwenden einer Meßbrücke ohne Gleichstromdurchgang

Die Kapazitäten C_1 und C_2 müssen für die Meßfrequenz einen ausreichenden Kurzschluß darstellen. Die Induktivität L soll die Gleichstromversorgung entkoppeln.

5.6 Input Capacitance C_{ISS}

Figure 37
Basic circuit diagram for measuring input capacitance C_{ISS} when using a bridge without the passage of direct current

Capacitors C_1 and C_2 must form an adequate short-circuit for the test frequency. Inductor L decouples the D_C supply.

5.7 Ausgangskapazität C_{OSS}

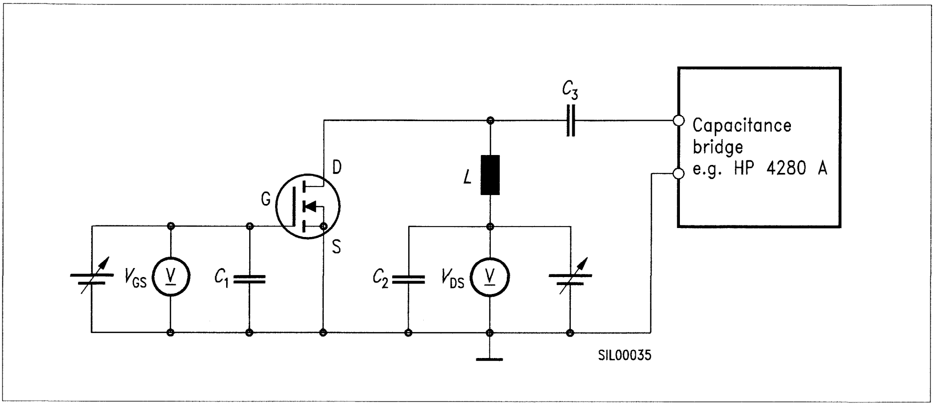


Bild 38
Prinzipschaltbild zum Messen der Ausgangskapazität C_{OSS} beim Verwenden einer Meßbrücke ohne Gleichstromdurchgang

Die Kapazitäten C_1, C_2 und C_3 müssen für die Meßfrequenz einen ausreichenden Kurzschluß darstellen. Die Induktivität L entkoppelt die Gleichstromversorgung.

5.7 Output Capacitance C_{OSS}

Figure 38
Basic circuit diagram for measuring output capacitance C_{OSS} when using a bridge without the passage of direct current

Capacitors C_1, C_2 and C_3 must form an adequate short-circuit for the test frequency. Inductor L decouples the D_C supply.

5.8 Rückwirkungskapazität C_{rss}

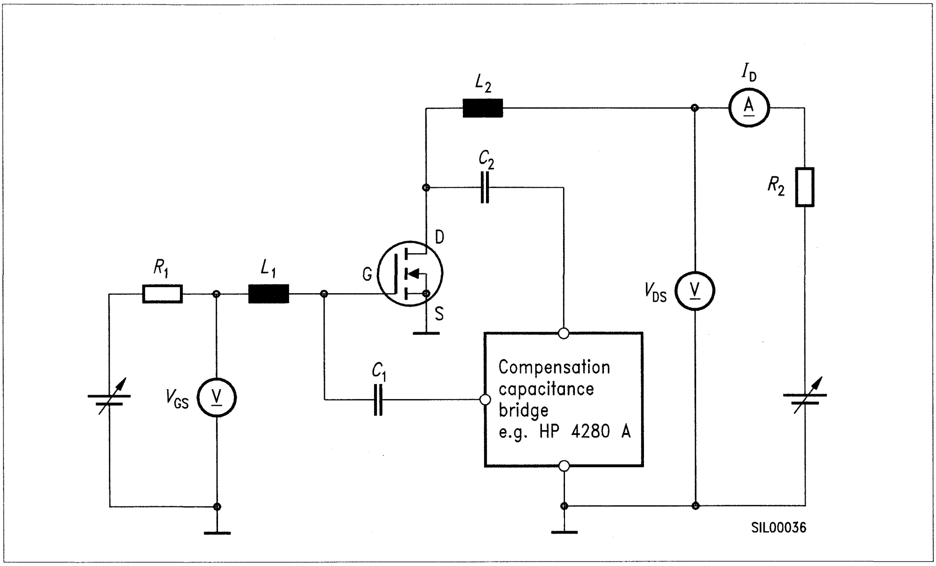


Bild 39
Prinzipschaltbild zum Messen der Rückwirkungskapazität C_{rss} beim Verwenden einer Meßbrücke ohne Gleichstromdurchgang

Die Kapazitäten C_1 und C_2 müssen für die Meßfrequenz einen ausreichenden Kurzschluß bilden. Die Induktivitäten L_1 und L_2 sollen die Gleichstromversorgung entkoppeln.

5.8 Reverse Transfer Capacitance C_{rss}

Figure 39
Basic circuit diagram for measuring reverse transfer capacitance C_{rss} when using a bridge without the passage of D_C current

Capacitors C_1 and C_2 must form an adequate short-circuit for the test frequency. Inductors L_1 and L_2 decouple the D_C supply.

5.9 Gate-Ladung Q_{Gate}

5.9 Gate Charge Q_{Gate}

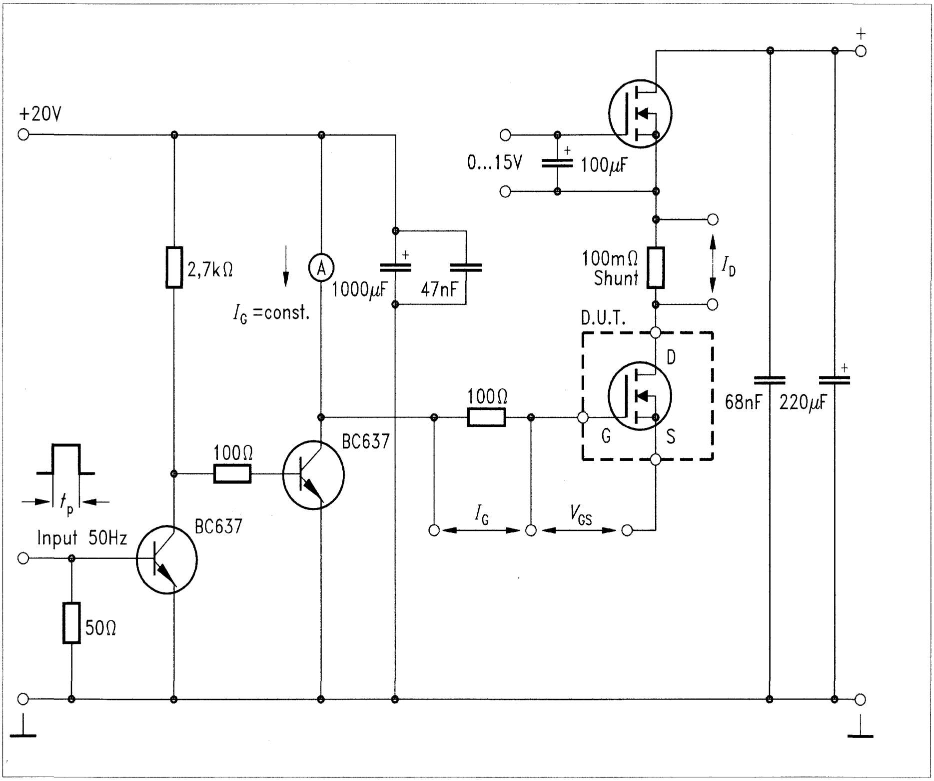


Bild 40
Prinzipschaltbild zum Messen der Gate-Ladung Q_{Gate}

Figure 40
Basic circuit diagram for measuring the gate charge Q_{Gate}

1 Qualität

Der Bereich Halbleiter (HL) der Siemens AG plant, entwickelt, fertigt und vertreibt ein breites Spektrum von Halbleiter-Bauelementen und optoelektronischen Komponenten und erbringt die dazu erforderlichen Dienstleistungen.

In diesem Markt ist hohe Qualiät der Produkte, aber auch der zugehörigen Leistungen eine unerläßliche Voraussetzung. Der Bereich Halbleiter hat deshalb ein umfassendes Qualitätskonzept, "Total Quality Management" (TQM) eingeführt. Die Qualitätsgrundsätze sind in der Qualitätsordnung des Bereichs Halbleiter festgelegt.

Wesentliche Bestandteile des TQM-Konzeptes sind ein Qualitätsprogramm und ein Qualitätssicherungssystem. Das Qualitätsprogramm beschreibt die allgemeinen Qualitätsziele – wie das Null-Fehler-Konzept für alle Leistungen – und die speziellen Ziele für Produkte und Prozesse, d.h. das in bestimmten Zeiträumen zu erreichende Maß an Fehlerfreiheit und Zuverlässigkeit.

Das Qualitätssicherungssystem regelt Verantwortung und Zuständigkeiten für Qualität und Qualitätssicherung. Es legt Abläufe fest, um die Verwirklichung der Qualitätsziele zu erreichen und nachzuweisen.

Das Qualitätssicherungssystem des HL deckt wichtige nationale und internationale Normen ab, insbesondere die für den Vertragsfall vorgesehenen Normen der Reihe DIN ISO 9000. Es ist entsprechend zertifiziert.

1 Quality

The Semiconductor Group (HL), a unit of the Siemens AG plans, develops, manufactures and markets a wide spectrum of semiconductor components and optoelectronic components and supplies the necessary respective services.

In this market a high quality of the products, as well as the proper services is an indispensable requirement. Therefore the Semiconductor Group has implemented an extensive quality concept, "Total Quality Management". The quality fundamentals are defined in the Quality Policy of the Semiconductor Group.

A quality program and a quality assurance system are essential elements of the TQM concept. The quality program describes the general quality goals – like the zero-defect-principle for all products and services – and the particular goals for products and processes, meaning the freedom from defects and the level of reliability, which have to be achieved in a given period of time.

The quality assurance system defines the responsibility and authority for quality and quality assurance. It defines procedures to achieve and to verify the realization of the quality goals.

The quality assurance system of HL covers important national and international standards, particularly those of the DIN ISO 9000 series, which are intended for contractual situations. It has achieved the relevant certificates.

2 Qualitätsprogramm

Der Geschäftszweig SIPMOS-Halbleiter hat das Ziel, durch ständige Verbesserungen seiner Produkte und Serviceleistungen die Kundenerwartungen zu erfüllen.

2 Quality Program

The aim of the SIPMOS semiconductors division is to satisfy customer expectations through constant improvement of its products and services.

Bild 41
Qualität auf solider Basis

Figure 41
Quality on a firm basis

3 Qualitätssicherungssystem

Der Fertigungsflußplan zeigt:

- den prinzipiell mit Prozeßkontrollen abgesicherten Fertigungsfluß sowie die Ausgangskontrolle fertiger Bauelemente
- den Ablauf für ständige Verbesserungen

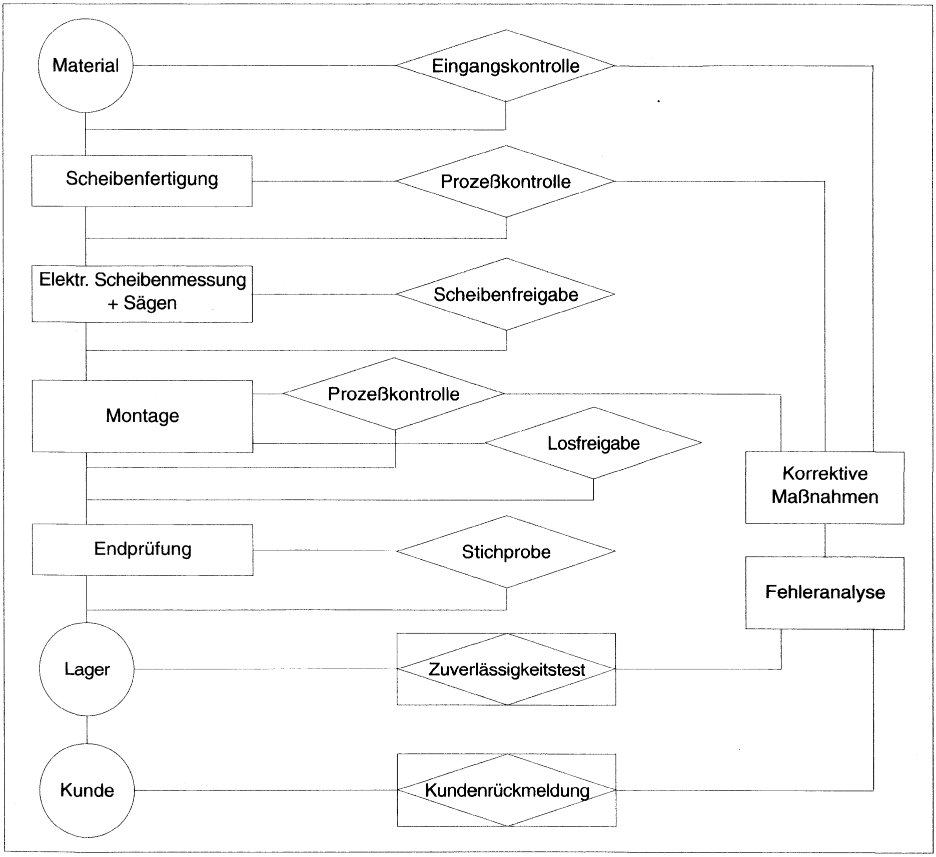


Bild 42
Fertigungsflußplan

3 Quality Assurance System

The production flowchart shows:

- Production, routinely assured by in-process inspections and the outgoing inspection of finished components
- The process of continuous improvement

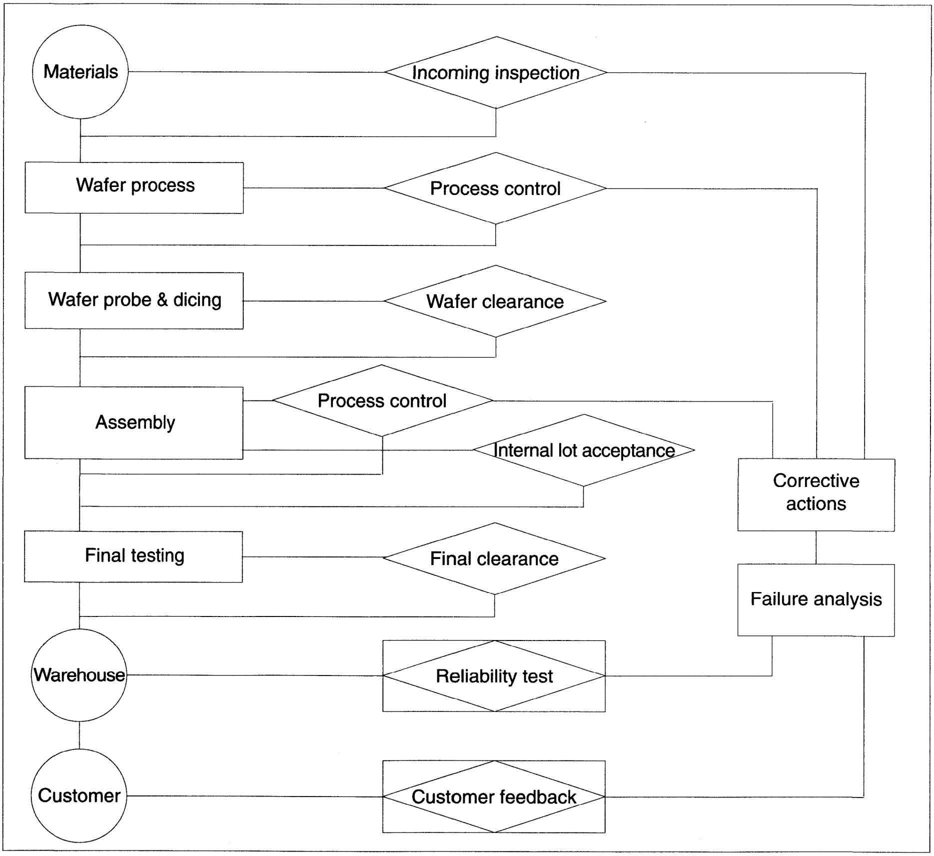


Figure 42
Production flowchart

4 Chip-Technologie

Bei der Zuverlässigkeit von SIPMOS-Halbleitern werden die Bereiche mechanischer Aufbau, Montage und Chip-Technologie berücksichtigt. SIPMOS-Halbleiter werden auf millionenfach bewährten Fertigungslinien montiert. Stabilität und damit die Zuverlässigkeit wurde bei der Chipentwicklung besonders berücksichtigt.

Der Querschnitt eines SIPMOS-Chiprandes ist in **Bild 43** dargestellt. Die Oberfläche ist durch Feldplatten, bestehend aus Polysilizium bzw. Aluminium abgedeckt. Dies gilt nicht nur für die Randzone, sondern für die gesamte Oberfläche des aktiven Systems. Damit ist der SIPMOS gegen äußere Einflüsse, wie bewegliche Ionen, abgeschirmt. Der Channel-Stopper verhindert die Ausdehnung der Raumladungszone zum Rand. Durch den lückenlosen Schutz des SIPMOS gegen äußere Einflüsse wird eine hohe Stabilität und Zuverlässigkeit auch bei Feuchteeinwirkung erreicht.

4 Chip Technology

When it comes to the reliability of SIPMOS semiconductors, attention is paid to mechanical design, mounting and chip technology. SIPMOS semiconductors are manufactured on production lines that have already been used to produce millions of transistors. Stability, and thus also reliability, received special attention during chip development.

The cross-section of a SIPMOS chip edge is illustrated in **Figure 43**. The surface is covered with field plates consisting of polysilicon and aluminum. This applies not only to the edge region but to the complete surface of the active system as well. In this way the SIPMOS is shielded against external influences, such as ion mobility. The channel stopper prevents the space-charge region from expanding to the edge. Complete protection of the SIPMOS against external influences means that high stability and reliability are assured in humid conditions.

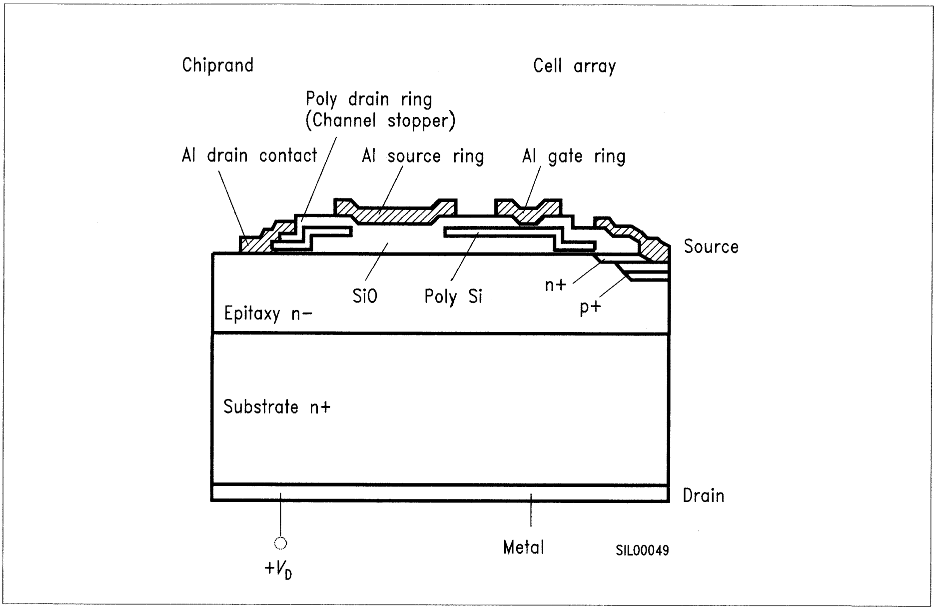


Bild 43
Querschnitt eines SIPMOS-Chiprandes

Figure 43
Cross-section of SIPMOS chip edge

5 Auslieferqualität

Zweimalige 100-%-Prüfung

Alle SIPMOS-Halbleiter werden bei folgenden Parametern einer zweimaligen 100-%-Prüfung unterzogen.

5 Delivery Quality

Double 100 % testing

All SIPMOS semiconductors are twice subjected to 100 % testing of the following parameters.

Parameter (Definition siehe Erläuterungen der Datenblattwerte)		**Parameters (see Explanation of Data Sheet Parameters for definition)**	
Drain-Source-Durchbruchspannung	$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{(BR)DSS}$
Gate-Schwellenspannung	$V_{GS(th)}$	Gate threshold voltage	$V_{GS(th)}$
Drain-Reststrom	I_{DSS}	Zero gate voltage drain voltage	I_{DSs}
Gate-Source-Leckstrom	I_{GSS}	Gate-source leakage current	I_{GSS}
Drain-Source-Einschaltwiderstand	$R_{DS(on)}$	Drain-source ON resistance	$R_{DS(on)}$
Übertragungssteilheit	g_{fs}	Forward transconductance	g_{fs}
Inversdioden-Durchlaßspannung	V_{SD}	Reverse-diode forward voltage	V_{SD}
Avalanche Energie, Einzelpuls	E_{AS}	Avalanche energy, single pulse	E_{AS}

AOQL: Anzahl der fehlerhaft gelieferten Bauelemente

Die Typenstichprobe mit AQL ist ausschließlich von dem wirtschaftlich noch vertretbaren Stichprobenumfang bestimmt (z.B. AQL 0,1: n = 125, c = 0).

Bedingt durch den hohen Qualitätsstand der Fertigung und mehrfachen elektrischen Prüfungen bei unterschiedlichen Temperaturen bewegt sich die Anzahl von ausgelieferten fehlerhaften Bauelementen im dpm-Bereich (dpm = Defekte per Mil-

AOQL: Number of Defective Components

Final clearance is in accordance with industry standards (e.g. AQL 0.1: N = 125, c = 0).

Based on the high quality level achieved in production and the numerous electrical tests performed at various temperatures, the number of defective units delivered is in the dpm (defects per million) range, corresponding to the **AOQL** = **A**verage lion, das entspricht dem **AOQL** = **A**verage **O**utgoing **Q**uality **L**evel).

Das angestrebte Ziel von 10 dpm für elektrische und 20 dpm für mechanische Ausfälle ist nahezu erreicht. Diese Aussage ermöglicht es uns zu klären, ob der durch die Typenstichprobe festgelegte dpm-Level (statistische Absicherung) mit dem tatsächlichen Qualitätsstand (100 %) übereinstimmt.

6 Zuverlässigkeitsprüfungen

Die Einhaltung der Anforderungen an SIPMOS-Halbleiter der in der **Tabelle 1** festgelegten Bedingungen zur Simulation von extremen Umwelt- und Betriebsbedingungen, ist eine Selbstverständlichkeit. Die dabei angegebenen LTPD-Level entsprechen einer statistischen Stichprobenabsicherung.

Aus den vierteljährlich durchgeführten Requalifikations-Tests kann eine Ausfallrate von < 10 Fit errechnet werden.

1 Fit $\triangleq$ 1 Fehler in 10^9 Bauelemente × Std.

Vor Freigabe neuer Produkte müssen Zuverlässigkeitstests bestanden werden. Diese Tests werden an Leitprodukten aus laufender Fertigung periodisch fortgesetzt. Die Tests wiederum sind eine Auswahl aus **Tabelle 1**.

Outgoing **Q**uality **L**evel).

The goal of 10 dpm for electrical and 20 dpm for mechanical defects has virtually been achieved. This statement allows us to examine whether the dpm level determined at final clearance (statistical guarantee) is in agreement with the actual quality (100 %).

6 Reliability Tests

It is self-evident that SIPMOS Semiconductors meet the requirements described in **Table 1**, which simulate extreme environmental and oprating conditions. The LTPD-level given merely reflects the statistical sampling check.

A failure rate of < 10 Fit can be calculated as a result of our quarterly requalification test.

1 Fit $\triangleq$ 1 defect within 10^9 devices × hours

Reliability tests have to be passed before new products are approved. These tests are continued at regular intervals on generic reference types taken from current production. The tests are a selection of those listed in **Table 1**.

Failure Criteria According to MIL-STD 19500

I_{GSS}	max. variation: ± 20 nA or ± 100% of initial value, whichever is greater.
I_{DSS}	max. variation: ± 100 µA or ± 100% of initial value, whichever is greater.
$R_{DS(on)}$	max. variation: ± 20% from initial value.
$V_{GS(th)}$	max. variation: ± 20% from initial value.
$R_{th(JC)}$	max. variation: ± 20% from initial value.

Tabelle 1
Qualifikationstest für SIPMOS-Halbleiter

Table 1
Quality Approval Test Specification for SIPMOS Semiconductor

No.	Test	Conditions	Standard	LTPD
01	High Temperature Storage	1000 h at $T_{\text{stg max}}$	DIN IEC 68 Part 2-2 Test Ba	5
02	Low Temperature Storage	168 h at $T_{\text{stg min}}$	DIN IEC 68 part 2-1 Test Aa	5
03	High Temperature Reverse Bias	1000 h, V_{DSmax}, $T_{\text{j max}}$	DIN 41 794, IEC 147-4	5
04	High Temperature Gate Stress	1000 h, V_{GSmax}, $T_{\text{j max}}$	DIN 45 930, CECC 50 000 4.5.2	5
05	High Humidity High Temperature Storage	1000 h, 85 °C, 85 % R_H	DIN 45 930, CECC 50 000 4.4.3 unbiased	5
06	High Humidity High Temperature Reverse Bias	1000 h, 85 °C, 85 % R_H V_{DS} = 80 % V_{DSmax}, but max. 80 V	DIN 45 930, CECC 50 000 4.4.3	5
07	Temperature Cycling plus Pressure Cooker Test	100 cycles of T_C plus 96 h, 119 °C, 100 % R_H 100 kPa (1 bar)	–	7
08	Temperature Cycling	1000 cycles at $T_{\text{stg max}}$ - $T_{\text{stg min}}$, but max. 150 °C	DIN IEC 68 part 2-14 Test Na	7
09	Power Cycling	10,000 cycles, $\mathrm{d}T_j = \mathrm{d}T_{\text{j max}} - 50$ K, but max. 100 K	IEC 147-4, DIN 41 794	7

No.	Test	Conditions	Standard	LTPD
10	Resistance to Solder Heat	260°C ± 5 K, 10 s ± 1 s wave	DIN IEC 68, Part 2-20 Test Tb	10
11	Resistance to Solder R_H ≙ Relative Humidity	260 °C ± 5 K, 10 s ± 1 s, wave	SN 53 063, Part 2	5
12	Resistance to Solder Heat for SMD Devices	215 °C ± 5 K, 2 × (40 ± 1) s, reflow	SN 53 063, Part 2	5
13	Solderability	235 °C ± 5 K, (aging 3)	DIN IEC 68, Part 2-20 Test Ta	10
14	Vibration for Hermetic Devices	In accordance with Standard	DIN IEC 68, Part 2-6 Test Fc	10
15	Seal Test for Hermetic Devices	$\geq 10^{-7}$ torr/s (helium test)	DIN IEC 68, Part 2-17 Test Qk	10
16	Pull Test	In accordance with Standard	DIN IEC 68, Part 2-21 Test UaI	10
17	Bending Test	In accordance with Standard	DIN IEC 68, Part 2-21 Test Ub	10

Tabelle 1
Qualifikationstest für SIPMOS-Halbleiter

Table 1
Quality Approval Test Specification for SIPMOS Semiconductor

7 CECC-Gütebestätigungssystem

Die Qualifikation nach CECC umfaßt neben der periodischen Qualifikation der Bauelemente die Qualifikation der Scheibenfertigung, der Montagelinien und des für die Durchführung der Tests verantwortlichen Prüflabors.

7 CECC Quality Assessment System

Apart from the periodic qualification of components, CECC qualification covers wafer fabrication, assembly lines and the test laboratory responsible for performing testing.

Verarbeitungsrichtlinien Gehäusemaßbilder

Mounting Instructions Package Outlines

1 Montagehinweise

Jeder SIPMOS-Halbleiter ist durch die aufgestempelte Typen- und Polaritätsbezeichnung eindeutig gekennzeichnet. Die Einbaulage der Halbleiter ist beliebig.

1.1 Bedrahtete Halbleiter im TO-218/ TO-220-Gehäuse

Anlieferform:

- Schiene

Biegevorschriften bei TO-218/TO-220-Anschlüssen

Vor dem Einbau sind die Anschlüsse auf das jeweilige Abstandsmaß der Lötanschlußpunkte zu biegen.

Dabei ist ein Biegeabstand von ≥ 2 mm einzuhalten. Der Biegeradius darf nicht kleiner als 0,5 mm sein. Ein Abbiegen der Drähte direkt am Gehäuse ist unzulässig.

Das Abwinkeln der Anschlüsse soll in einer Biegevorrichtung erfolgen. Während des Biegevorganges muß der zwischen Biegestelle und Gehäuse liegende Anschlußteil von mechanischen Zugspannungen entlastet werden. Notfalls können die Anschlüsse auch von Hand gebogen werden. Dabei muß das Anschlußende zwischen Biegestelle und Halbleiterkörper mit einer Zange festgehalten werden, ohne Einkerbungen zu verursachen. Pro Anschluß ist nur ein einmaliges Abwinkeln auf einen Winkel von max. 90° erlaubt. Ein Abbiegen der Anschlüsse auf andere Rastermaße ist möglich, jedoch müssen die Anschlüsse ebenfalls mechanisch durch geeignete Vorrichtungen gesichert werden.

1 Mounting Instructions

Every SIPMOS semiconductor is clearly identified by a stamp containing its type and polarity marking. The semiconductors may be mounted in any position.

1.1 Leaded Semiconductors in TO-218/TO-220 Package

Packing:

- Tube

Bending Instructions for TO-218/TO-220 Leads

Prior to mounting, the leads must be bent to the relevant pitch of the solder pads.

In doing so, the bend pitch must be ≥ 2 mm. The bend radius must not be less than 0.5 mm. The leads must not be bent directly onto the package.

The leads should be shaped in a bending device. The part of the lead between the point of bending and the package must be relieved of tensile stress during the bending process. If necessary, the leads may also be bent by hand. In this case the end of the lead between the point of bending and the semiconductor case must be held with pliers in such a way that no notches are caused. One-shot shaping is permitted, per lead, to an angle of not more than 90°. The leads may be bent to other pitch rasters but, again, the leads must be mechanically secured by means of suitable devices.

Die Zugfestigkeit der Anschlüsse in axialer Richtung beträgt max. 20 N.

Montageteile

Alle hier angeführten Montageteile gehören nicht zum Lieferumfang. Bitte wenden Sie sich an die entsprechenden Fachfirmen.

Montagebeispiele

The tensile strength of the leads in an axial direction is 20 N at most.

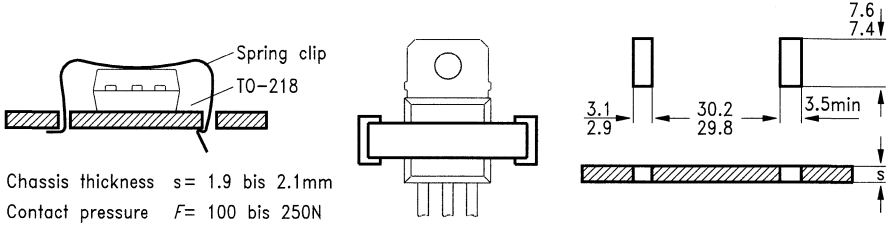
Mounting Parts

All the mounting parts listed here are options. Please contact the specialized companies concerned.

Examples of Mounting

Non–Insulated Construction with Spring Clip

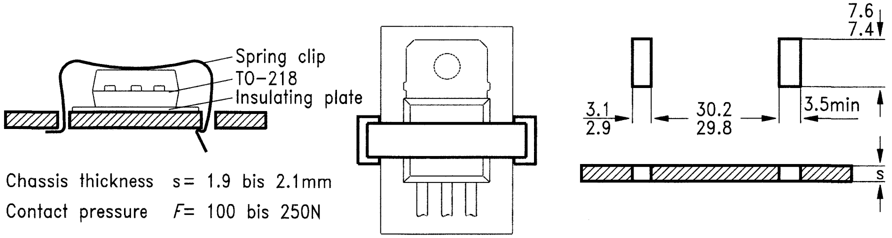
Hole grid in chassis



Chassis thickness s= 1.9 bis 2.1mm
Contact pressure F= 100 bis 250N

Insulated Construction with Spring Clip

Hole grid in chassis



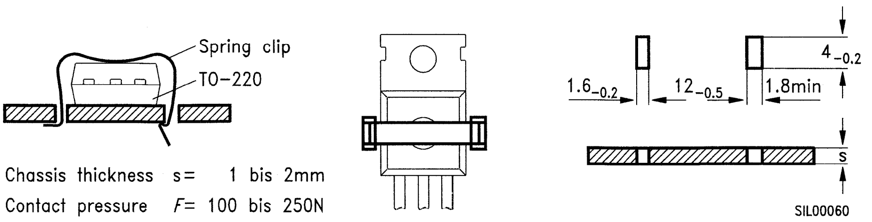
Chassis thickness s= 1.9 bis 2.1mm
Contact pressure F= 100 bis 250N

Bild 1
Kunststoffgehäuse TO-218

Figure 1
Plastic package TO-218

Non-Insulated Construction with Spring Clip

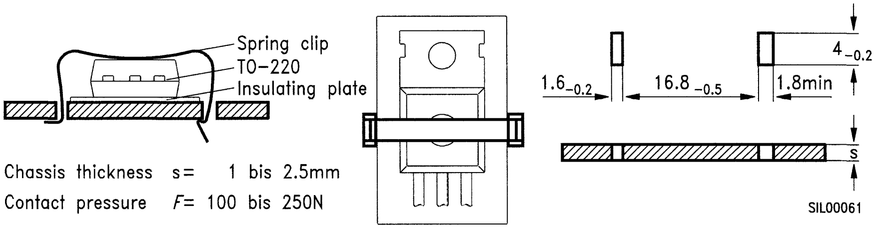
Hole grid in chassis



Chassis thickness s = 1 bis 2mm
Contact pressure F = 100 bis 250N

Insulated Construction with Spring Clip

Hole grid in chassis



Chassis thickness s = 1 bis 2.5mm
Contact pressure F = 100 bis 250N

Kunststoffgehäuse TO-220

Plastic package TO-220

Schraubbefestigung

Das empfohlene Anzugsdrehmoment für Schrauben M3 und M3,5 beträgt 60 Ncm bei einem Schraubenwerkstoff 5.8.
Daraus resultiert eine Anzugskraft von max. 1600 N.

Screw mounting

The recommended mounting torque for M3 and M3.5 screws is 60 Ncm with the screw material 5.8.
This results in a mounting force of max. 1600 N.

Kunststoffgehäuse TO-218, TO-220

Plastic package TO-218, TO-220

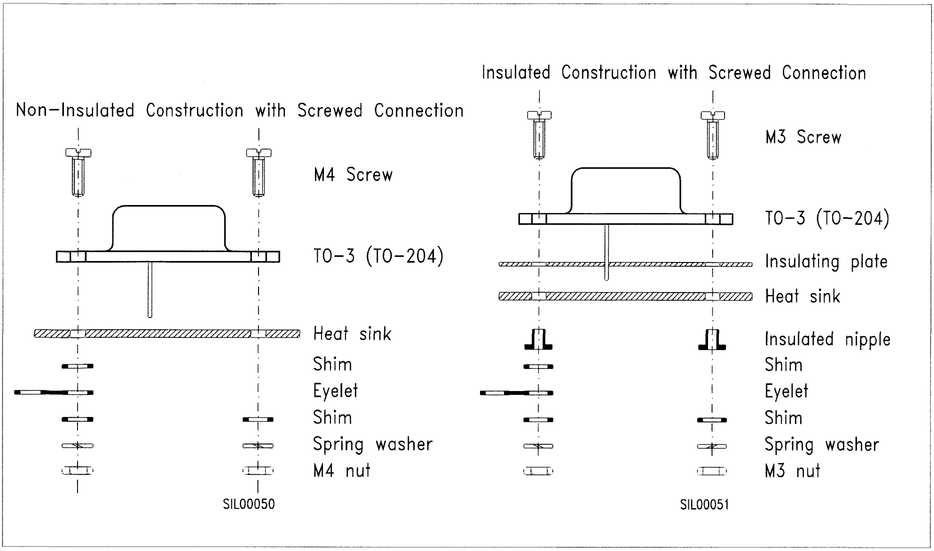


Bild 2
Metallgehäuse TO-3 (TO-204)

Achtung!

Bei isolierter Montage der Gehäuse TO-204, TO-218 und TO-220 ist der erhöhte Wärmeübergangswiderstand vom Halbleiter zum Kühlkörper zu beachten.

1.2 Halbleiter im TO-220-SMD-Gehäuse

Im Gegensatz zu bedrahteten Halbleitern kommen bei TO-220-SMD praktisch für jeden Typ zwei Anlieferformen in Frage:

- Gurtband
- Schiene

Figure 2
Metal Package TO-3 (TO-204)

Beware!

With insulated mounting of the TO-204, TO-218 and TO-220 packages due consideration must be given to the increased heat-transfer resistance from the semiconductor to the heat sink.

1.2 Semiconductors in TO-220 SMD Package

In contrast to leaded semiconductors, there are practically two forms of packing for every type in respect of TO-220 SMDs:

- Tape
- Tube

Gurtband (nach DIN IEC 286-3)

Eine häufig verwendete SMD-Anlieferung ist die Gurtbandverpackung. Der große Vorteil liegt darin, daß die Halbleiter verwechslungssicher aufbewahrt werden und außerdem viele Bestückungsautomaten diese Bereitstellung akzeptieren.

Das Gurtband hat vorgeformte Vertiefungen entsprechend der Bauelementegröße, die mit einer Deckfolie verschlossen werden. Blistergurte können aus Plastik oder aus einer beidseitig mit Plastikfolien kaschierten Alufolie bestehen. Der Vorteil der Alufolie besteht u.a. darin, daß sie sehr formstabil ist und vor elektrostatischer Aufladung schützt. Deshalb verwenden wir für die Gurtung unserer diskreten Halbleiter ausschließlich Gurte aus Alufolie.

Die Gurte sind nach DIN IEC 286-3 weltweit genormt. Damit ist sichergestellt, daß die Gurte auf allen dafür vorgesehenen Automaten verwendet werden können.

Tape (Complying with DIN IEC 286-3)

SMDs are frequently supplied in tape packing. The major advantage of tapes is that they accommodate semiconductors without danger of their being confused and, in addition, this form of feeding is accepted by many placers.

A tape has preformed recesses, that are sealed with a cover foil; their dimensions depending on the size of the devices. Blister tapes may be of plastic or a double-sided, plastic laminated aluminum foil. The advantage of aluminum foil consists, among other things, in its high stability with regard to shape and in its ability to protect against electrostatic charges. This is the reason why we only use tapes of aluminum foil for taping our discrete semiconductors.

The tapes are standardized worldwide in accordance with DIN IEC 286-3. This ensures that the tapes can be used on all the placers for which they are intended.

Gurtband-Verpackungseinheiten

Tape Packing Units

Gurtrollengröße Tape reel size	Gehäuse TO-220 E3044 package	Gehäuse TO-220 E3045 package
33 cm	1000 Stück 1.000 ea	1000 Stück 1.000 ea

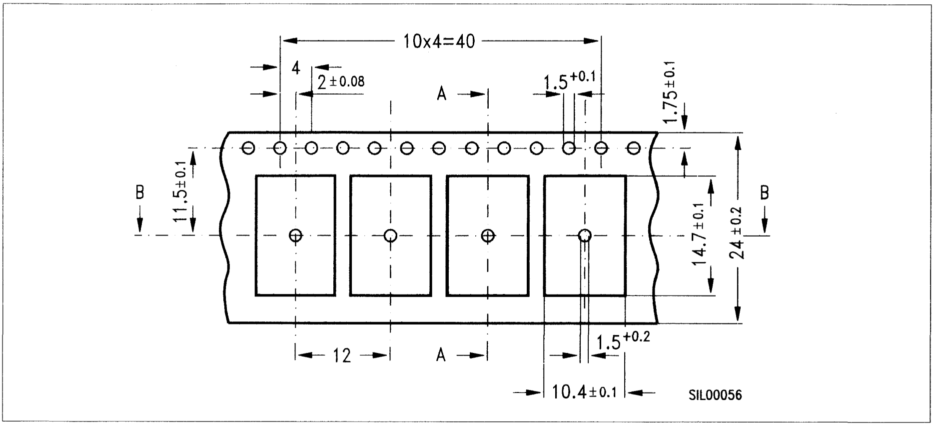


Bild 3
Gurtband

Figure 3
Tape

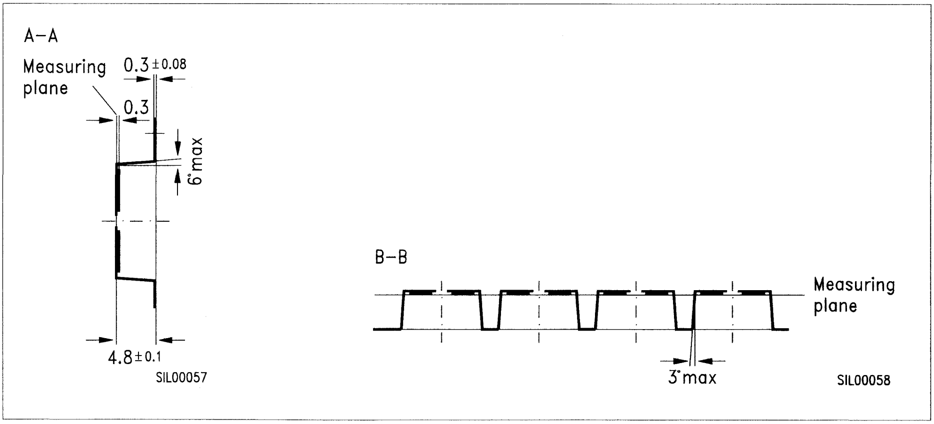


Bild 4
Bauteilfach

Figure 4
Semiconductor recess

Polarität und Lage der Bauelemente im Gurtband

Alle polarisierten Bauelemente sind in einer Richtung orientiert. Dabei liegt die Montageseite auf dem Boden des Bauteilfaches. Die Bodenseite ist definiert als unsichtbare Gurtbandseite (Unterseite).

Polarity and Position of Devices in Tape

All polarized devices are arranged in the same direction. The mounting side is on the base of the device recess. The base side is defined as the non-visible (lower) side of the tape.

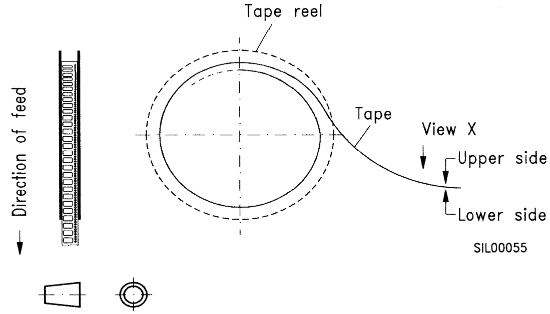


Bild 5
Gurtrolle

Figure 5
Tape reel

Fixieren der Bauelemente

Ein Herausfallen der Bauelemente aus den Bauteilfächern wird durch die Deckfolie verhindert.

Securing the Devices in Position

A cover foil prevents the devices from falling out of their compartments.

Gurtbandlagerung

Eine Gurtbandlagerung bis max. 240 h bei 40 + 5 °C und einer rel. Luftfeuchte ≤ 95 % ist zulässig.

Tape Storage

Tapes may be stored for a maximum of 240 h at 40 + 5 °C and at ≤ 95% relative humidity.

Reißfestigkeit des Gurtbandes

Die maximale Reißfestigkeit in Abwickelrichtung beträgt ≥ 10 N.

Tearing Strength of Tape

Maximum tearing strength in the direction of feed is ≥ 10 N.

Deckfolienabzugskraft

Der Winkel zwischen der Deckfolie und der Abwickelrichtung beim Abziehen beträgt 180°. Die Deckfolienabzugskraft liegt zwischen 0,2 und 1,0 N.

Peeling Force of Cover Foil

The angle between the cover foil and the direction of feed during peeling is 180°. The peeling force of the cover foil is between 0.2 and 1.0 N.

Reißfestigkeit der Deckfolie

Die minimale Reißfestigkeit der Deckfolie beträgt 10 N.

Tearing Strength of Cover Foil

Minimum tearing strength of the cover foil is 10 N.

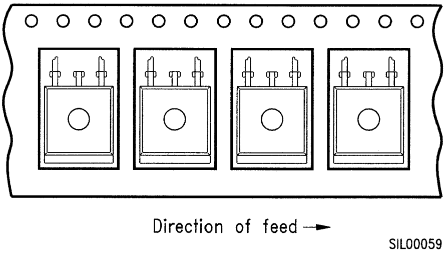


Bild 6
Polarität und Lage im Gurt

Figure 6
Polarity and orientation of tape

Deckfolienabzugsgeschwindigkeit

Die Deckfolie ist bis zu einer Abzugsgeschwindigkeit von 5 mm/s bis 20 mm/s abzugsfähig.

Peeling Rate of Cover Foil

The cover foil can be peeled at a peeling rate of 5 mm/s to 20 mm/s.

Gurtrollenkennzeichnung

Jede Gurtrolle trägt Angaben über Hersteller, Typ, Seriennummer und Datum.

Tape Reel Markings

Every tape reel bears details of its manufacturer, type, serial number, and date.

Fehlende Bauelemente

Es dürfen maximal zwei aufeinanderfolgende Bauelemente fehlen, vorausgesetzt, daß danach sechs Bauelemente

Missing Devices

Not more than two successive devices may be missing, providing they are followed by six devices without gaps. The ohne Lücke folgen. Die Anzahl von Leerstellen darf max. 0,25 % der Gesamtzahl aller Bauelemente pro Gurtrolle nicht übersteigen. Auf Wunsch sind auch andere Vereinbarungen möglich.

number of empty spaces must not exceed 0.25% of the total number of devices per tape reel. Other arrangements are possible on request.

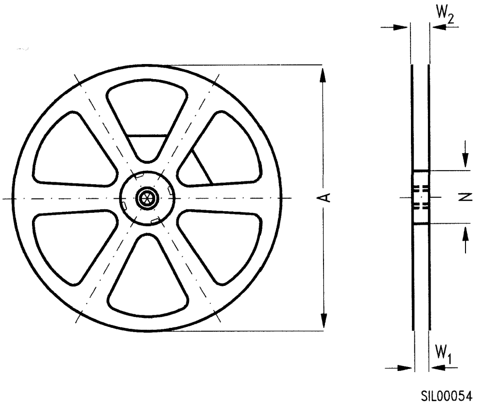
Gurtbandvor- und -nachlauf

Trägerbandgurt mit Deckfolie, ohne Bauelemente.

Carrier Tape Leader
Carrier Tape Trailer

Carrier tape with cover foil, without devices.

Gurtbandvorlauf **Carrier tape leader**	**Gurtbandnachlauf** **Carrier tape trailer**
min. 400 mm (100 Löcher) min. 300 mm (75 Löcher)	min. 400 mm (100 pitches) min. 300 mm (75 pitches)



Maß Dimension	A mm	W1 mm	W2 mm	N mm
	330	24.4 + 7	28.6	62

Bild 7
Gurtrollen-Abmessungen

Figure 7
Tape reel dimensions

TO-218/TO-220-Schiene
Die Abmessungen entsprechen der DIN-IEC-Norm.

TO-218/TO-220 per Tube
The tube dimensions correspond to the DIN IEC standards recommendation.

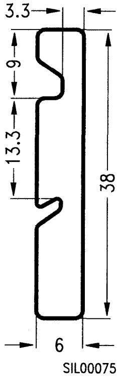
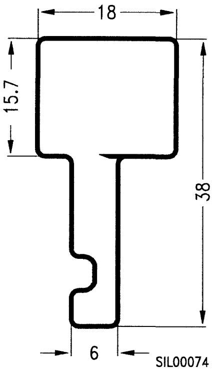
Gehäuse **Package**	**Verpackungseinheit** **Packaging unit**	**Abmessungen** **Dimensions**
TO-218 Option	25	 Länge: 524 mm Length: 524 mm
TO-218 Option E 3033	25	 Länge: 524 mm Length: 524 mm

Bild 8
Gehäuse TO-218

Figure 8
Package TO-218

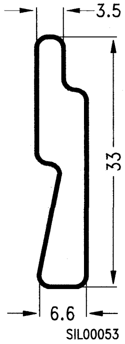
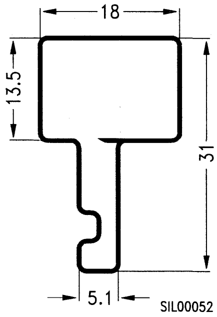
Gehäuse Package	Verpackungseinheit Packaging unit	Abmessungen Dimensions
TO-220 Option	50	 Länge: 524 mm Length: 524 mm
TO-220 Option E 3045 E 3044	50	 Länge: 524 mm Length: 524 mm

Bild 9
Gehäuse TO-220

Figure 9
Package TO-220

2 Lötvorschriften

2.1 Lötvorschriften für TO-220/ TO-218-Anschlüsse

- Lötbarkeit mit Voralterung 3 nach DIN IEC 68, Teil 2-20, Test Ta (235 °C, ± 5 K, 5 s)
- Lötwärmebeständigkeit nach DIN IEC 68, Teil 2-20, Test TB (260 °C, ± 5 K, 10 s)

Alle bedrahteten Bauelemente sind nach obiger Spezifikation geprüft und qualifiziert.

2.2 Lötvorschriften für TO-220-SMD-Anschlüsse

- Lötbarkeit mit Voralterung nach DIN IEC 68, Teil 2-20, Test Ta (215 °C, ± 3 K, 4 s)
- Lötwärmebeständigkeit nach SN 53063 Reflowlötverfahren (215 °C, ± 3 K, 2 × 40 s)

2 Soldering Instructions

2.1 Soldering Instructions for TO-220/ TO-218 Leads

- Solderability with Burn-in 3 in compliance with DIN IEC 68, Part 2-20, Test Ta (235 °C, ± 5 K, 5 s).
- Resistance to soldering heat in compliance with DIN IEC 68. Part 2-20, Test Tb (260 °C, ± 5 K, 10 s).

All leaded devices have to be tested and qualified in accordance with the above specification.

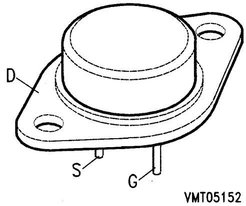
2.2 Soldering Instructions for TO-220 SMD Leads

- Solderability with burn-in in compliance with DIN IEC 68, Part 2-20, Test Ta (215 °C, ± 3 K, 4 s).
- Resistance to soldering heat in compliance with SN 53063, Reflow Method (215 °C, ± 3 K, 2 × 40 s).

Gehäusemaßbilder

Package Outlines

TO-204 AA/TO-204 AE
Gewicht etwa 13 g
Approx. weight 13 g



TO-204 AA	∅	1.0
TO-204 AE	∅	1.5

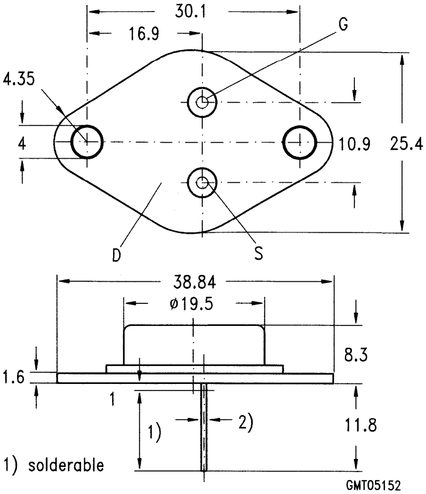
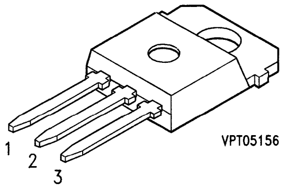


Bild 10

Figure 10

TO-218 AA
Gewicht etwa 4,5 g
Approx. weight 4.5 g



Pin	1	2	3
SIPMOS	G	D	S
IGBT	G	C	E

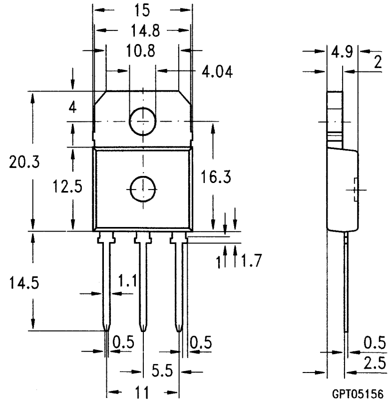
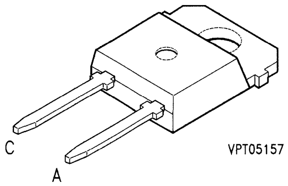


Bild 11

Figure 11

TO-218 AD
Gewicht etwa 4,5 g
Approx. weight 4.5 g



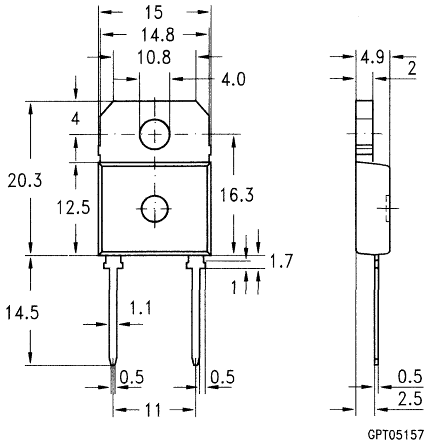
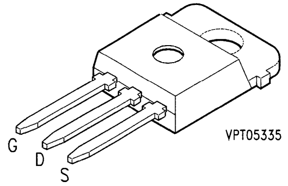


Bild 12 **Figure 12**

TO-218 AB
Gewicht etwa 4,5 g
Approx. weight 4.5 g



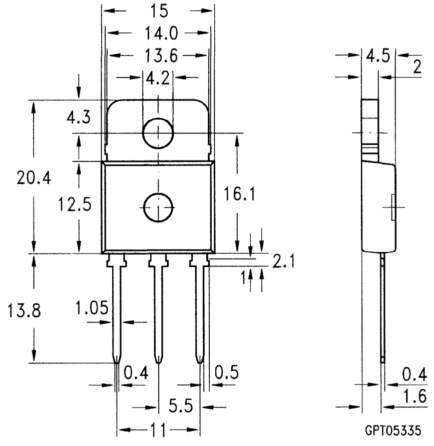
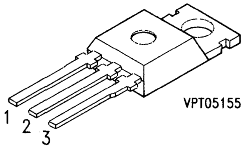
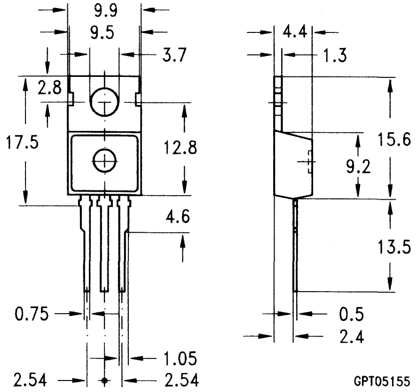


Bild 13 **Figure 13**

TO-220 AB
Gewicht etwa 2,0 g
Approx. weight 2.0 g

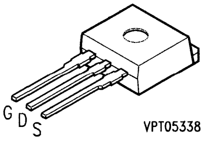


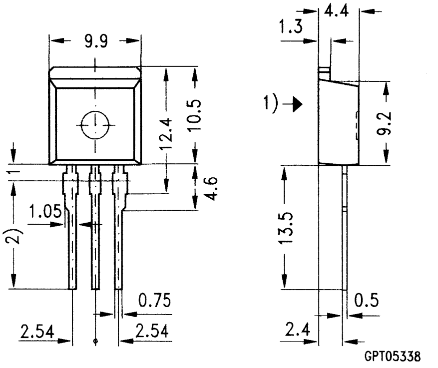


Pin	1	2	3
SIPMOS	G	D	S
IGBT	G	C	E

Bild 14 **Figure 14**

TO-220 AB Option E3046
Gewicht etwa 2,0 g
Approx. weight 2.0 g

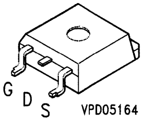


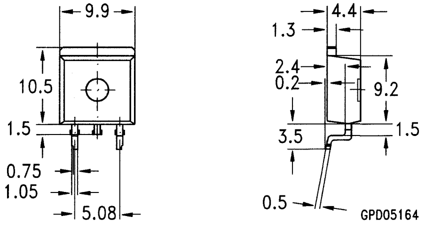


1) shear and punch direction no burrs this surface
2) dip tinning

Bild 15 **Figure 15**

TO-220 AB Option E3045
Gewicht etwa 2 g
Approx. weight 2 g



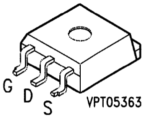


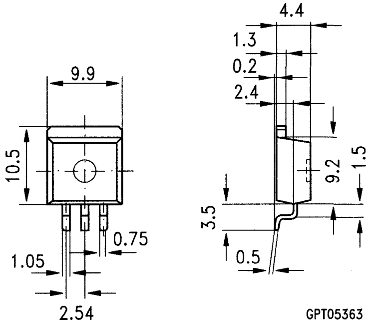
Note
Alle Metallflächen, mit Ausnahme der Schnittflächen, galvanisch verzinnt.
All metal surfaces tin plated except area of cut.

Bild 16

Figure 16

TO-220 AB Option E3044
Gewicht etwa 2 g
Approx. weight 2 g





Note
Alle Metallflächen, mit Ausnahme der Schnittflächen, galvanisch verzinnt.
All metal surfaces tin plated except area of cut.

Bild 17

Figure 17

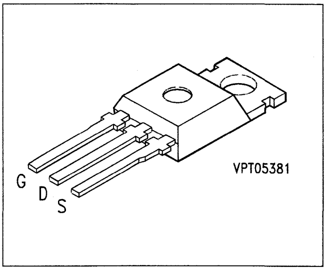
SIPMOS-Leistungstransistoren
Datenblätter
in alphanumerischer Reihenfolge

SIPMOS Power Transistors
Data sheets
in alphanumerical order

SIPMOS® Power Transistors

BUZ 10
BUZ 10 S2

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 10	50 V	23 A	0.07 Ω	TO-220 AB	C67078-S1300-A2
BUZ 10 S2	60 V	23 A	0.07 Ω	TO-220 AB	C67078-S1300-A7

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 26 °C	I_D	**23**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**92**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**23**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**1.3**	mJ
Avalanche energy, single pulse V_{DD} = 25 V, R_{GS} = 25 Ω, T_j = 25 °C I_D = 23 A, L = 15.1 µH	E_{AS}	**8.0**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	–

---

1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Static characteristics					
Drain-source breakdown voltage	$V_{(BR)\,DSS}$				V
V_{GS} = 0 V, I_D = 0.25 mA BUZ 10		50	–	–	
BUZ 10 S2		60	–	–	
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1mA	$V_{GS\,(th)}$	2.1	3.0	4.0	V
Zero gate voltage drain current V_{DS} = 50 V, V_{GS} = 0 V V_{DS} = 60 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 14 A	$R_{DS\,(on)}$	–	0.05	0.07	Ω

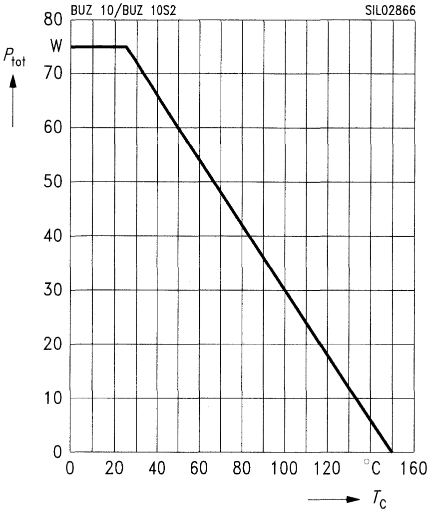
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 14 A	g_{fs}	7	13	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	650	820	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	300	450	pF
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	110	170	pF
Turn-on time t_{on}, ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, R_{GS} = 50 Ω I_D = 3 A	$t_{d(on)}$	–	20	35	ns
	t_r	–	40	65	ns
Turn-off time t_{off}, ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, R_{GS} = 50 Ω I_D = 3 A	$t_{d(off)}$	–	80	110	ns
	t_f	–	60	75	ns
Reverse diode					
Continuous reverse drain current	I_S	–	–	23	A
Pulsed reverse drain current	I_{SM}	–	–	92	A
Diode forward on-voltage I_S = 46 A, V_{GS} = 0 V	V_{SD}	–	1.5	1.9	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F/dt = 100 A/µs	t_{rr}	–	60	–	ns
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F/dt = 100 A/µs	Q_{rr}	–	0.1	–	µC

Characteristics at T_j = 25 ˚C, unless otherwise specified.

Total power dissipation

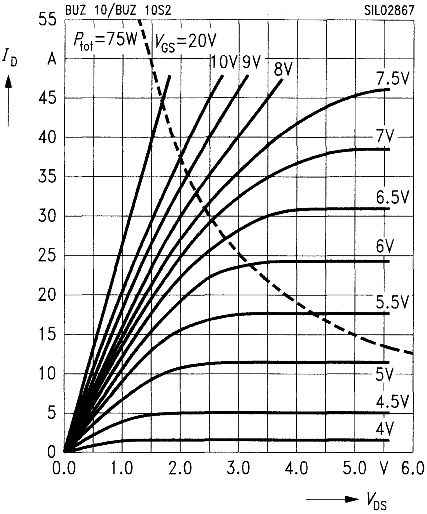
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

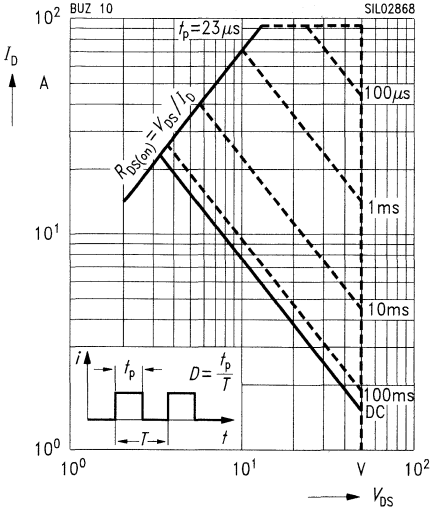
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$ **BUZ 10**

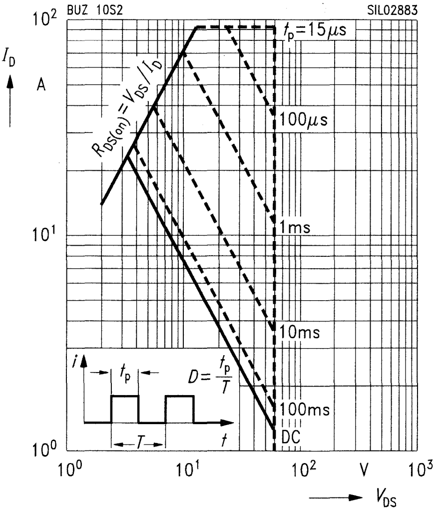
parameter: D = 0.01, T_C = 25 ˚C



Safe operating area

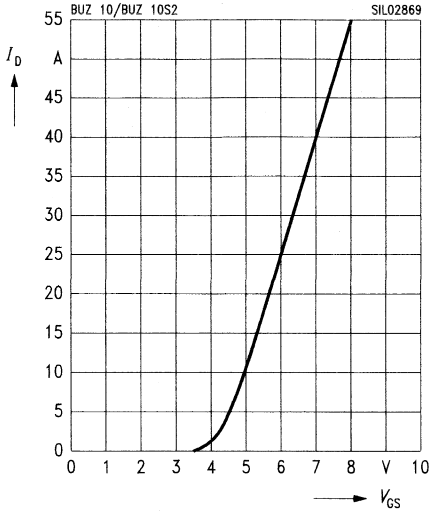
$I_D = f(V_{DS})$ **BUZ 10 S2**

parameter: D = 0.01, T_C = 25 ˚C



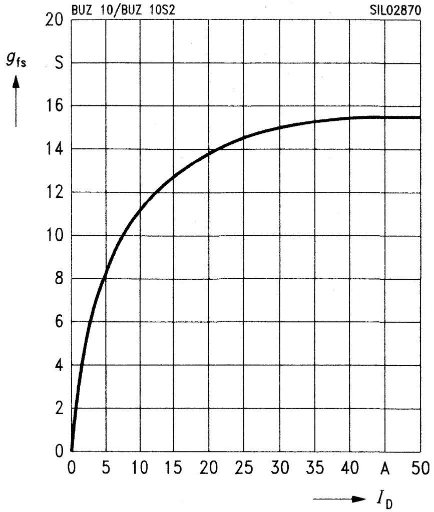
Typ. transfer characteristics

$I_D = f(V_{GS})$
parameter: t_p = 80 µs, V_{DS} = 25 V



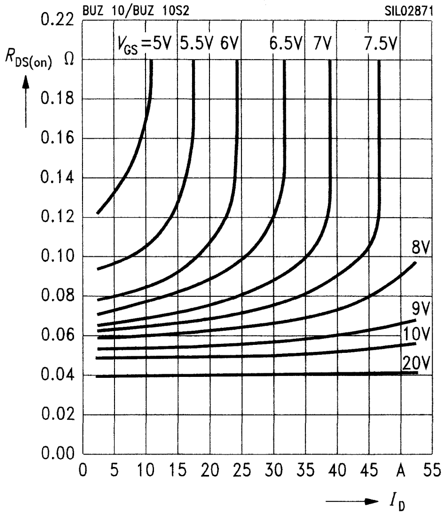
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: t_p = 80 µs



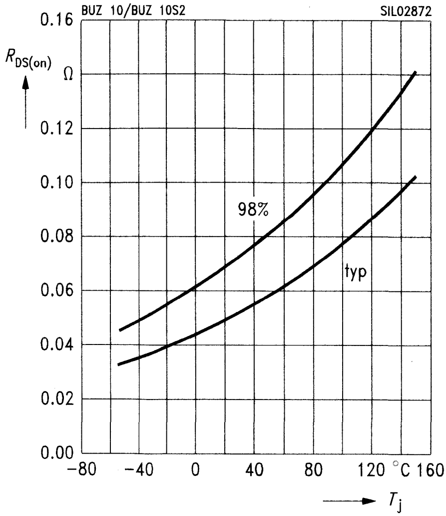
Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}



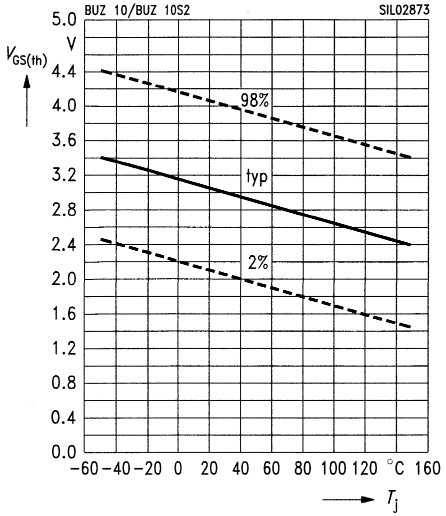
Drain-source on-resistance

$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 14 A, V_{GS} = 10 V, (spread)



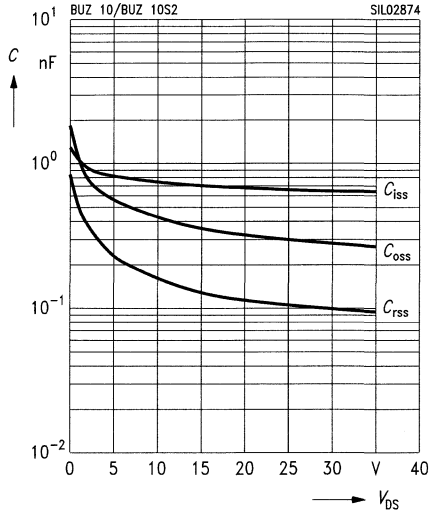
Gate threshold voltage

$V_{GS\,(th)} = f(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



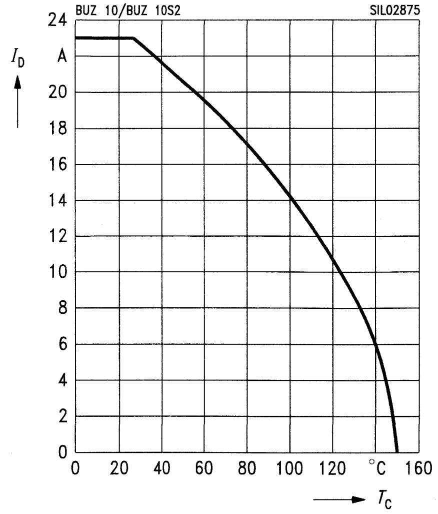
Typ. capacitances

$C = f(V_{DS})$
parameter: V_{GS} = 0 V, f = 1 MHz



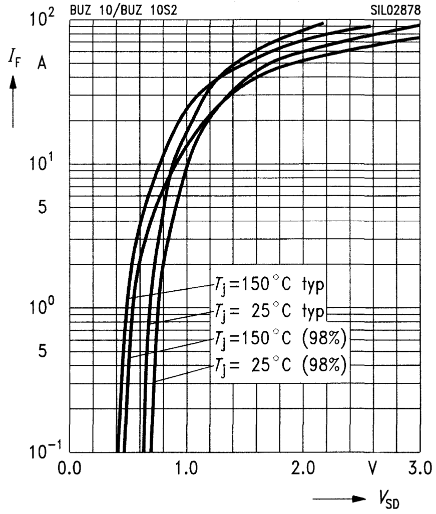
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V

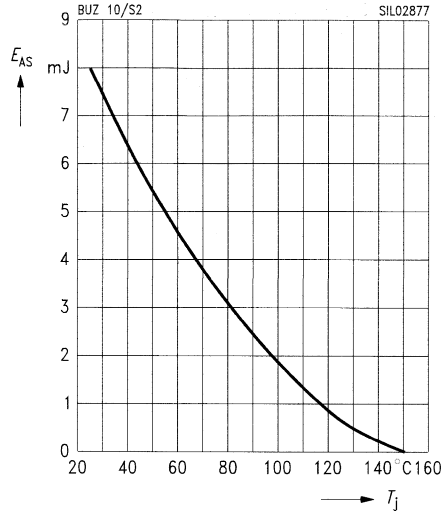


Forward characteristics of reverse diode

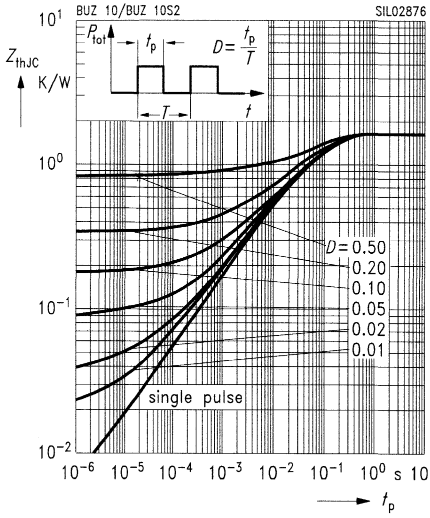
$I_F = f(V_{SD})$
parameter: T_j, t_p = 80 µs, (spread)



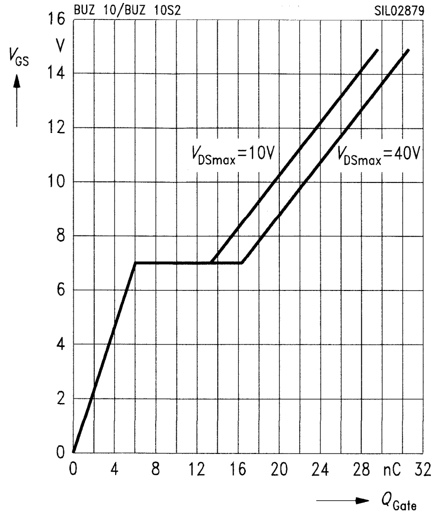
Avalanche energy $E_{AS} = f(T_j)$
parameter: I_D = 23 A, V_{DD} = 25 V
R_{GS} = 25 Ω, L = 15.1 μH



Transient thermal impedance
$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$

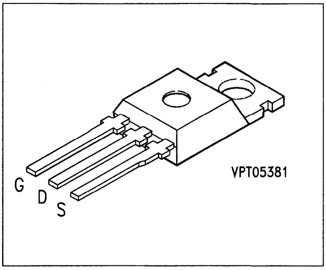


Typ. gate charge
$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls}$ = 37.5 A



SIPMOS® Power Transistor **BUZ 10 L**

- N channel
- Enhancement mode
- Logic Level
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	**Package** [1]	**Ordering Code**
BUZ 10 L	50 V	23 A	0.07 Ω	TO-220 AB	C67078-S1329-A2

Maximum Ratings

Parameter	**Symbol**	**Values**	**Unit**
Continuous drain current, $T_C = 26\ ^\circ C$	I_D	**23**	A
Pulsed drain current, $T_C = 25\ ^\circ C$	$I_{D\ puls}$	**92**	
Avalanche current, limited by $T_{j\ max}$	I_{AR}	**23**	
Avalanche energy, periodic limited by $T_{j\ (max)}$	E_{AR}	**1.3**	mJ
Avalanche energy, single pulse $I_D = 23$ A, $V_{DD} = 25$ V, $R_{GS} = 25\ \Omega$ $L = 15.1\ \mu H$, $T_j = 25\ ^\circ C$	E_{AS}	**8**	
Gate-source voltage	V_{GS}	**± 10**	V
Gate-source peak voltage, aperiodic	V_{gs}	**± 20**	
Power dissipation, $T_C = 25\ ^\circ C$	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\ JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	–

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	50	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS(th)}$	1.5	2.0	2.5	
Zero gate voltage drain current V_{DS} = 50 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 5 V, I_D = 11.5 A	$R_{DS(on)}$	–	0.06	0.07	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 11.5 A	g_{fs}	8	14.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	800	1100	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	300	450	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	110	170	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	25	40	ns
	t_r	–	75	120	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	110	160	
	t_f	–	75	95	

Electrical Characteristics (cont'd)

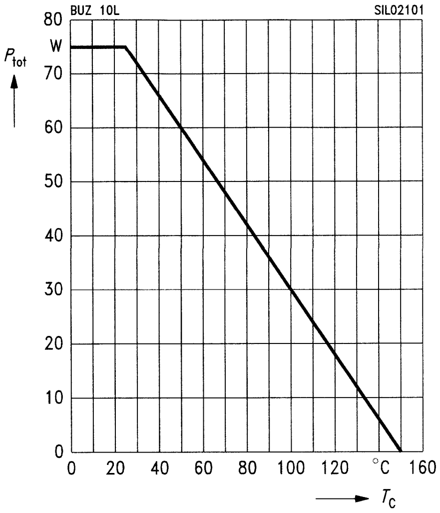
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	25	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	100	
Diode forward on-voltage I_S = 50 A, V_{GS} = 0 V	V_{SD}	–	1.5	2.0	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	60	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.1	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

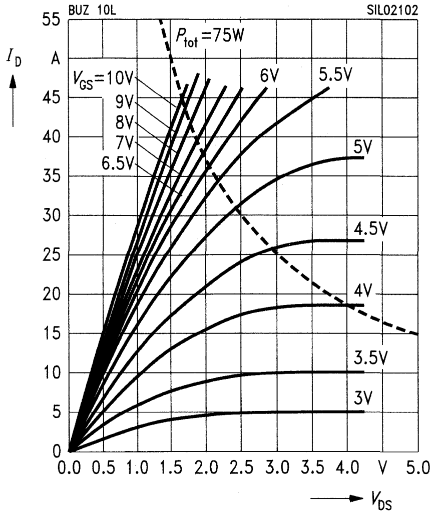
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

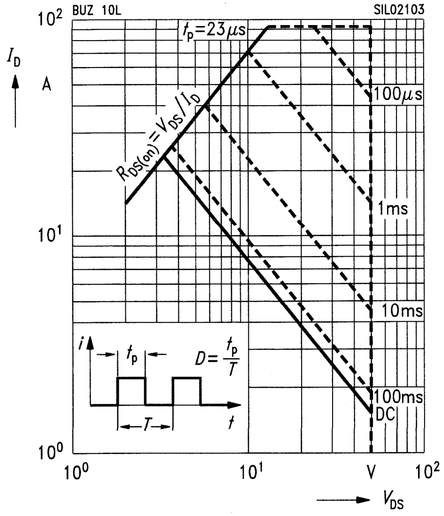
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

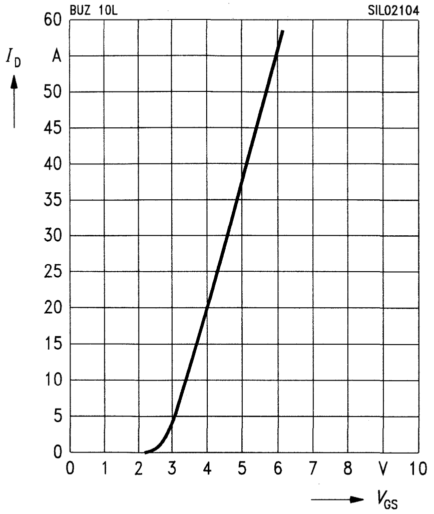
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

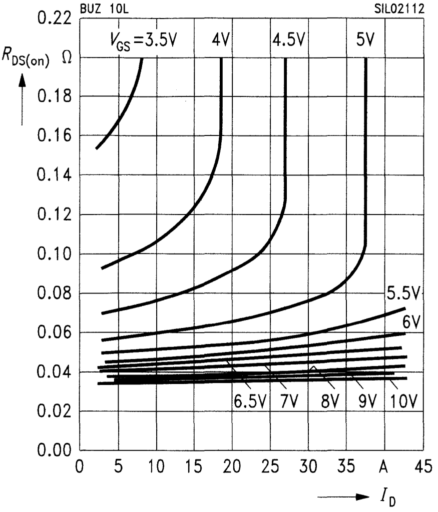
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

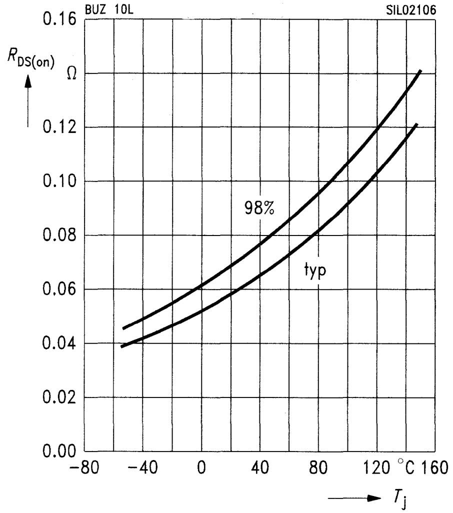
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

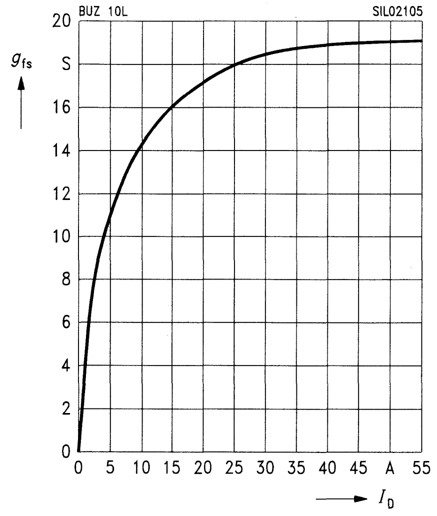
parameter: I_D = 11.5 A, V_{GS} = 5 V, (spread)



Typ. forward transconductance

$g_{fs} = f\,(I_D)$

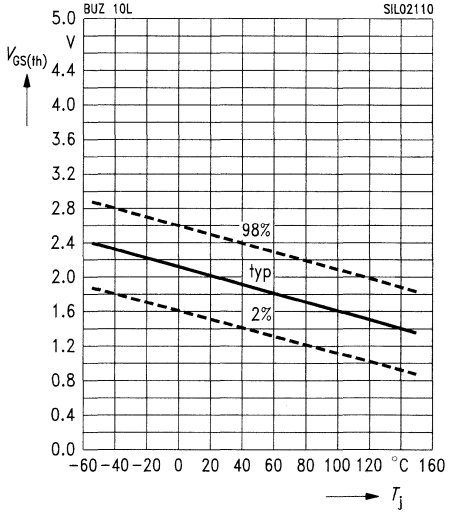
parameter: t_p = 80 µs



Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

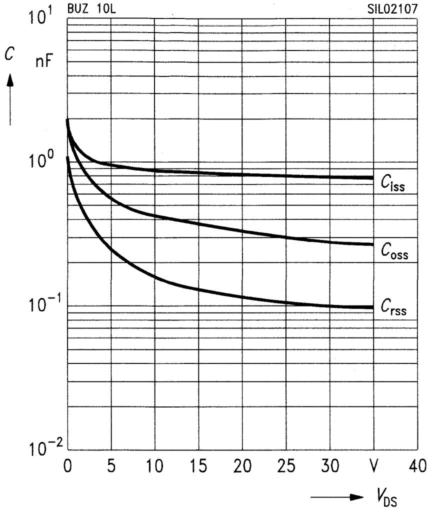
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

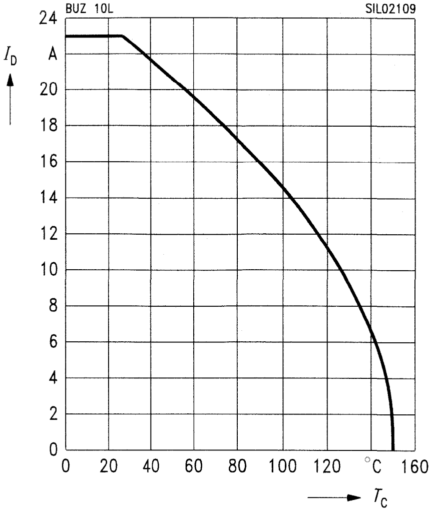
parameter: V_{GS} = 0 V, f = 1 MHz



Drain current

$I_D = f(T_C)$

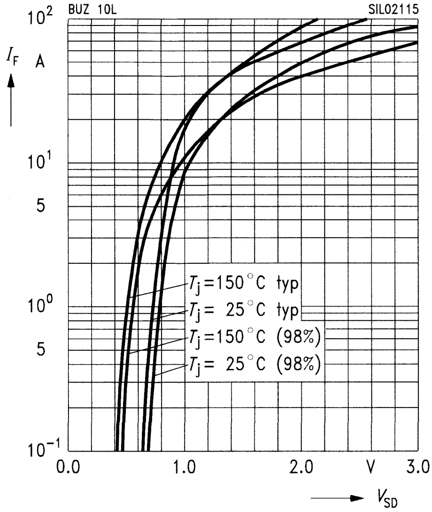
parameter: $V_{GS} \geq 5$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

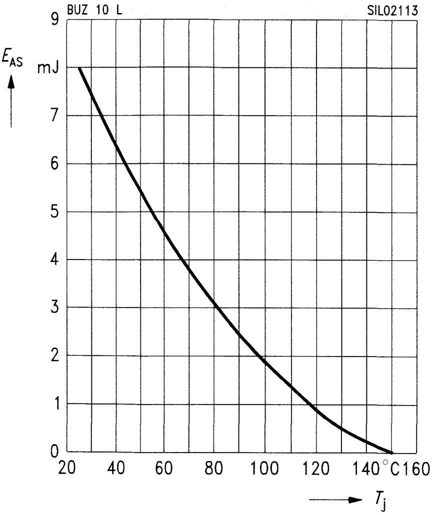
parameter: T_j, t_p = 80 µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

parameter: I_D = 23 A, V_{DD} = 25 V

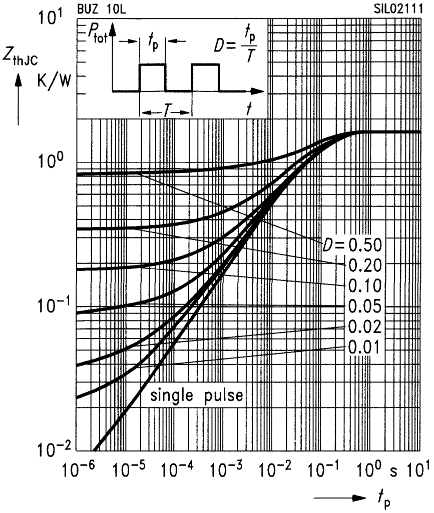
R_{GS} = 25 Ω, L = 15.1 µH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

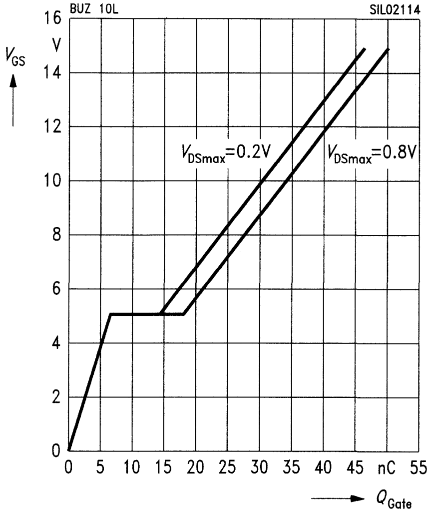
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{\text{Gate}})$

parameter: $I_{\text{D puls}}$ = 37.5 A

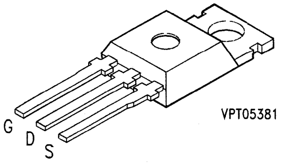


SIEMENS

SIPMOS® Power Transistors

BUZ 11
BUZ 11 A, BUZ 11 S2

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	T_C	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 11	50 V	30 A	29 °C	0.040 Ω	TO-220 AB	C67078-S1301-A2
BUZ 11 A	50 V	26 A	25 °C	0.055 Ω	TO-220 AB	C67078-S1301-A3
BUZ 11 S2	60 V	30 A	29 °C	0.040 Ω	TO-220 AB	C67078-S1301-A5

Maximum Ratings

Parameter	Symbol	BUZ			Unit
		11	**11 A**	**11 S2**	
Continuous drain current	I_D	**30**	**26**	**30**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**120**	**104**	**120**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**30**			
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**1.9**			mJ
Avalanche energy, single pulse V_{DD} = 25 V, R_{GS} = 25 Ω, T_j = 25 °C I_D = 30 A, L = 15.6 µH	E_{AS}	**14**			
Gate-source voltage	V_{GS}	**± 20**			V
Power dissipation, T_C = 25 °C	P_{tot}	**75**			W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**			°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	–

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA BUZ 11 / 11 A BUZ 11 S2	$V_{(BR)\,DSS}$	 50 60	 – –	 – –	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 0.25 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	V
Zero gate voltage drain current V_{GS} = 0 V V_{DS} = 50 V BUZ 11 / 11 A V_{DS} = 60 V BUZ 11 S2 T_j = 25 °C T_j = 125 °C	I_{DSS}	 – –	 0.1 10	 0.1 100	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 19 A BUZ 11 / 11 S2 BUZ 11 A	$R_{DS\,(on)}$	 – –	 0.03 0.04	 0.04 0.055	Ω

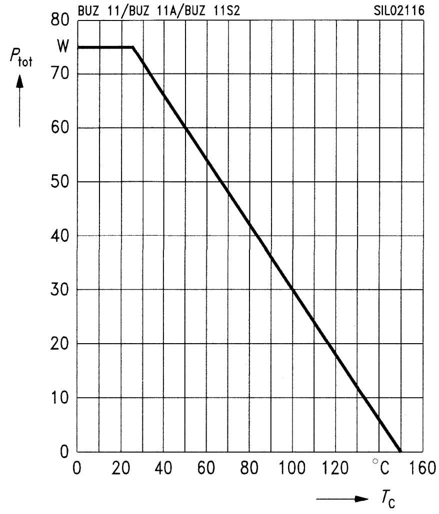
Electrical Characteristics (cont'd)
at $T_j = 25\ ^\circ C$, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$ $I_D = 19$ A	g_{fs}	10	17	–	A
Input capacitance $V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	C_{iss}	–	1000	1350	pF
Output capacitance $V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	C_{oss}	–	450	680	pF
Reverse transfer capacitance $V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	C_{rss}	–	165	250	pF
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_D = 3$ A, $R_{GS} = 50\ \Omega$	$t_{d\,(on)}$ t_r	 –	15 55	25 85	ns
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_D = 3$ A, $R_{GS} = 50\ \Omega$	$t_{d\,(off)}$ t_f	– –	120 80	160 110	ns
Reverse diode					
Continuous reverse drain current $T_C = 25\ ^\circ C$ BUZ 11 / 11 S2 BUZ 11 A	I_S	 – –	 – –	 30 26	A
Pulsed reverse drain current $T_C = 25\ ^\circ C$ BUZ 11 / 11 S2 BUZ 11 A	I_{SM}	 – –	 – –	 120 104	A
Diode forward on-voltage $V_{GS} = 0\ V$ $I_S = 60$ A	V_{SD}	–	1.6	1.8	V
Reverse recovery time $V_R = 30$ V, $I_F = I_S$, $di_F / dt = 100$ A/µs	t_{rr}	–	80	–	ns
Reverse recovery charge $V_R = 30$ V, $I_F = I_S$, $di_F / dt = 100$ A/µs	Q_{rr}	–	0.1	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

$P_{tot} = f(T_C)$

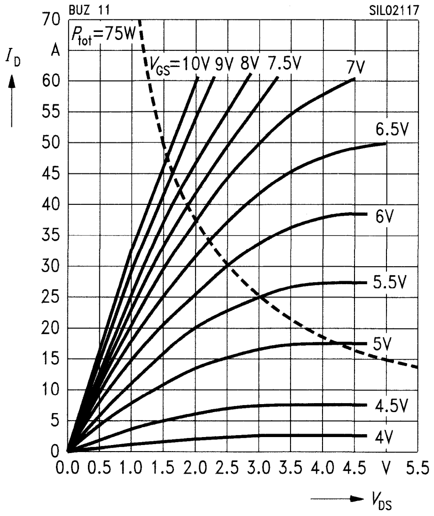


Typ. output characteristics

$I_D = f(V_{DS})$

BUZ 11

parameter: t_p = 80 µs

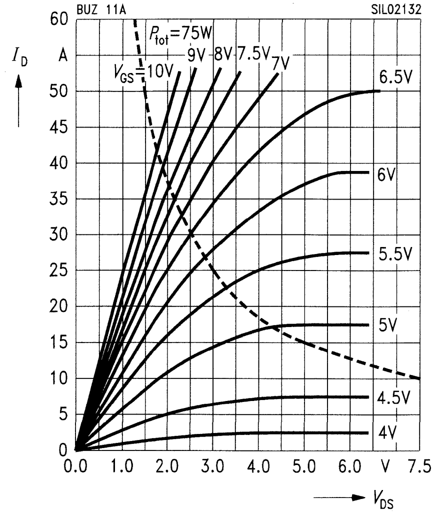


Typ. output characteristics

$I_D = f(V_{DS})$

BUZ 11A

parameter: t_p = 80 µs

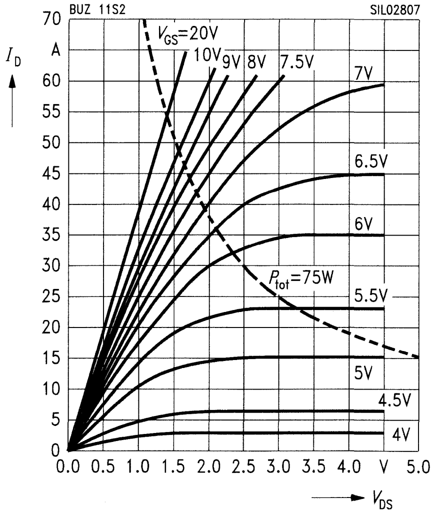


Typ. output characteristics

$I_D = f(V_{DS})$

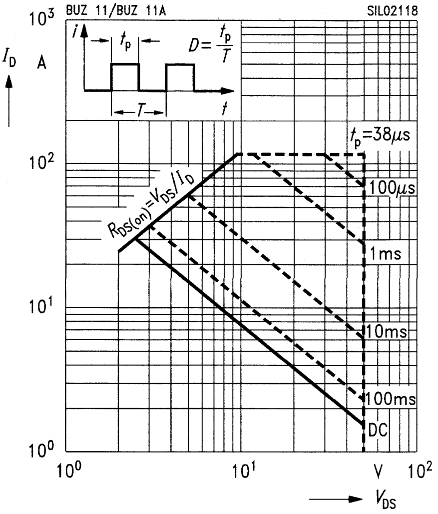
BUZ 11 S2

parameter: t_p = 80 µs



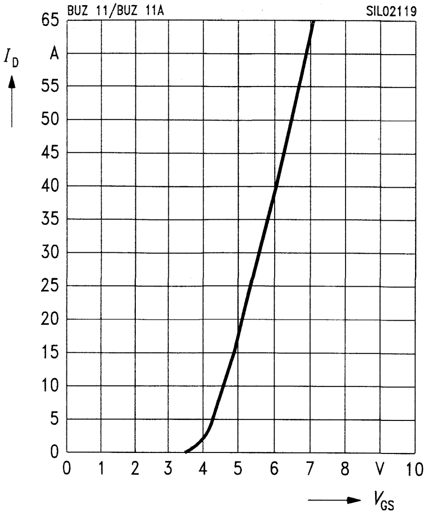
Safe operating area

$I_D = f(V_{DS})$ **BUZ 11 / BUZ 11 A**
parameter: $D = 0.01$, $T_C = 25$ °C



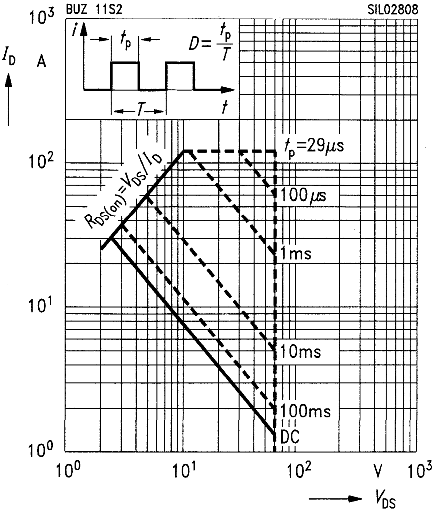
Typ. transfer characteristics

$I_D = f(V_{GS})$ **BUZ 11 / BUZ 11 A**
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



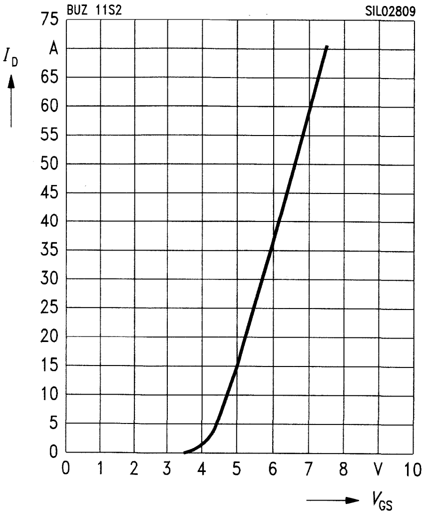
Safe operating area

$I_D = f(V_{DS})$ **BUZ 11 S2**
parameter: $D = 0.01, T_C = 25$ °C



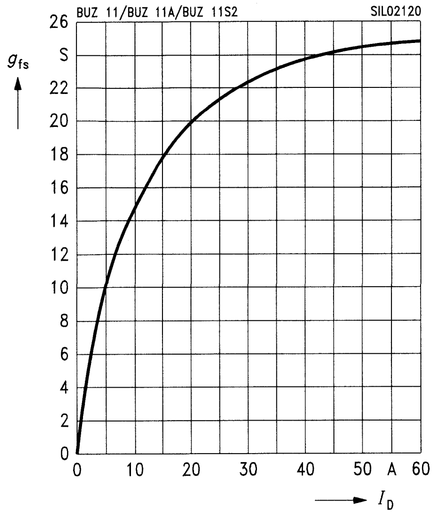
Typ. transfer characteristics

$I_D = f(V_{GS})$ **BUZ 11 S2**
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



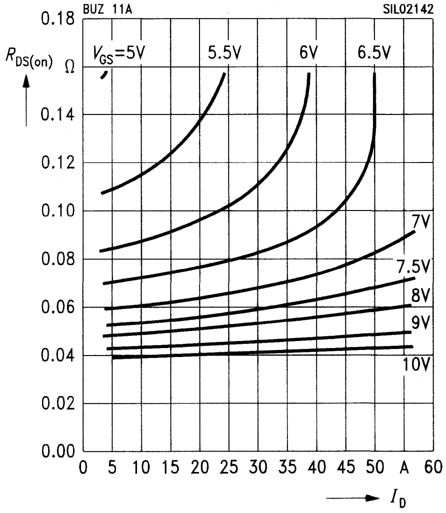
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: t_p = 80 µs



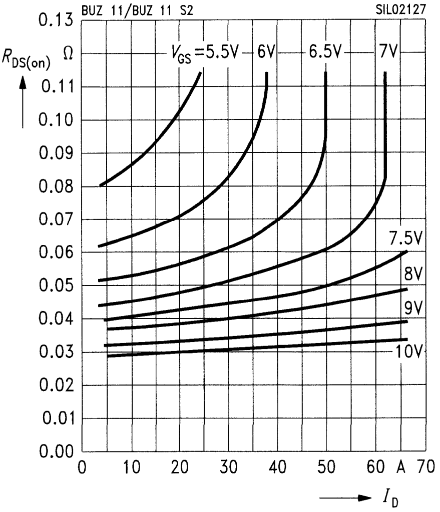
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 11 A**
parameter: V_{GS}



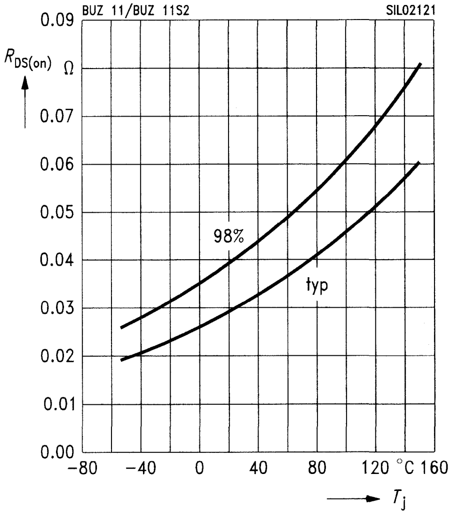
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 11 / BUZ 11 S2**
parameter: V_{GS}



Drain-source on-resistance

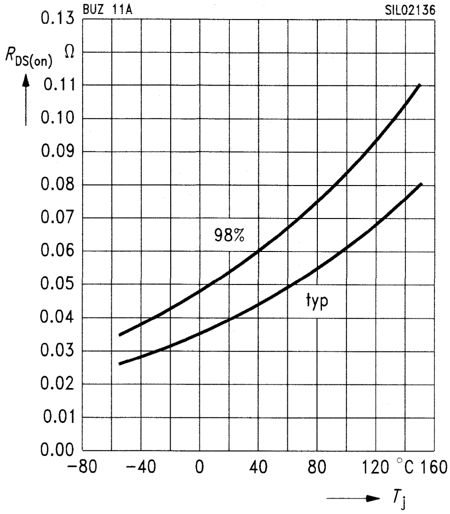
$R_{DS(on)} = f(T_j)$ **BUZ 11/BUZ 11 S2**
parameter: I_D = 19 A, V_{GS} = 10 V, (spread)



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 11 A**

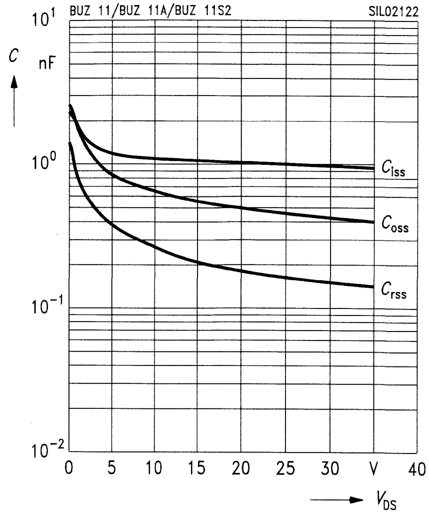
parameter: I_D = 19 A, V_{GS} = 10 V, (spread)



Typ. capacitances

$C = f\,(V_{DS})$

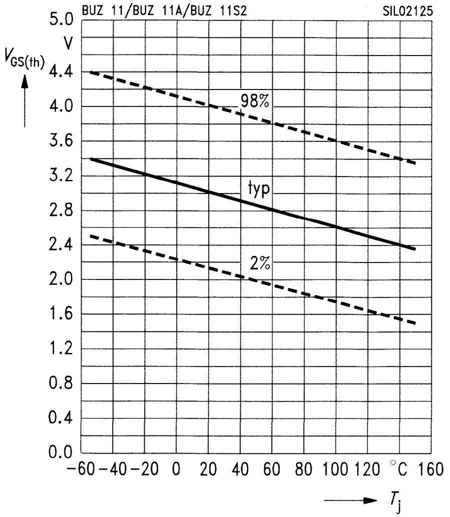
parameter: V_{GS} = 0 V, f = 1 MHz



Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

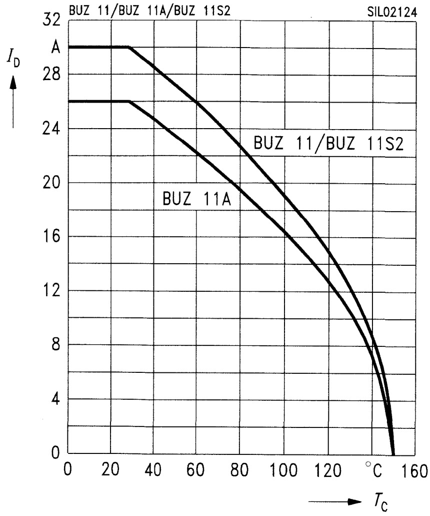
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Drain current

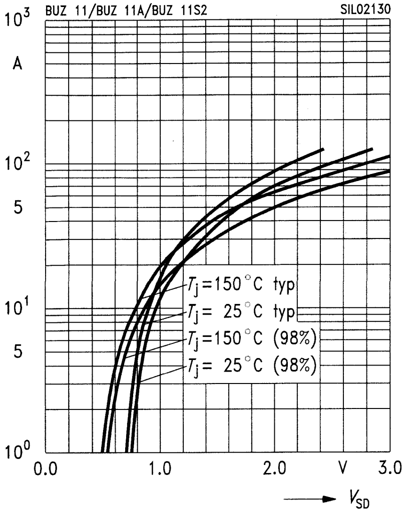
$I_D = f\,(T_C)$

parameter: $V_{GS} \geq$ 10 V



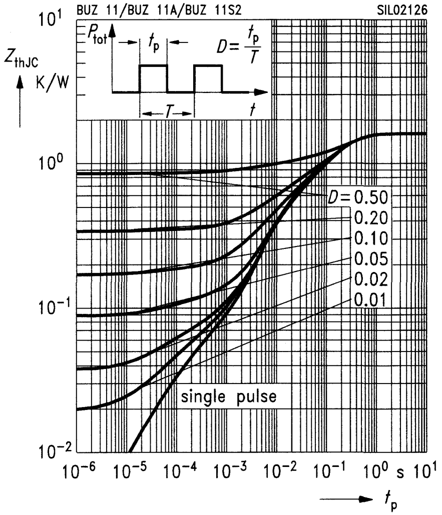
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: T_j , t_p = 80 µs,(spread)



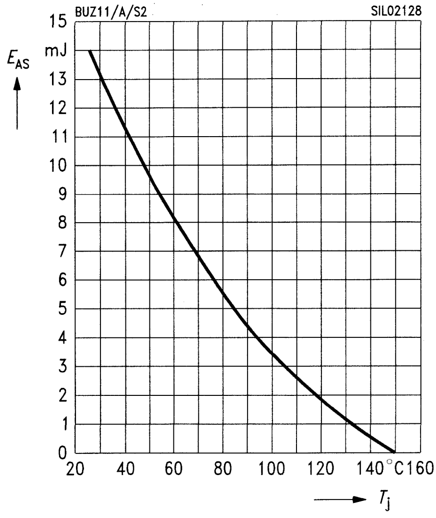
Transient thermal impedance

$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



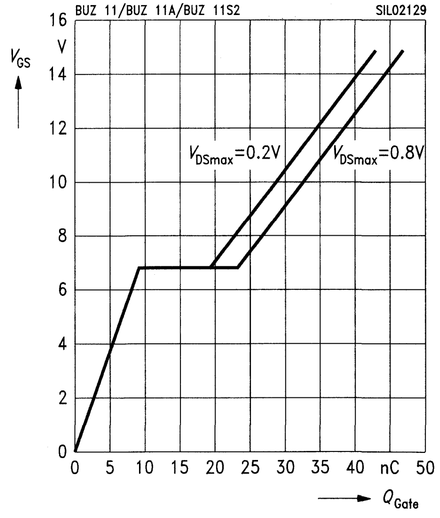
Avalanche energy $E_{AS} = f(T_j)$

parameter: I_D = 30 A, V_{DD} = 25 V
R_{GS} = 25 Ω, L = 15.6 µH



Typ. gate charge

$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls}$ = 55.5 A

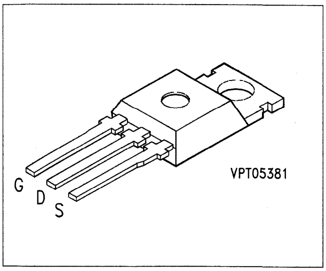


SIEMENS

SIPMOS® Power Transistor

BUZ 11 AL

- N channel
- Enhancement mode
- Logic Level
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\ (on)}$	Package [1]	Ordering Code
BUZ 11 AL	50 V	26 A	0.055 Ω	TO-220 AB	C67078-S1330-A3

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 25 ˚C	I_D	**26**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\ puls}$	**104**	
Avalanche current, limited by $T_{j\ max}$	I_{AR}	**26**	
Avalanche energy, periodic limited by $T_{j\ (max)}$	E_{AR}	**1.9**	mJ
Avalanche energy, single pulse I_D = 26 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 20.7 µH, T_j = 25 ˚C	E_{AS}	**14**	
Gate-source voltage	V_{GS}	**± 10**	V
Gate-source peak voltage, aperiodic	V_{gs}	**± 20**	
Power dissipation, T_C = 25 ˚C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\ JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	50		–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	1.5	2.0	2.5	
Zero gate voltage drain current V_{DS} = 50 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 ˚C		–	0.1	1.0	
T_j = 125 ˚C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 5 V, I_D = 13 A	$R_{DS\,(on)}$	–	0.040	0.055	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 13 A	g_{fs}	10	22	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1500	2000	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	580	840	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	190	300	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	25	40	ns
	t_r	–	80	120	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	110	160	
	t_f	–	80	110	

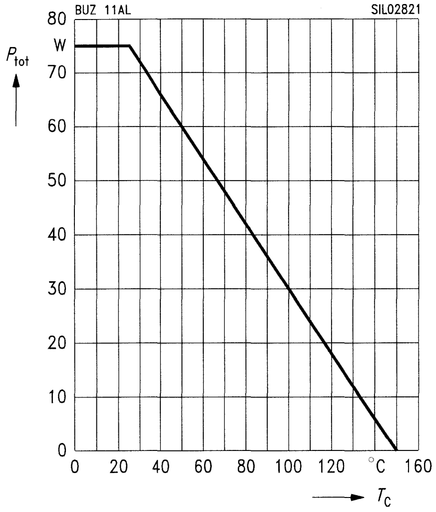
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C= 25 °C	I_S	–	–	26	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	104	
Diode forward on-voltage I_S = 52 A, V_{GS} = 0 V	V_{SD}	–	1.5	1.8	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	100	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.2	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

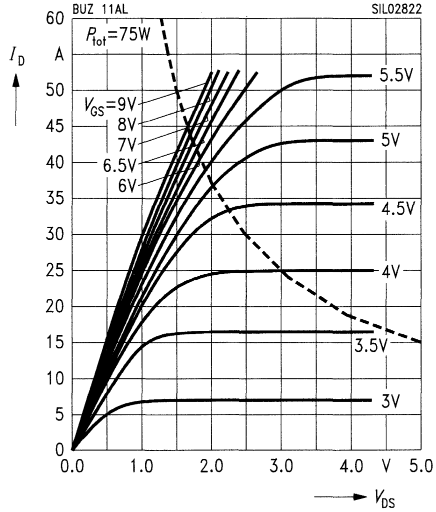
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

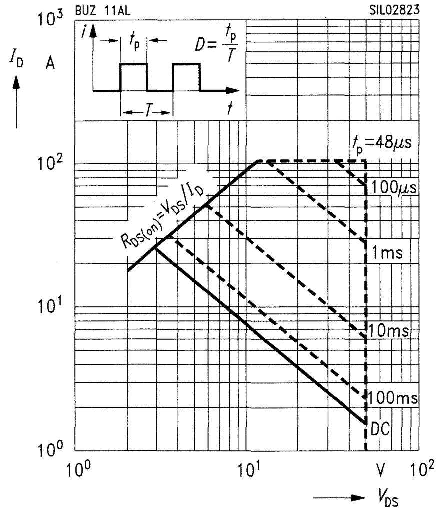
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

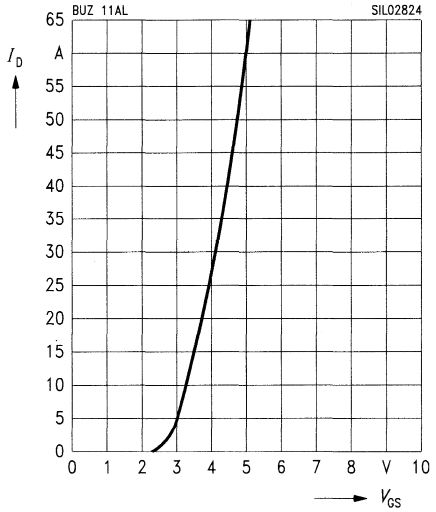
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

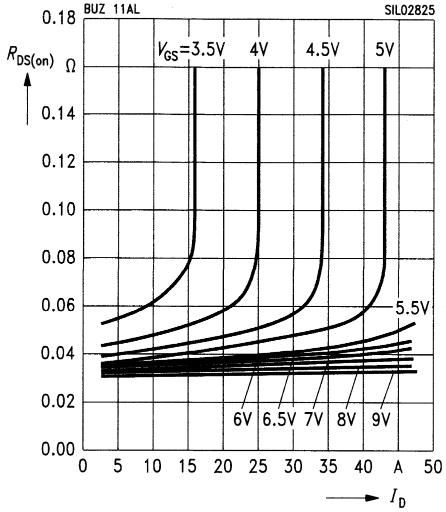
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



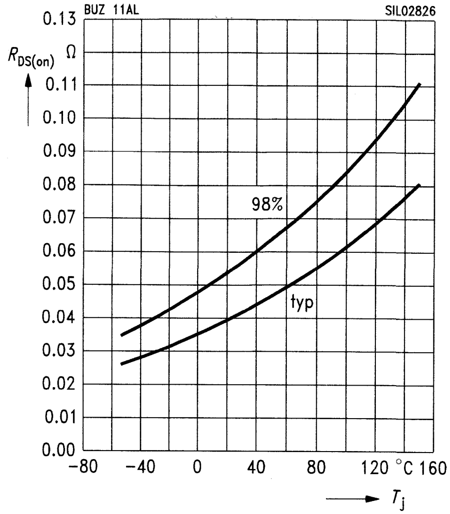
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$
parameter: V_{GS}



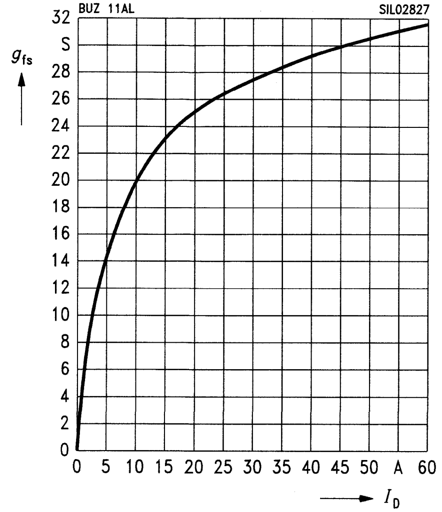
Drain-source on-resistance

$R_{DS(on)} = f(T_j)$
parameter: I_D = 13 A, V_{GS} = 5 V, (spread)



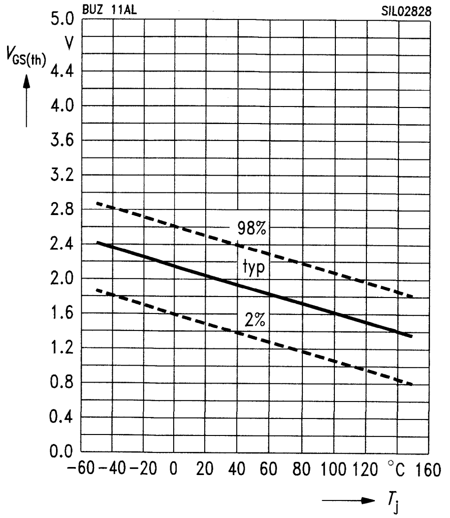
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

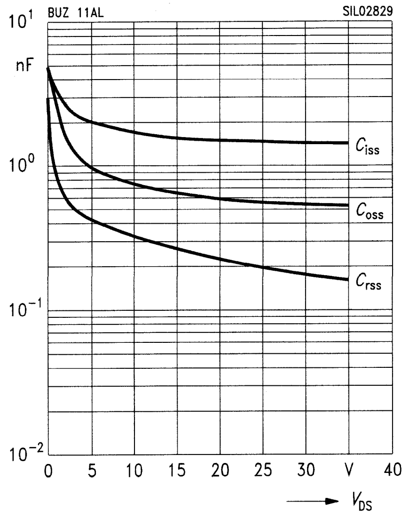
$V_{GS(th)} = f(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

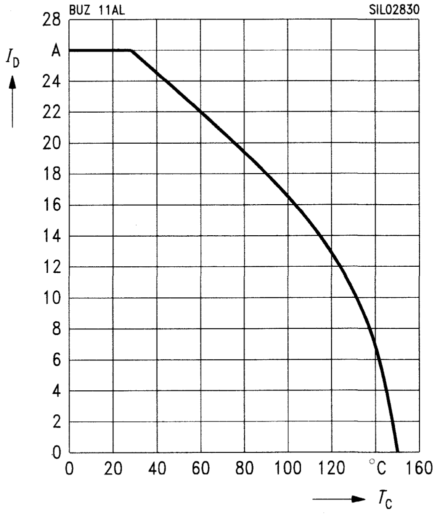
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

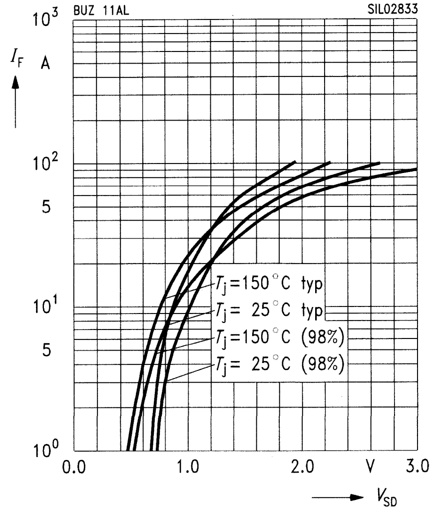
parameter: $V_{GS} \geq 5$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

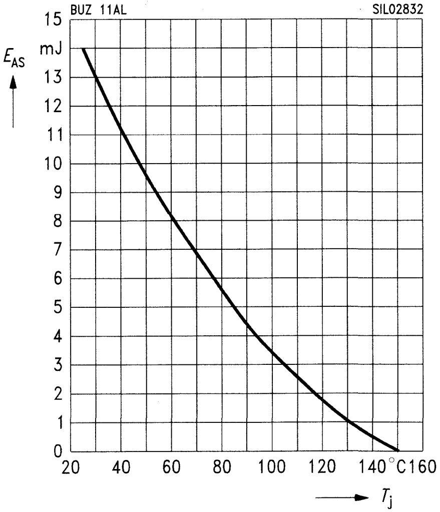
parameter: T_j , $t_p = 80$ µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

parameter: $I_D = 26$ A, $V_{DD} = 25$ V

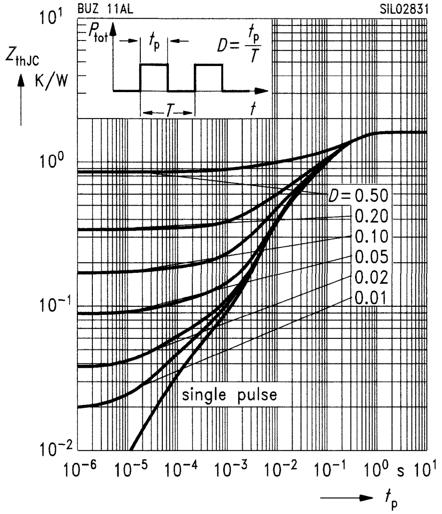
$R_{GS} = 25\ \Omega$, $L = 20.7\ \mu$H



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

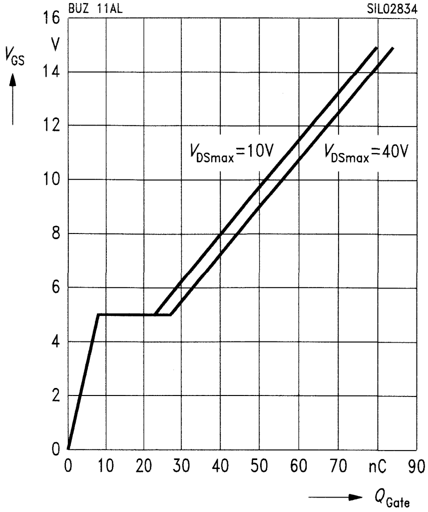
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{\text{Gate}})$

parameter: $I_{\text{D puls}}$ = 39 A

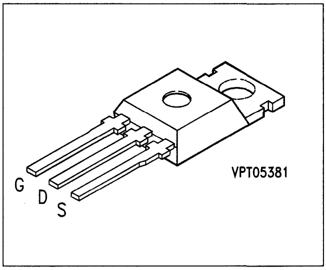


SIEMENS

SIPMOS® Power Transistors

BUZ 12
BUZ 12 A

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	T_C	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 12	50 V	42 A	65 ˚C	0.028 Ω	TO-220 AB	C67078-S1331-A2
BUZ 12 A	50 V	42 A	44 ˚C	0.035 Ω	TO-220 AB	C67078-S1331-A3

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current	I_D	**42**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**168**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**42**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**2.5**	mJ
Avalanche energy, single pulse I_D = 42 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 23.2 µH, T_j = 25 ˚C	E_{AS}	**41**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 ˚C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

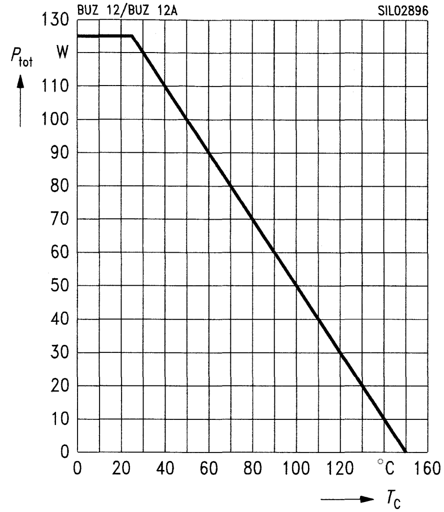
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	50	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 50 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS(on)}$				Ω
V_{GS} = 10 V, I_D = 32 A BUZ 12		–	0.024	0.028	
BUZ 12 A		–	0.030	0.035	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 32 A	g_{fs}	12.0	23.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1700	2300	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	800	1200	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	280	420	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	35	50	ns
	t_r	–	85	130	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	220	280	
	t_f	–	140	180	

Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

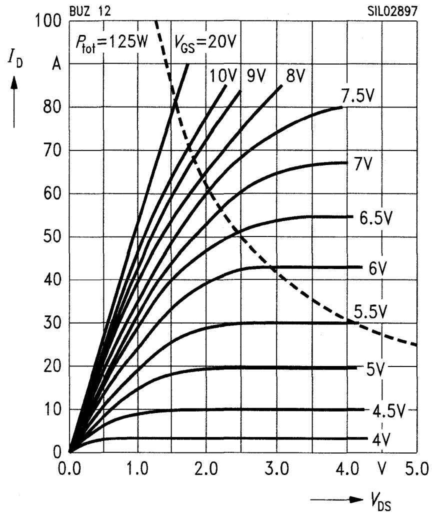
Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–		42	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–		168	
Diode forward on-voltage I_S = 84 A, V_{GS} = 0 V	V_{SD}	–	1.8	2.2	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	80	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.14	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

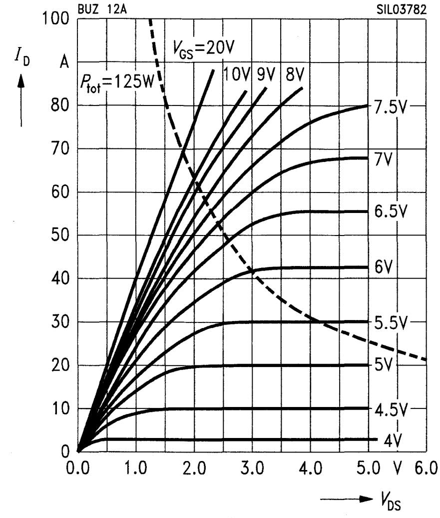
Total power dissipation
$P_{tot} = f(T_C)$



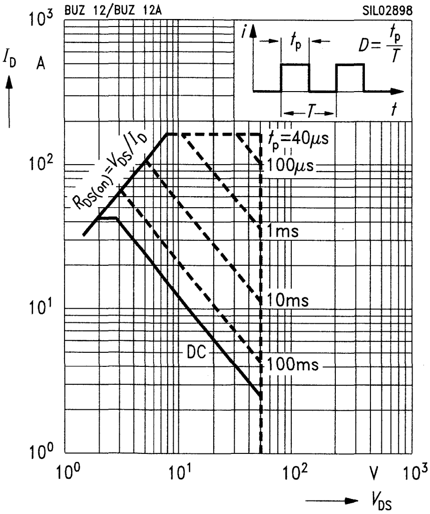
Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 12**
parameter: t_p = 80 µs



Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 12 A**
parameter: t_p = 80 µs

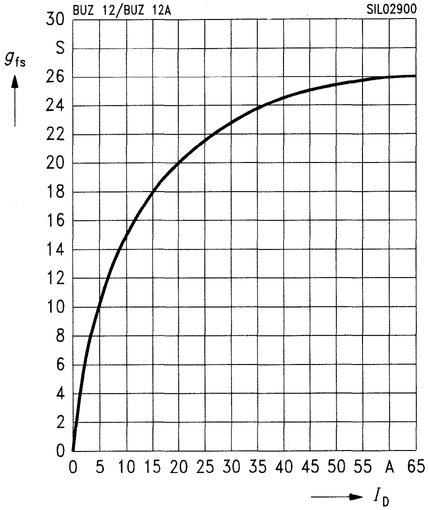


Safe operating area
$I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



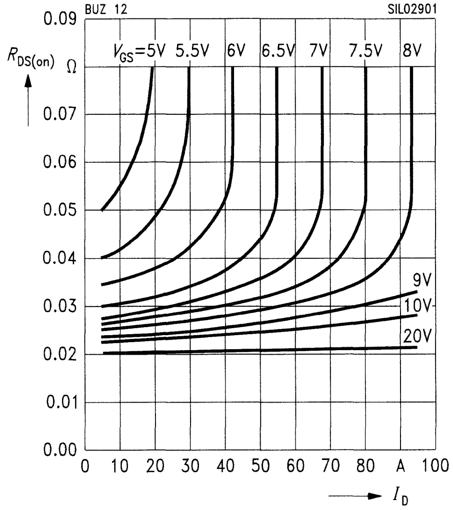
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: t_p = 80 µs



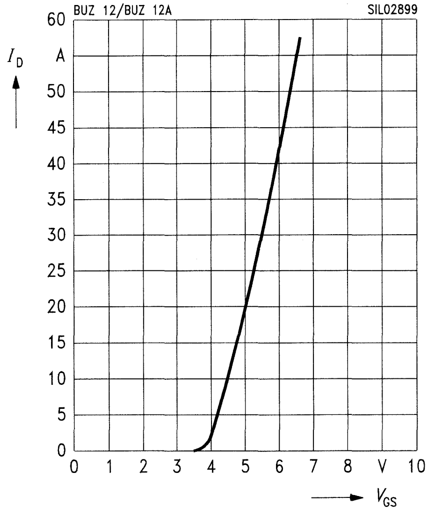
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 12**
parameter: V_{GS}



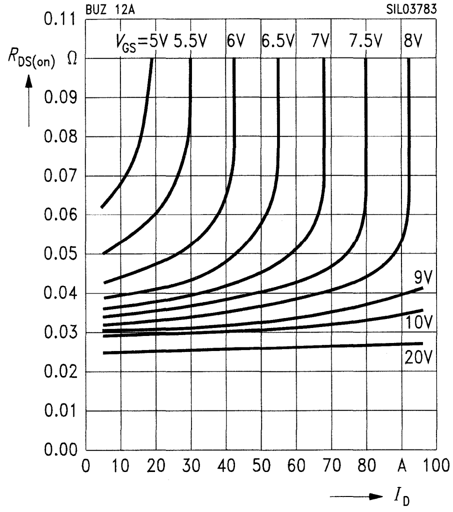
Typ. transfer characteristics

$I_D = f(V_{GS})$
parameter: t_p = 80 µs, V_{DS} = 25 V



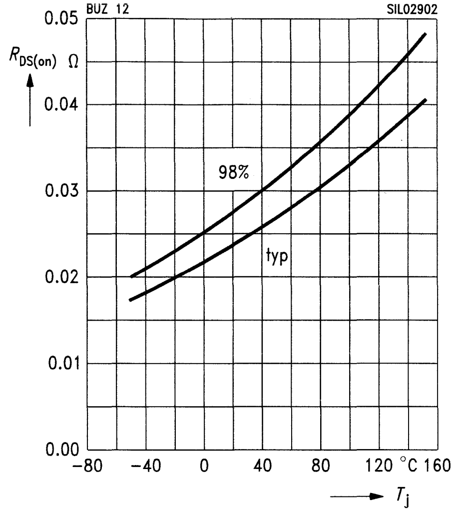
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 12 A**
parameter: V_{GS}



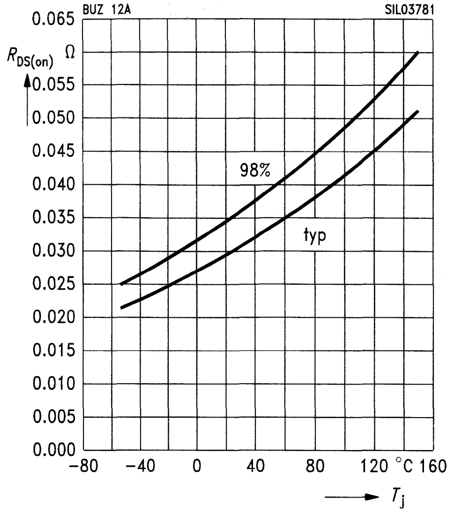
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 12**
parameter: I_D = 32 A, V_{GS} = 10 V, (spread)



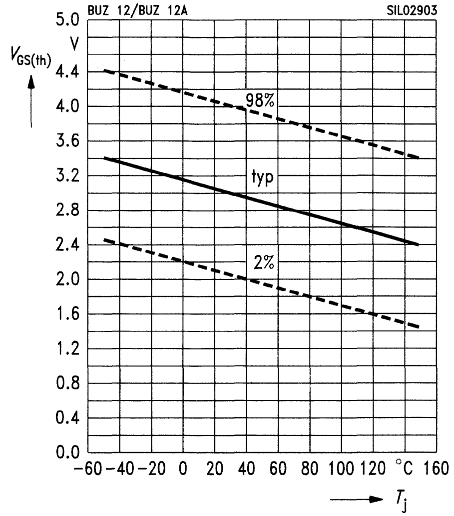
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 12 A**
parameter: I_D = 32 A, V_{GS} = 10 V, (spread)



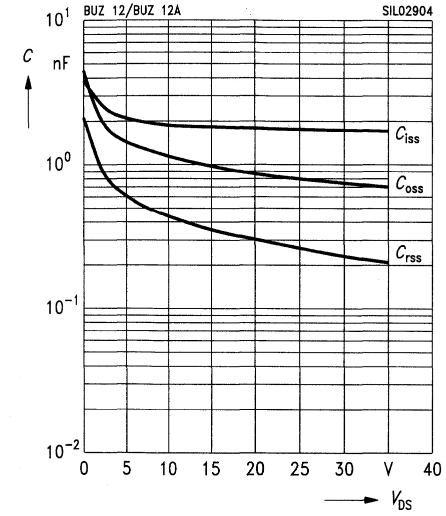
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



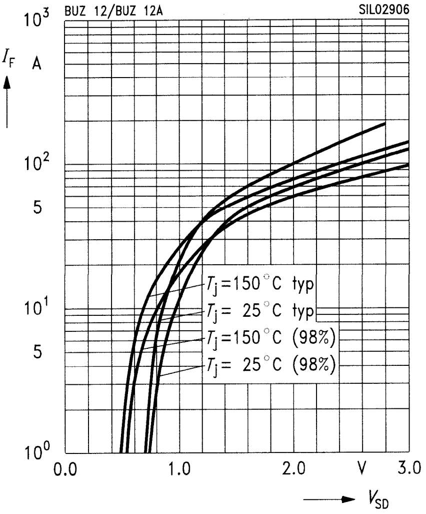
Typ. capacitances

$C = f\,(V_{DS})$
parameter: V_{GS} = 0 V, f = 1 MHz



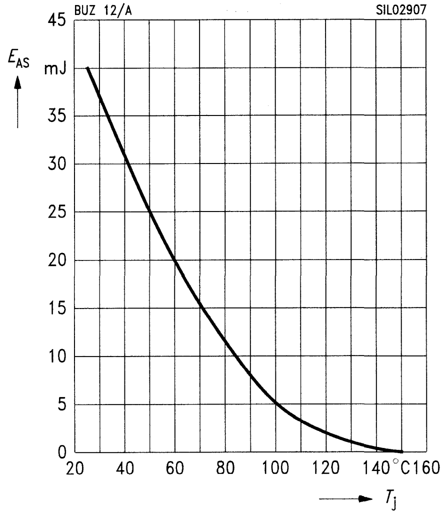
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: T_j, t_p = 80 µs, (spread)



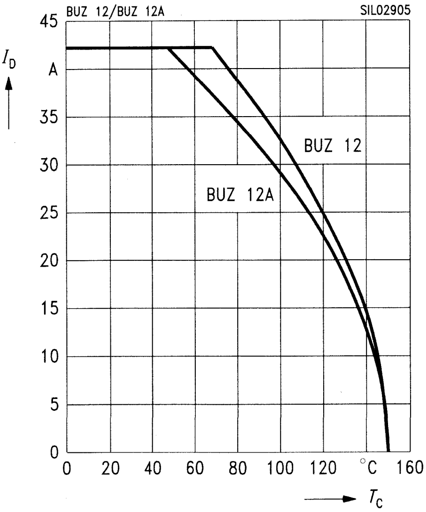
Avalanche energy $E_{AS} = f(T_j)$

parameter: I_D = 42 A, V_{DD} = 25 V
R_{GS} = 25 Ω, L = 23.2 µH



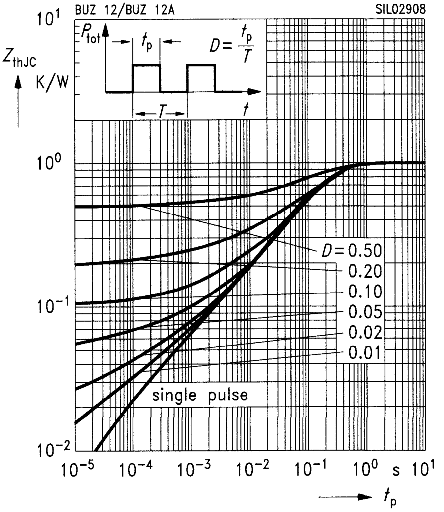
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq$ 10 V

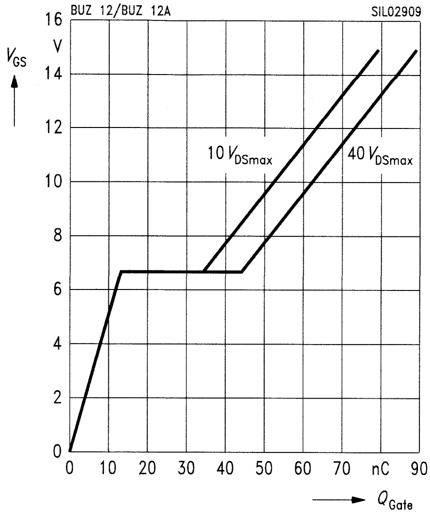


Transient thermal impedance

$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



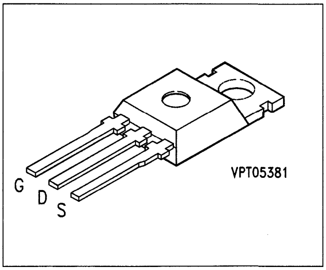
Typ. gate charge
$V_{GS} = f\,(Q_{Gate})$
parameter: $I_{D\,puls}$ = 63.0 A



SIPMOS® Power Transistor

BUZ 12 AL

- N channel
- Enhancement mode
- Logic Level
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 12 AL	50 V	42 A	0.035 Ω	TO-220 AB	C67078-S1332-A3

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 44 °C	I_D	**42**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**168**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**42**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**2.5**	mJ
Avalanche energy, single pulse I_D = 42 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 23.2 µH, T_j = 25 °C	E_{AS}	**41**	
Gate-source voltage	V_{GS}	**10**	V
Gate-source peak voltage, aperiodic	V_{gs}	**± 20**	
Power dissipation, T_C = 25 °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

Static characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	50	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	1.5	2.0	2.5	
Zero gate voltage drain current V_{DS} = 50 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	1.0	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 5 V, I_D = 21 A	$R_{DS(on)}$	–	0.030	0.035	Ω

Dynamic characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 21 A	g_{fs}	16.0	30.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	2100	2800	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	800	1200	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	280	450	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	45	60	ns
	t_r	–	160	240	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	270	350	
	t_f	–	160	200	

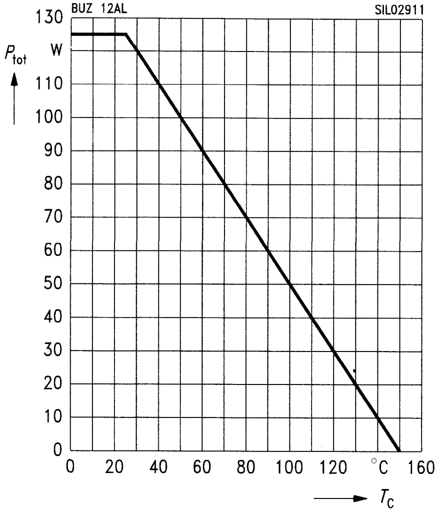
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	42	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	168	
Diode forward on-voltage I_S = 84 A, V_{GS} = 0 V	V_{SD}	–	1.8	2.2	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	200	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.25	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Total power dissipation

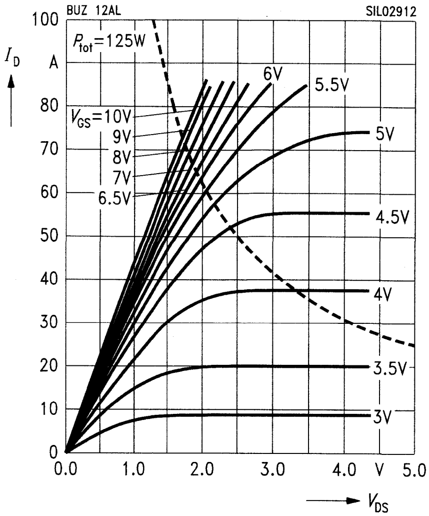
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

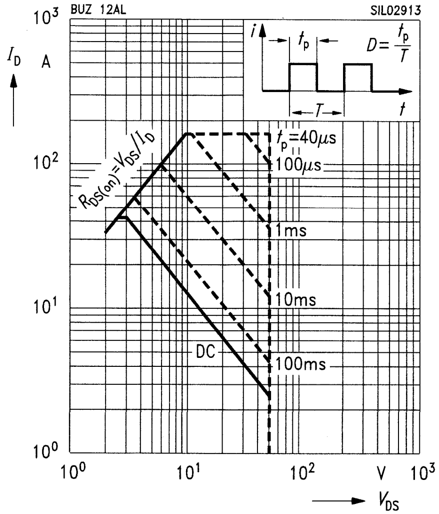
parameter: $t_p = 80$ µs



Safe operating area

$I_D = f(V_{DS})$

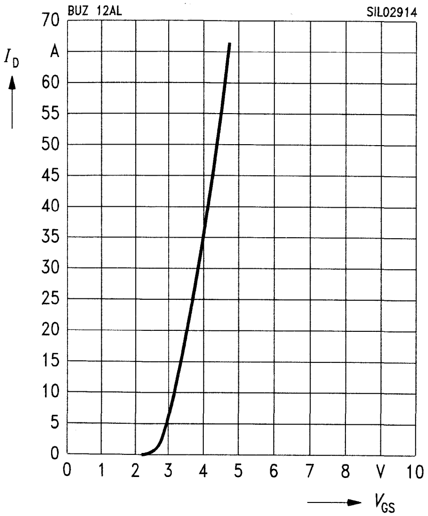
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

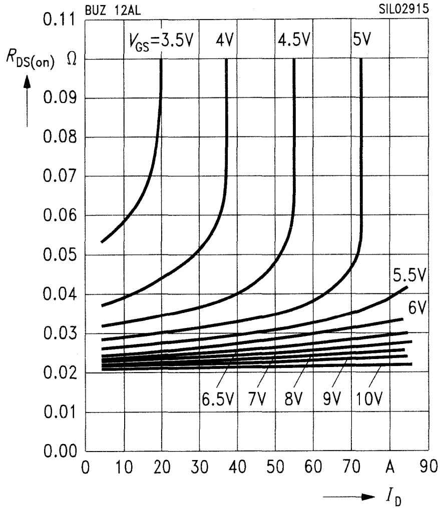
$I_D = f(V_{GS})$

parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



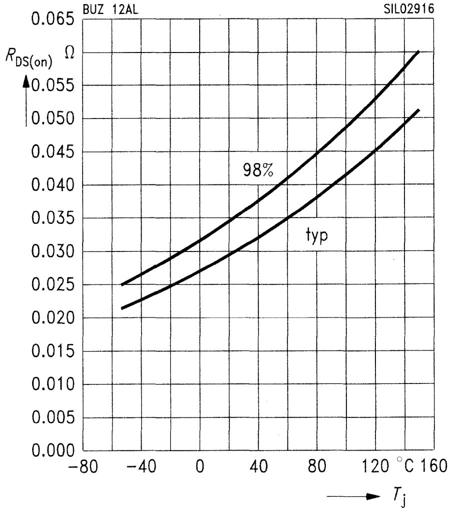
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



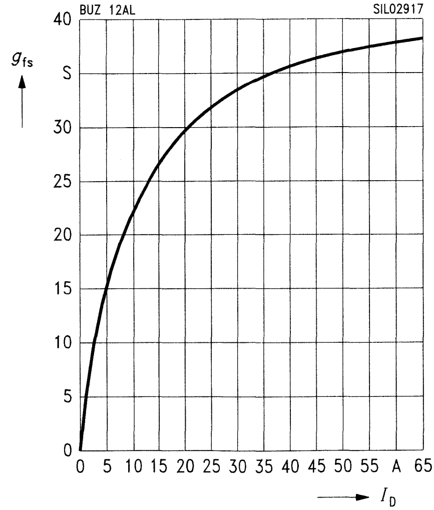
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 21 A, V_{GS} = 5 V, (spread)



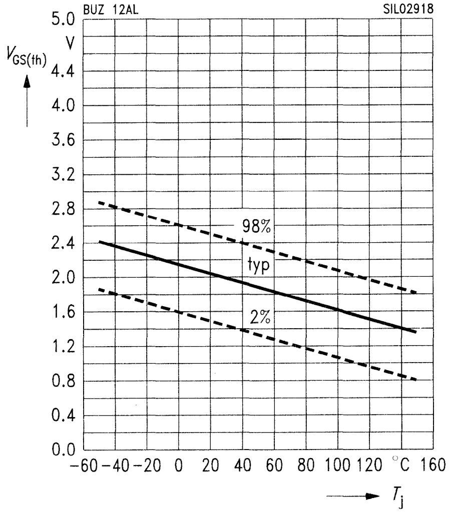
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

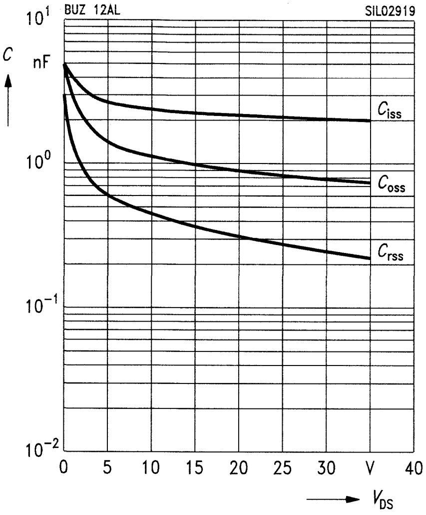
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

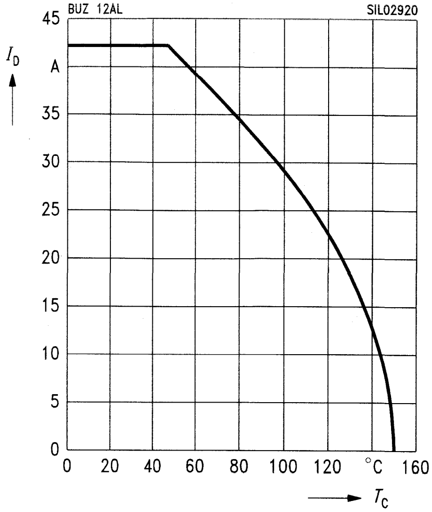
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

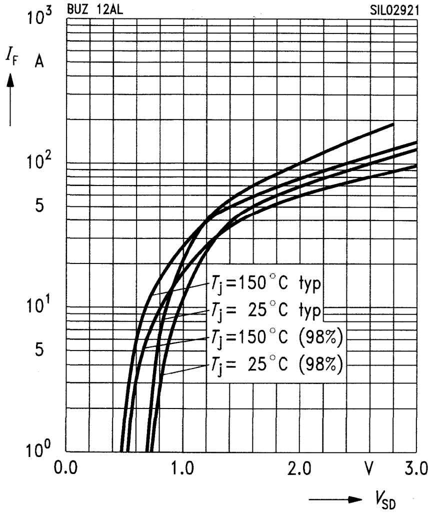
parameter: $V_{GS} \geq 5$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

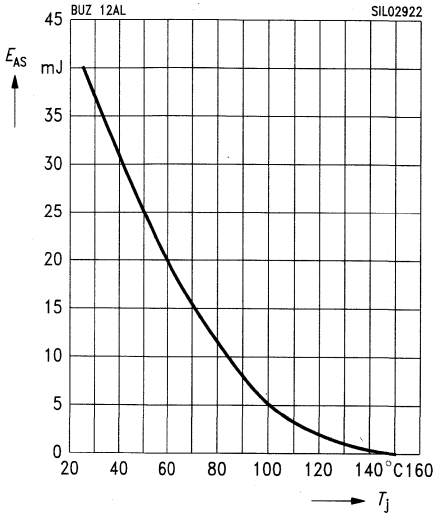
parameter: T_j , $t_p = 80$ µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

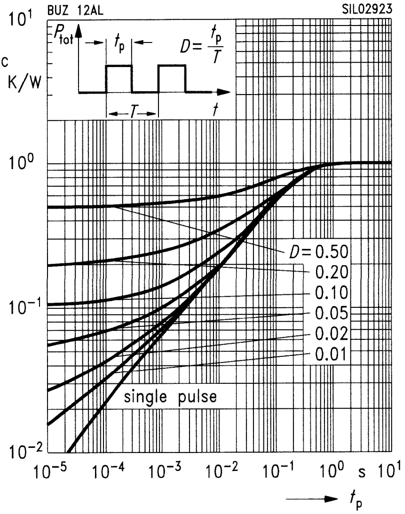
parameter: $I_D = 42$ A, $V_{DD} = 25$ V

$R_{GS} = 50\ \Omega$, $L = 23.2$ µH



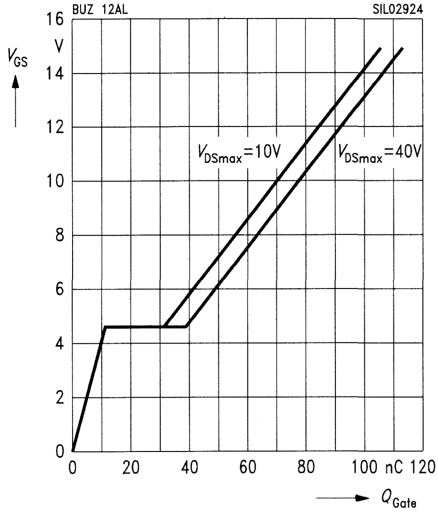
Transient thermal impedance

$Z_{th\ JC} = f(t_p)$
parameter: $D = t_p / T$



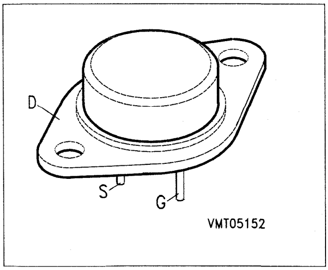
Typ. gate charge

$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 63$ A



SIPMOS® Power Transistor **BUZ 15**

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 15	50 V	45 A	0.03 Ω	TO-204 AE	C67078-S1001-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 28 °C	I_D	**45**	A
Pulsed drain current, T_C = 25°C	$I_{D\,puls}$	**180**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**45**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**2.5**	mJ
Avalanche energy, single pulse I_D = 42 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 20.2 µH, T_j = 25 °C	E_{AS}	**41**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040	–	**C**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

Static characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	50	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 50 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 ˚C		–	0.1	1.0	
T_j = 125 ˚C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 29 A	$R_{DS\,(on)}$	–	0.025	0.030	Ω

Dynamic characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 29 A	g_{fs}	7.0	22.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1800	2400	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	800	1200	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	280	450	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	35	50	ns
	t_r	–	85	130	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	220	280	
	t_f	–	140	180	

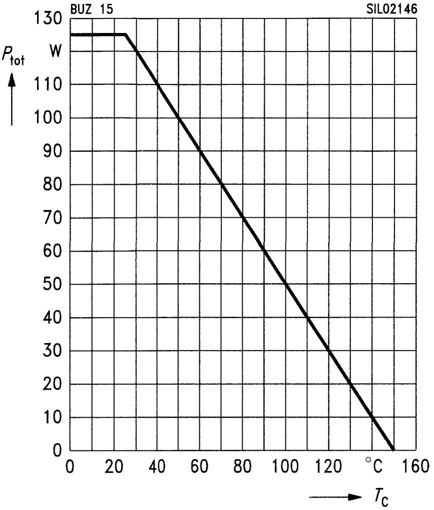
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	45	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	180	
Diode forward on-voltage I_S = 90 A, V_{GS} = 0 V	V_{SD}	–	1.8	2.2	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	80	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.14	–	µC

Characteristics at $T_j = 25\ ^\circ\text{C}$, unless otherwise specified.

Total power dissipation

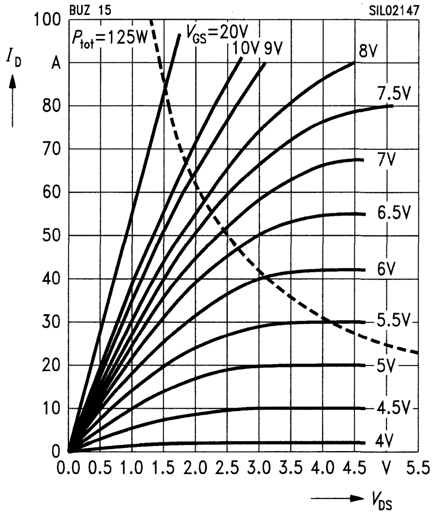
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

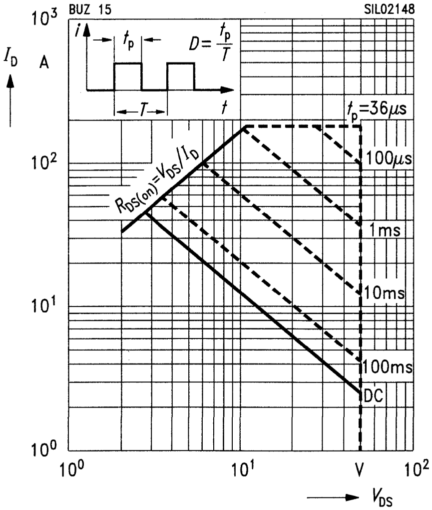
parameter: $t_p = 80\ \mu s$



Safe operating area

$I_D = f(V_{DS})$

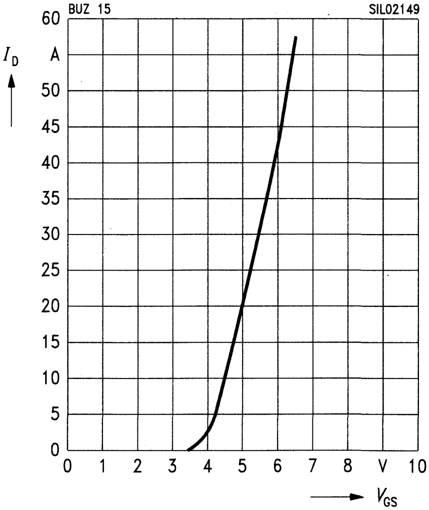
parameter: $D = 0.01$, $T_C = 25\ ^\circ\text{C}$



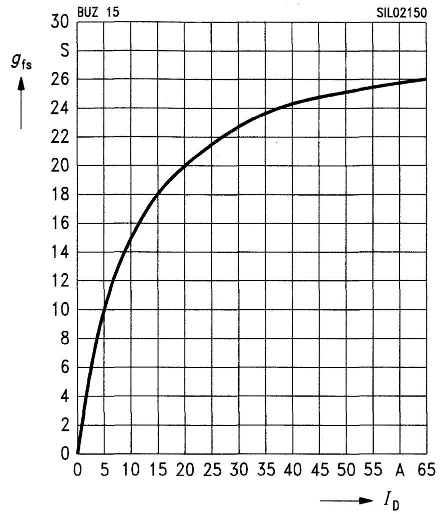
Typ. transfer characteristics

$I_D = f(V_{GS})$

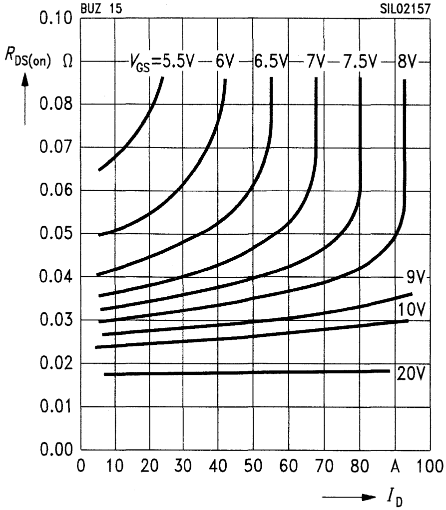
parameter: $t_p = 80\ \mu s$, $V_{DS} = 25$ V



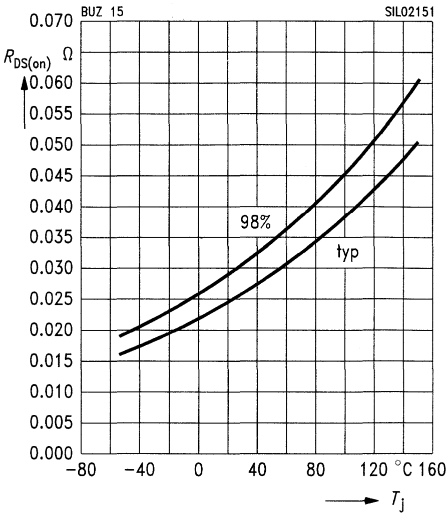
Typ. forward transconductance
$g_{fs} = f(I_D)$
parameter: $t_p = 80\ \mu s$



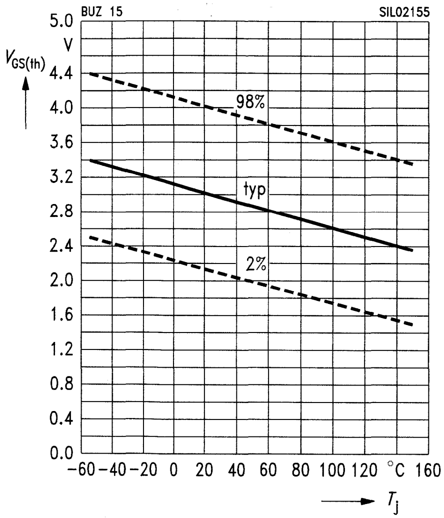
Typ. drain-source on-resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}



Drain-source on-resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 29 A, V_{GS} = 10 V, (spread)



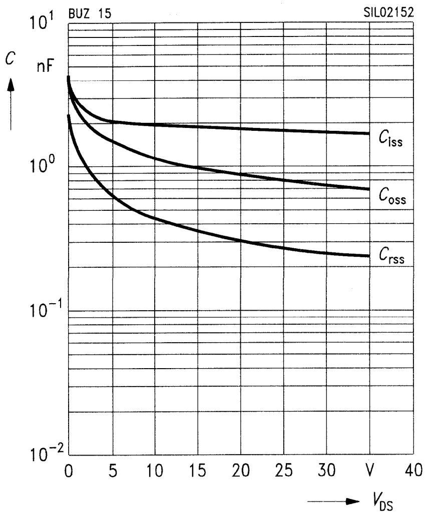
Gate threshold voltage
$V_{GS(th)} = f(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

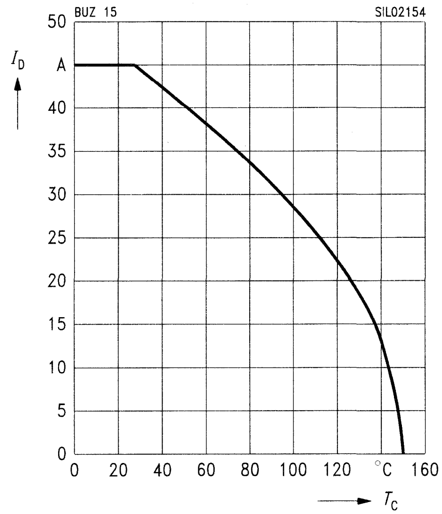
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

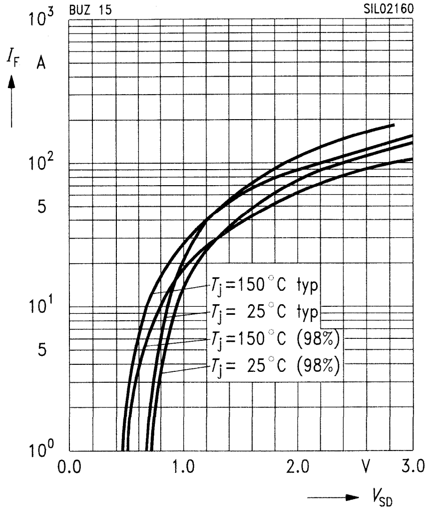
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

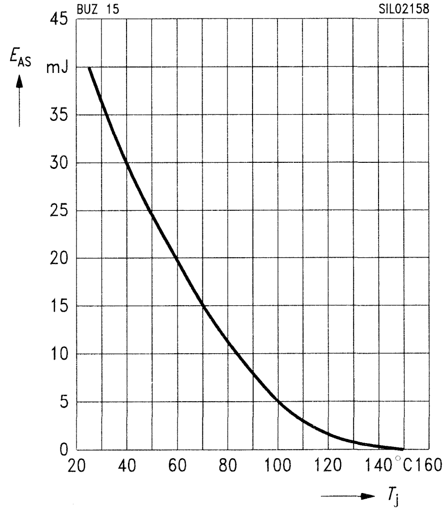
parameter: T_j, $t_p = 80$ µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

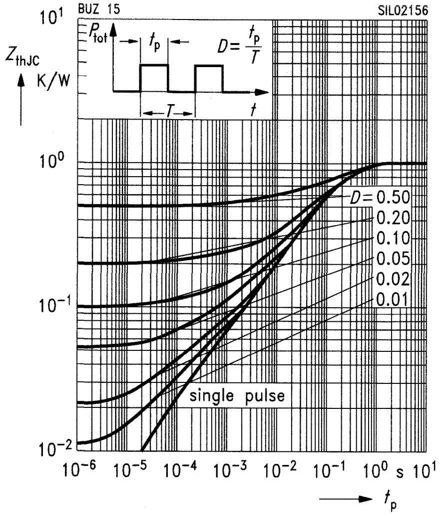
parameter: $I_D = 45$ A, $V_{DD} = 25$ V

$R_{GS} = 25\ \Omega$, $L = 20.2$ µH



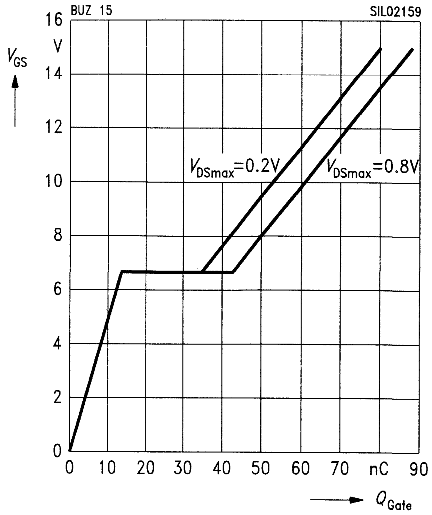
Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

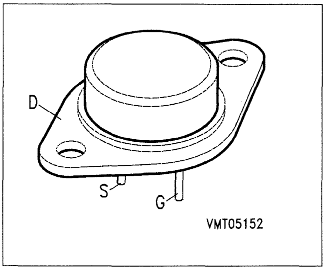
$V_{GS} = f(Q_{Gate})$
parameter: $I_{\text{D puls}}$ = 63.0 A



SIPMOS® Power Transistors

BUZ 16
BUZ 16 S2

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 16	50 V	48 A	0.018 Ω	TO-204 AE	C67078-S1020-A2
BUZ 16 S2	60 V	48 A	0.018 Ω	TO-204 AE	C67078-S1020-A3

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current , T_C = 79 °C	I_D	**48**	A
Pulsed drain current, T_C = 25°C	$I_{D\,puls}$	**192**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**48**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**4.5**	mJ
Avalanche energy, single pulse V_{DD} = 25 V, R_{GS} = 25 Ω, T_j = 25 °C I_D = 48 A, L = 31.3 µH	E_{AS}	**72**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040	–	**C**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

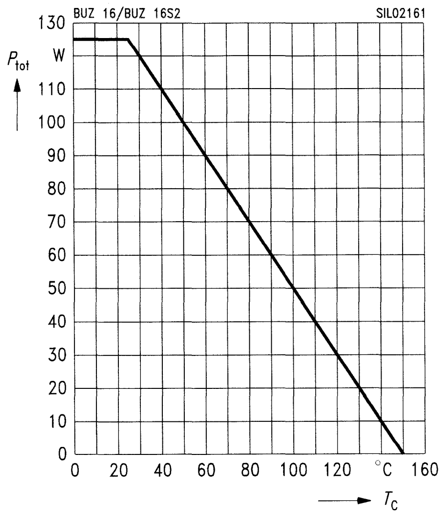
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA BUZ 16 BUZ 16 S2	$V_{(BR)\,DSS}$	 50 60	 – –	 – –	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{GS} = 0 V, V_{DS} = 50 V BUZ 16 V_{GS} = 0 V, V_{DS} = 60 V BUZ 16 S2 T_j = 25 °C T_j = 125 °C	I_{DSS}	 – –	 0.1 10	 1.0 100	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 40 A	$R_{DS\,(on)}$	–	0.012	0.018	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$ I_D = 40 A	g_{fs}	30	40	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	2900	4300	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	1400	2100	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	500	750	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	55	80	ns
	t_r	–	140	210	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	420	560	
	t_f	–	250	330	

Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

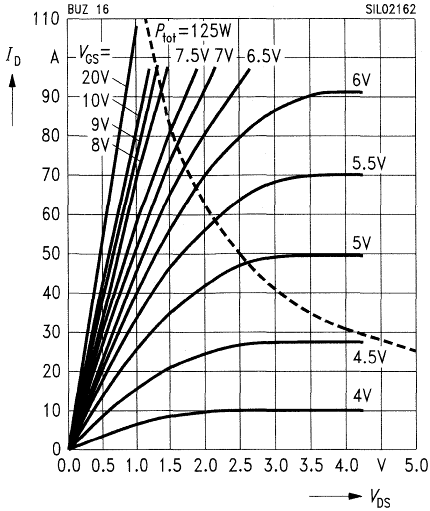
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	48	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	192	
Diode forward on-voltage I_S = 96 A, V_{GS} = 0 V	V_{SD}	–	1.6	2.0	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	100	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.3	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

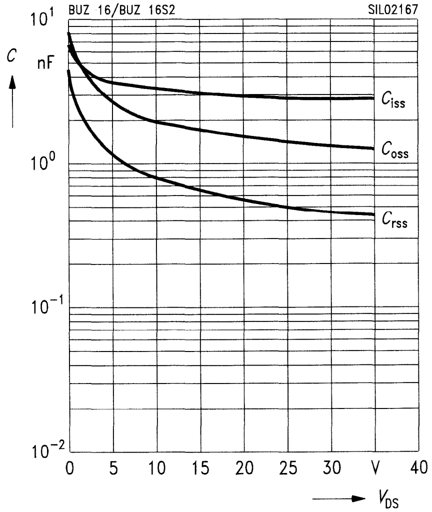
Total power dissipation
$P_{tot} = f(T_C)$



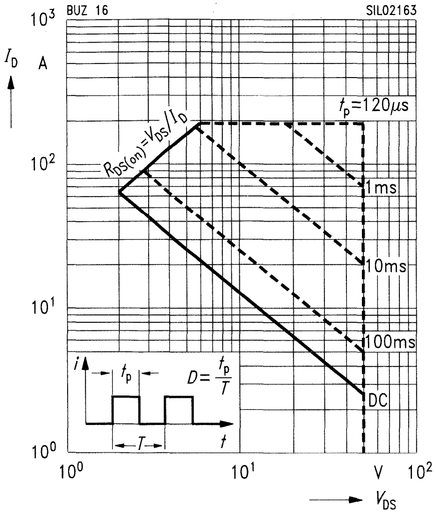
Typ. output characteristics
$I_D = f(V_{DS})$
parameter: t_p = 80 µs
BUZ 16



Typ. output characteristics
$I_D = f(V_{DS})$
parameter: t_p = 80 µs
BUZ 16 S2

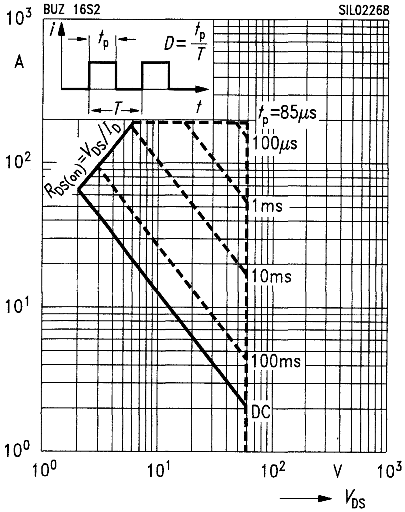


Safe operating area
$I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C
BUZ 16



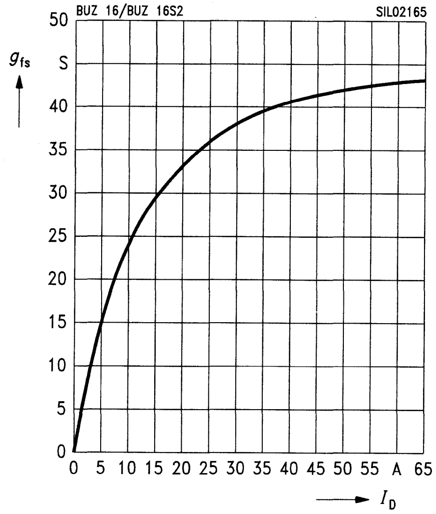
Safe operating area

$I_D = f(V_{DS})$ **BUZ 16 S2**
parameter: $D = 0.01$, $T_C = 25$ °C



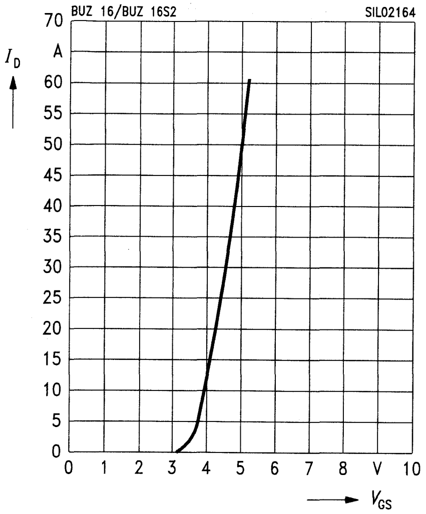
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: $t_p = 80$ µs



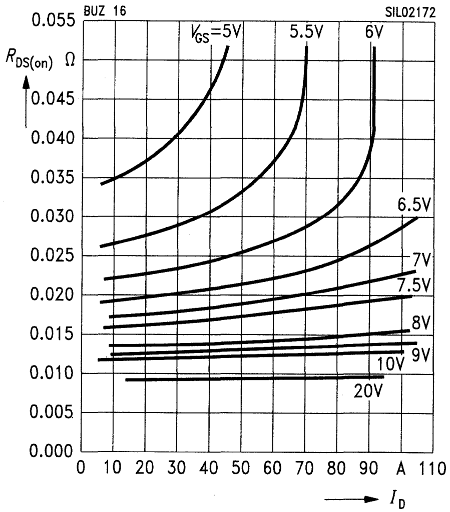
Typ. transfer characteristics

$I_D = f(V_{GS})$
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



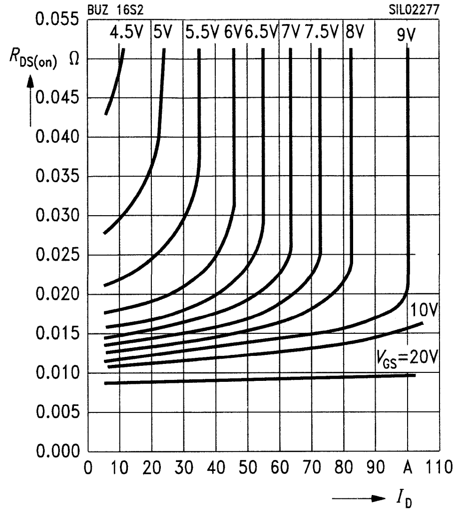
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 16**
parameter: V_{GS}



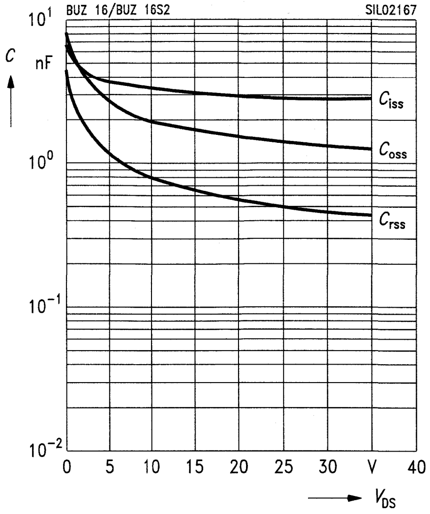
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 16 S2**
parameter: V_{GS}



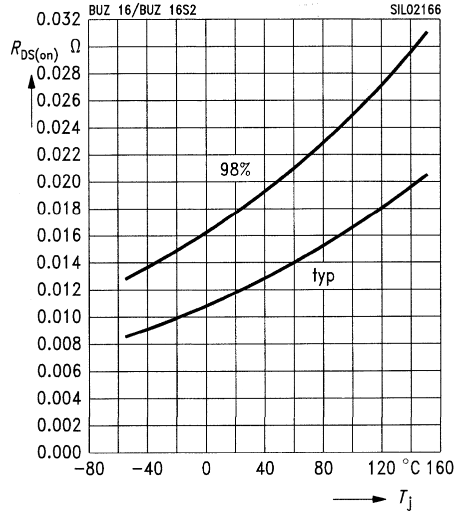
Typ. capacitances

$C = f\,(V_{DS})$
parameter: V_{GS} = 0 V, f = 1 MHz



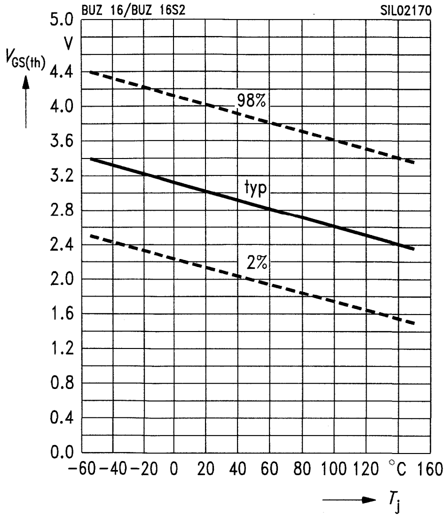
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 40 A, V_{GS} = 10 V, (spread)

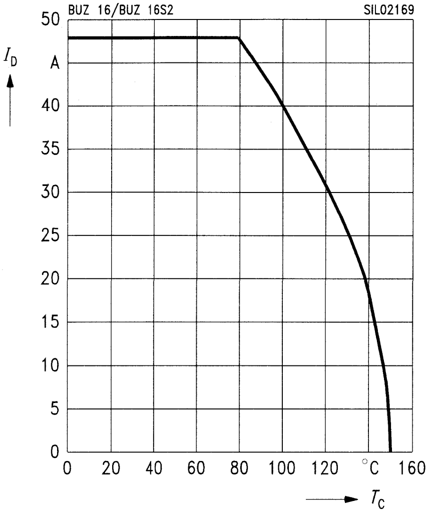


Gate threshold voltage

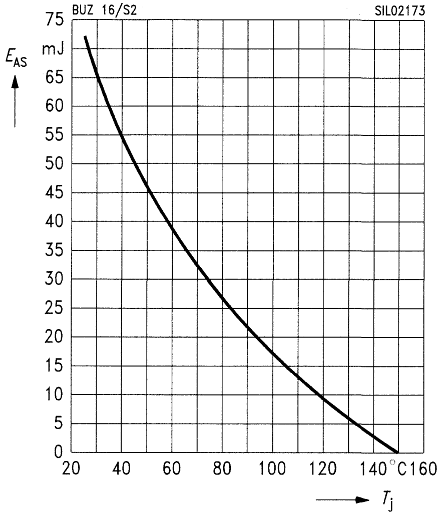
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



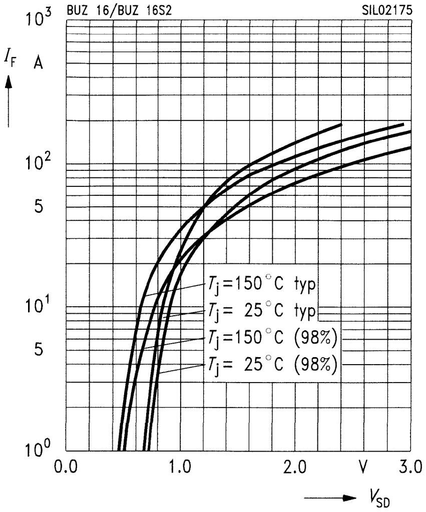
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



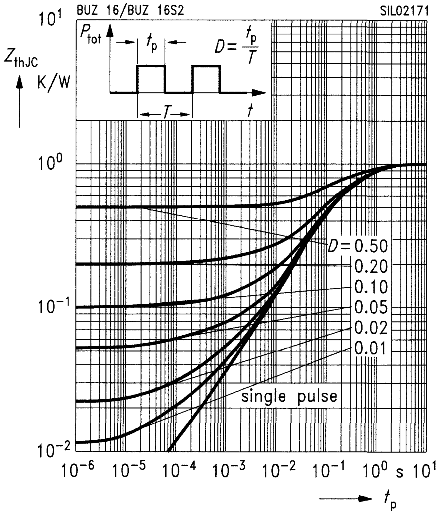
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 48$ A, $V_{DD} = 25$ V
$R_{GS} = 25\ \Omega$, $L = 31.3\ \mu$H



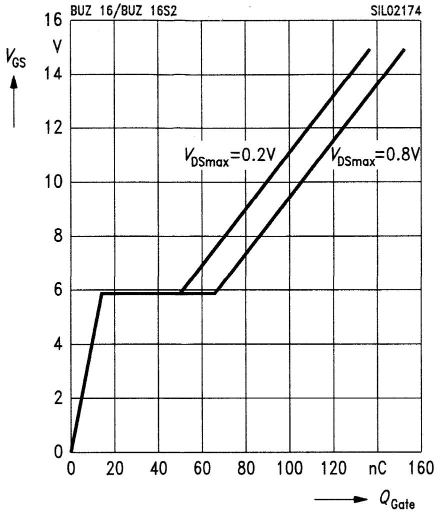
Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j , $t_p = 80\ \mu$s,(spread)



Transient thermal impedance
$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



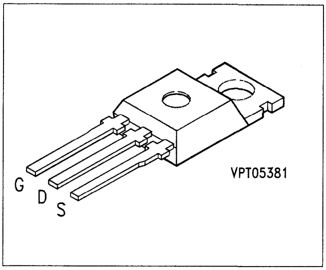
Typ. gate charge
$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls}$ = 87.0 A



SIPMOS® Power Transistor

BUZ 20

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 20	100 V	13.5 A	0.2 Ω	TO-220 AB	C67078-S1302-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 28 ˚C	I_D	**13.5**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\ puls}$	**54**	
Avalanche current, limited by $T_{j\ max}$	I_{AR}	**13.5**	
Avalanche energy, periodic limited by $T_{j\ (max)}$	E_{AR}	**7.9**	mJ
Avalanche energy, single pulse I_D = 13.5 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 486 µH, T_j = 25 ˚C	E_{AS}	**59**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 ˚C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\ JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	100	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 100 V, V_{GS} = 0 V T_j = 25 °C T_j = 125 °C	I_{DSS}	 – –	 0.1 10	 1.0 100	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 8.5 A	$R_{DS\,(on)}$	–	0.125	0.2	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 8.5 A	g_{fs}	3.0	4.7	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	400	530	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	120	180	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	70	105	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	10	15	ns
	t_r	–	45	70	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	55	75	
	t_f	–	40	55	

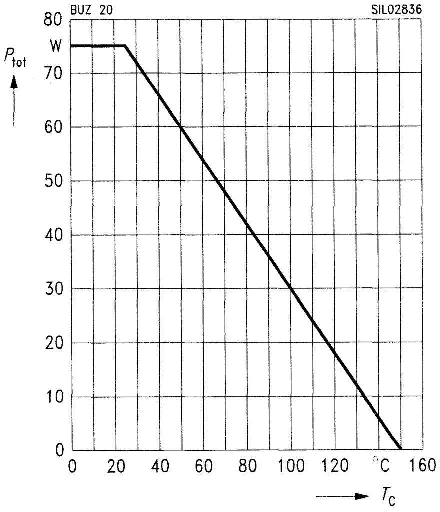
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C= 25 ˚C	I_S	–	–	13.5	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	54	
Diode forward on-voltage I_S = 27 A, V_{GS} = 0 V	V_{SD}	–	1.4	1.6	V
Reverse recovery time V_R = 30 V, I_F = I_S , di_F / dt = 100 A/µs	t_{rr}	–	170	–	ns
Reverse recovery charge V_R = 30 V, I_F = I_S , di_F / dt = 100 A/µs	Q_{rr}	–	0.30	–	µC

Characteristics at T_j = 25 ˚C, unless otherwise specified.

Total power dissipation

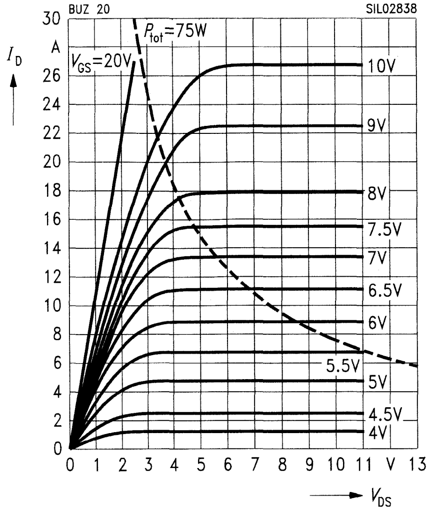
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

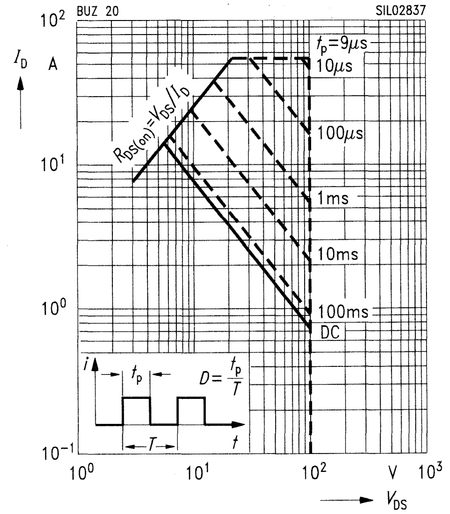
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

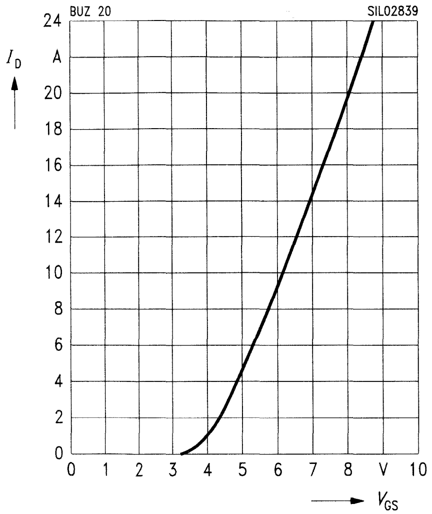
parameter: D = 0.01, T_C = 25 ˚C



Typ. transfer characteristics

$I_D = f(V_{GS})$

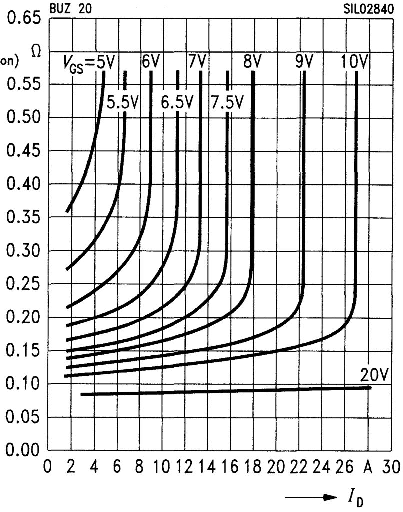
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS\ (on)} = f\ (I_D)$

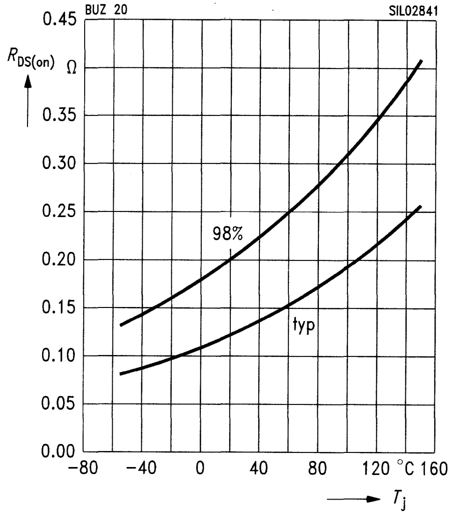
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\ (on)} = f\ (T_j)$

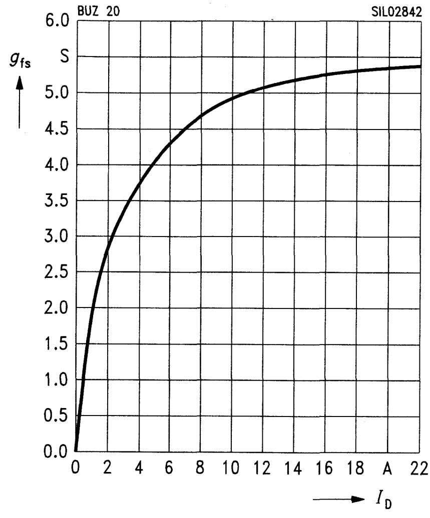
parameter: I_D = 8.5 A, V_{GS} = 10 V, (spread)



Typ. forward transconductance

$g_{fs} = f\ (I_D)$

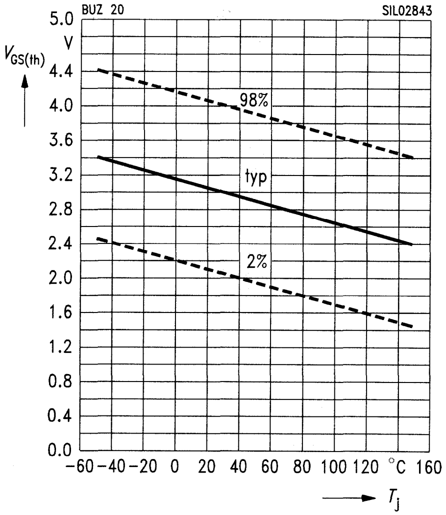
parameter: t_p = 80 µs



Gate threshold voltage

$V_{GS\ (th)} = f\ (T_j)$

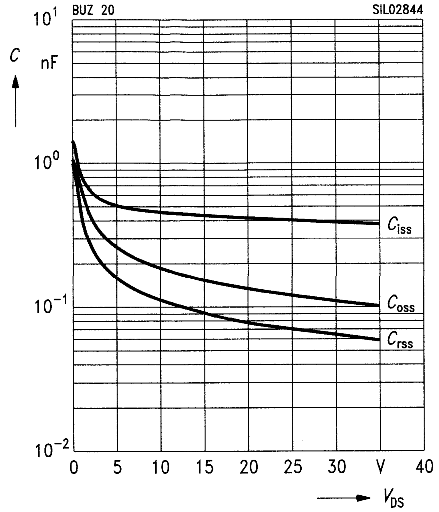
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

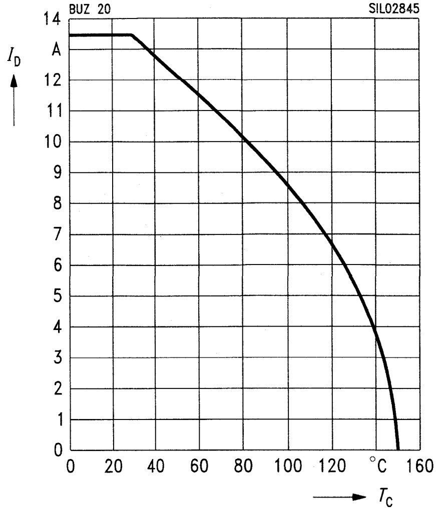
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

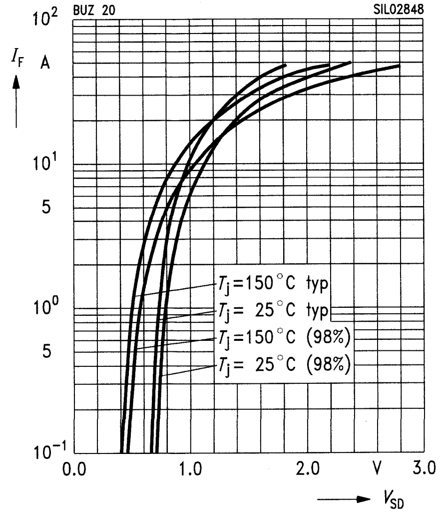
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

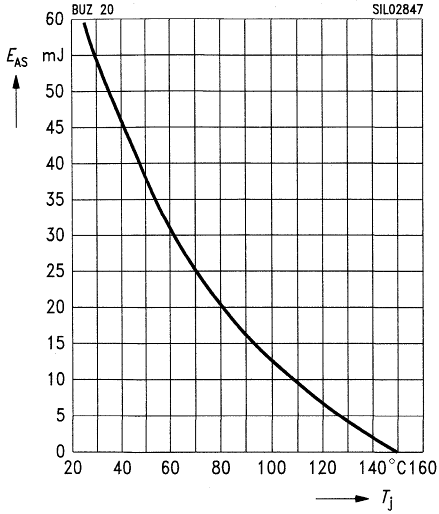
parameter: T_j , $t_p = 80$ µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

parameter: $I_D = 13.5$ A, $V_{DD} = 25$ V

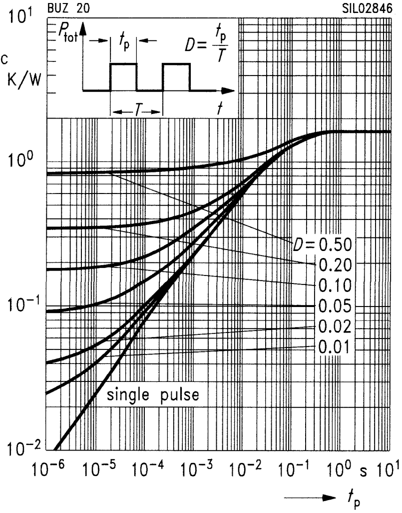
$R_{GS} = 25\ \Omega$, $L = 486$ µH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

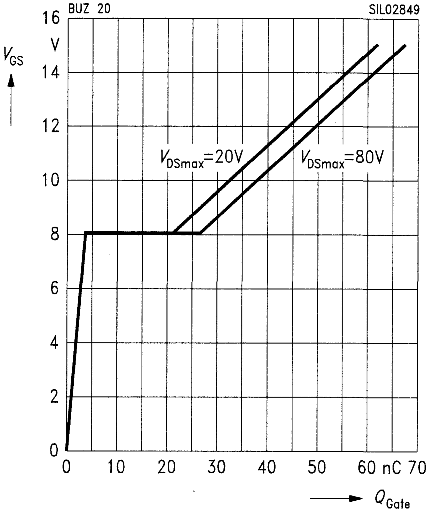
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{\text{Gate}})$

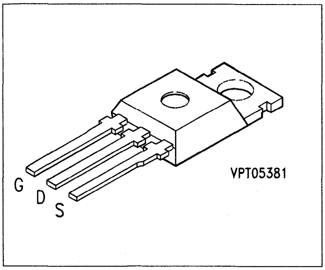
parameter: $I_{\text{D puls}} = 21.0$ A



SIPMOS® Power Transistor

BUZ 21

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 21	100 V	21 A	0.085 Ω	TO-220 AB	C67078-S1308-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 25 °C	I_D	**21**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**84**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**21**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**11**	mJ
Avalanche energy, single pulse I_D = 21 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 340 µH, T_j = 25 °C	E_{AS}	**100**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	100	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 100 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 13 A	$R_{DS(on)}$	–	0.065	0.085	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 13 A	g_{fs}	8	11	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1000	1300	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	300	530	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	150	240	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	25	40	ns
	t_r	–	50	75	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	160	210	
	t_f	–	80	110	

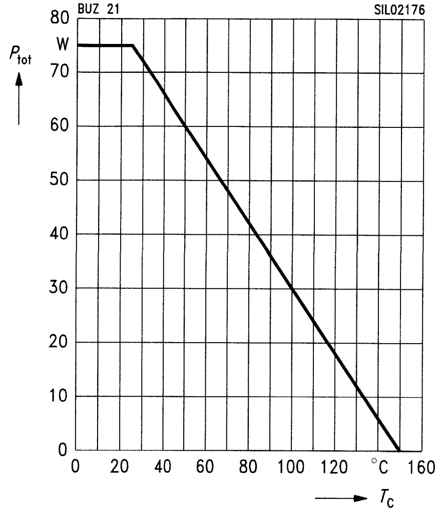
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	21	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	84	
Diode forward on-voltage I_S = 42 A, V_{GS} = 0 V	V_{SD}	–	1.3	1.7	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	150	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.48	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

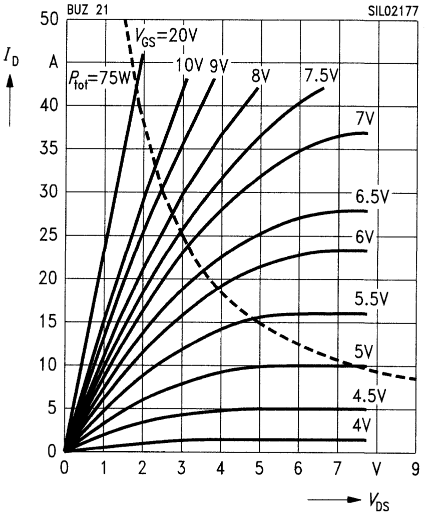
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

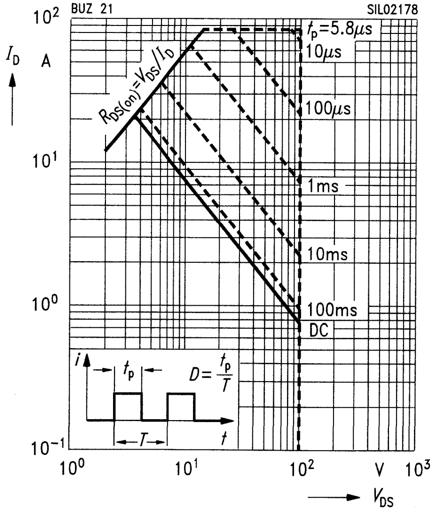
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

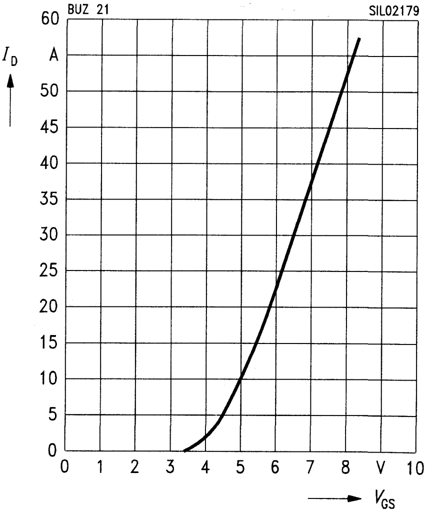
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

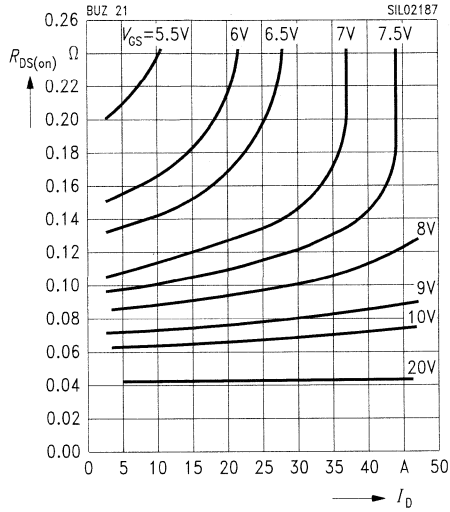
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

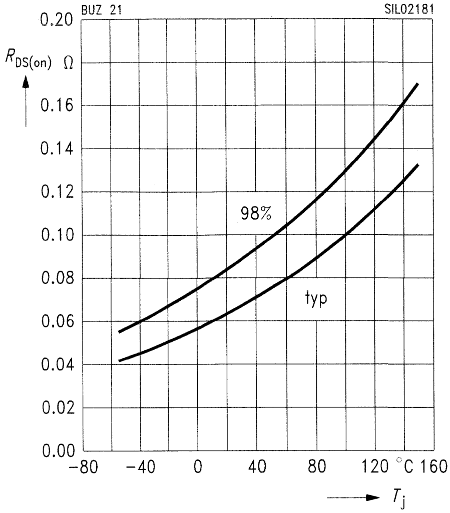
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

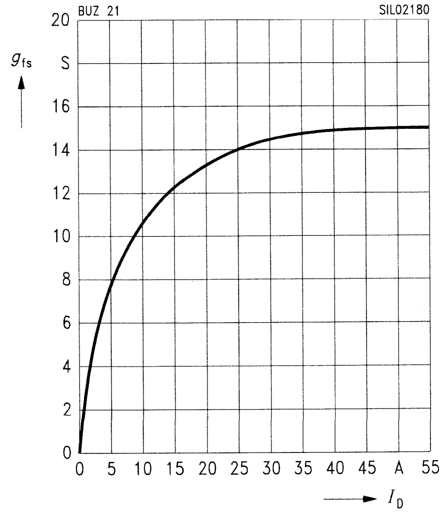
parameter: I_D = 13 A, V_{GS} = 10 V, (spread)



Typ. forward transconductance

$g_{fs} = f\,(I_D)$

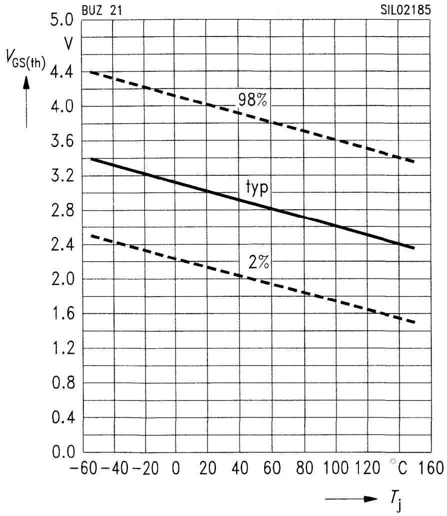
parameter: t_p = 80 µs



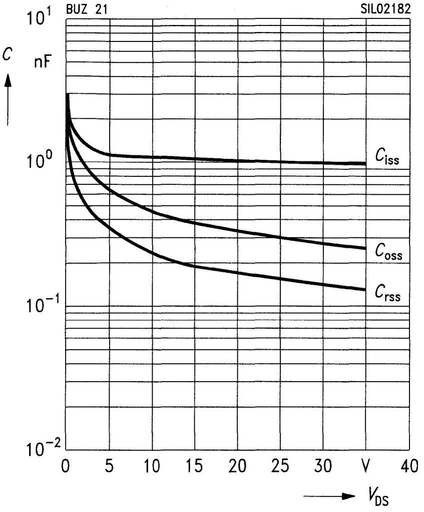
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

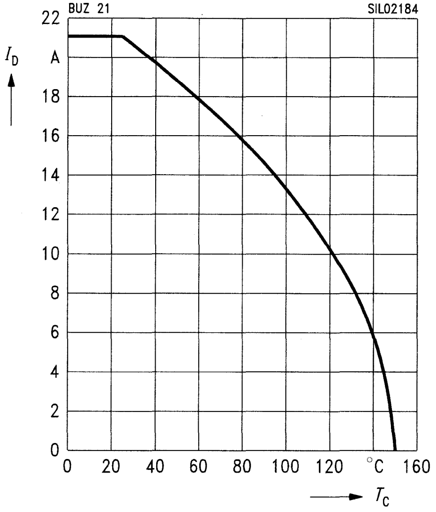
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



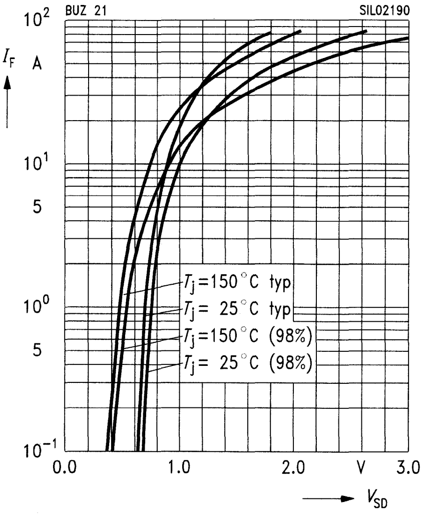
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



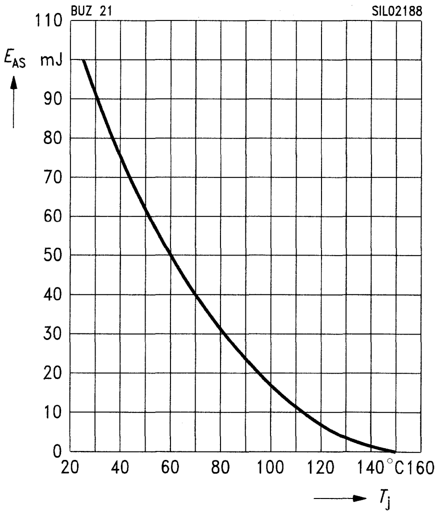
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs, (spread)



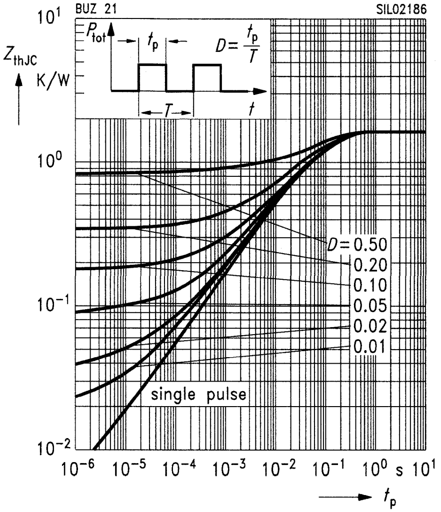
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 21$ A, $V_{DD} = 25$ V
$R_{GS} = 25\ \Omega$, $L = 340$ µH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

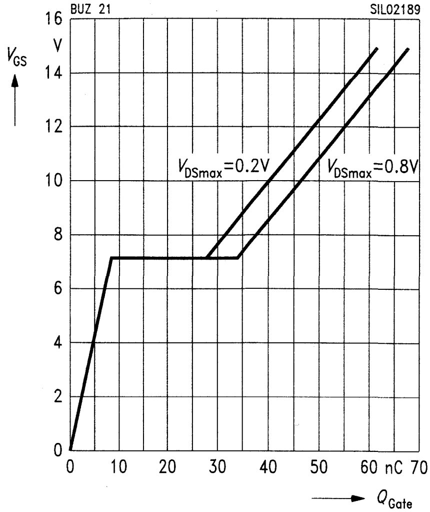
parameter: $D = t_p / T$



Typ. gate charge

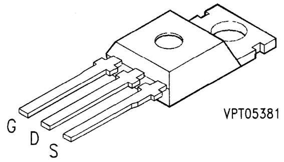
$V_{GS} = f(Q_{Gate})$

parameter: $I_{D\,puls} = 36.0$ A



SIPMOS® Power Transistor BUZ 21 L

- N channel
- Enhancement mode
- Logic Level
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 21 L	100 V	21 A	0.085 Ω	TO-220 AB	C67078-S1338-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 25 °C	I_D	**21**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**84**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**21**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**11.5**	mJ
Avalanche energy, single pulse I_D = 21 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 340 µH, T_j = 25 °C	E_{AS}	**100**	
Gate-source voltage	V_{GS}	**± 10**	V
Gate-source peak voltage, aperiodic	V_{gs}	**± 20**	
Power dissipation, T_C = 25 °C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	100	–	–	V
Gate threshold voltage V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS\,(th)}$	1.5	2.0	2.5	V
Zero gate voltage drain current V_{DS} = 100 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 5 V, I_D = 10.5 A	$R_{DS\,(on)}$	–	0.075	0.085	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 10.5 A	g_{fs}	8	14	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1200	1500	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	320	580	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	160	260	
Turn-on time t_{on}, ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	25	40	ns
	t_r	–	110	170	
Turn-off time t_{off}, ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	210	270	
	t_f	–	100	130	

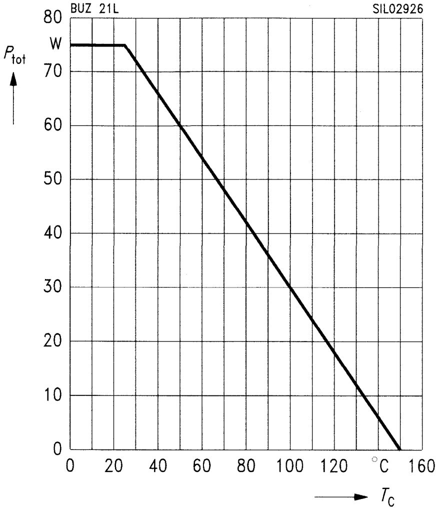
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	**typ.**	**max.**	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	21	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	84	
Diode forward on-voltage I_S = 42 A, V_{GS} = 0 V	V_{SD}	–	1.35	1.7	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	150	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.58	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

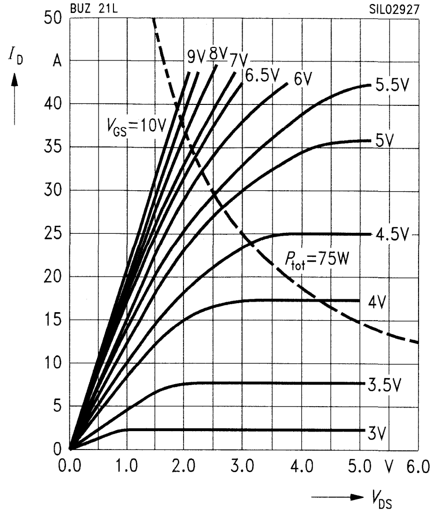
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

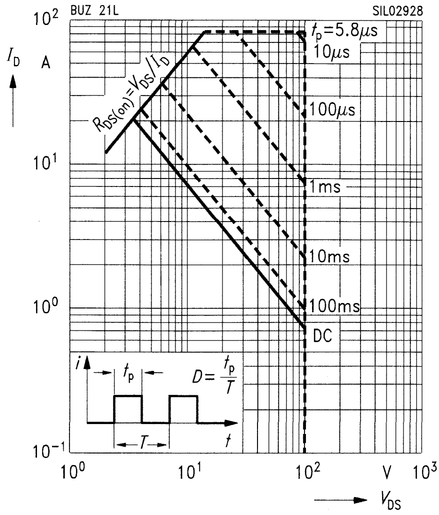
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

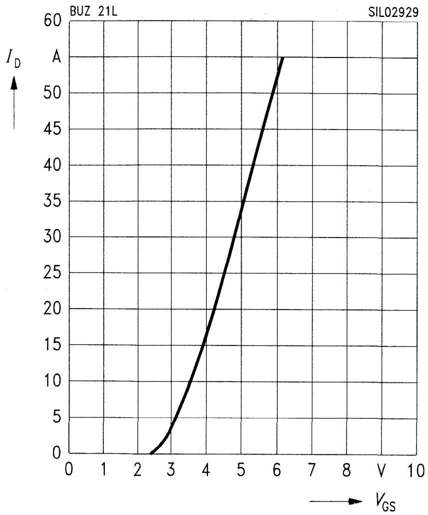
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

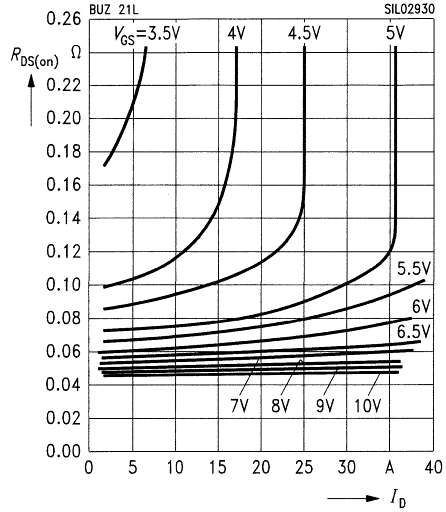
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



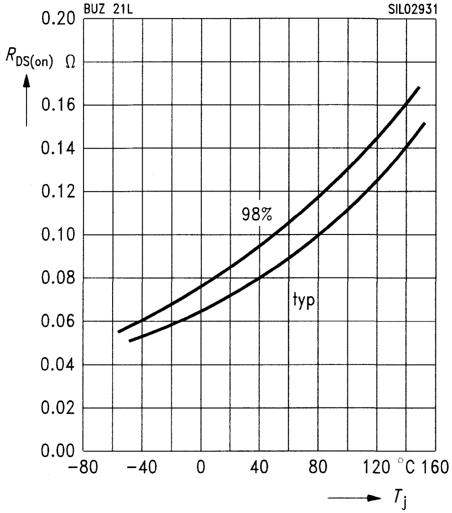
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$
parameter: V_{GS}



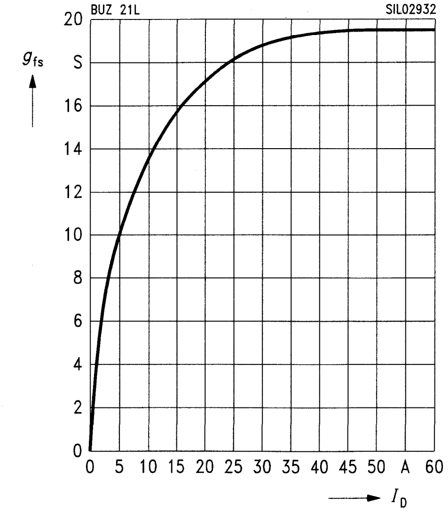
Drain-source on-resistance

$R_{DS(on)} = f(T_j)$
parameter: I_D = 10.5 A, V_{GS} = 5 V, (spread)



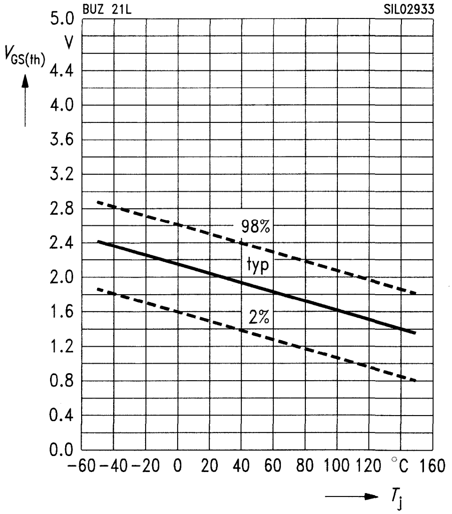
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: t_p = 80 µs

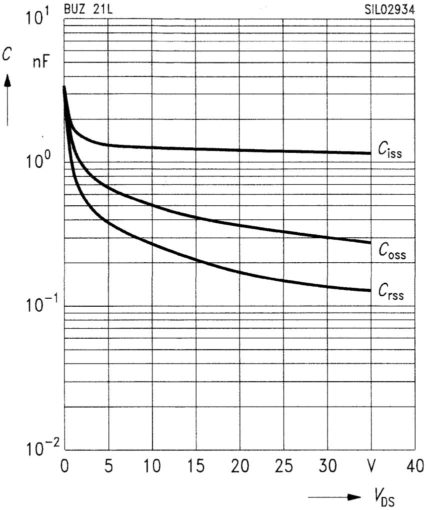


Gate threshold voltage

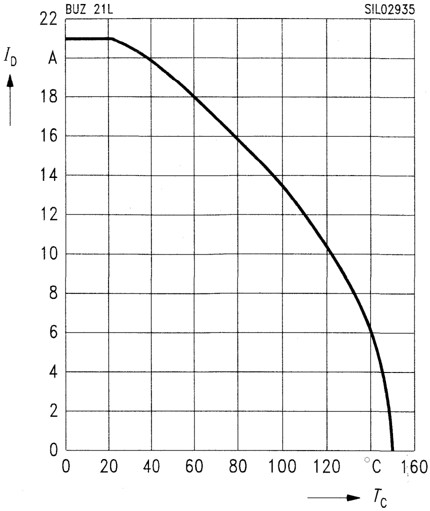
$V_{GS(th)} = f(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



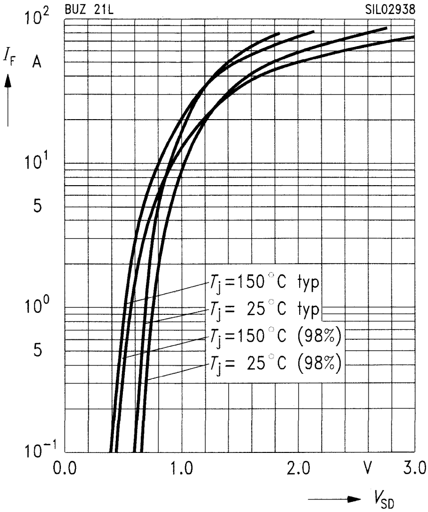
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



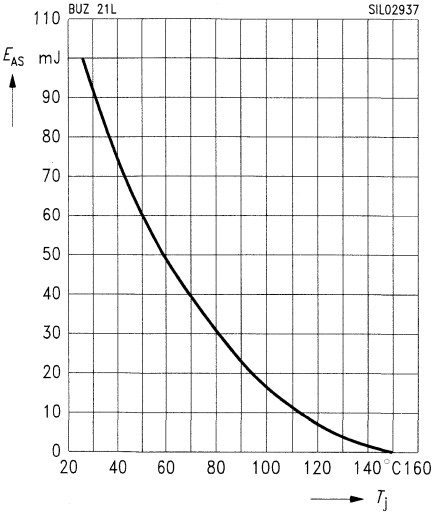
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 5$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs, (spread)

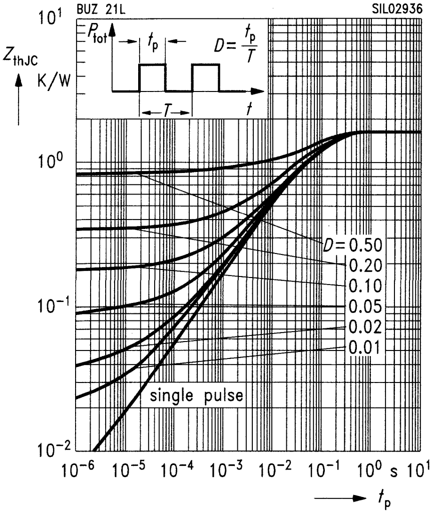


Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 21$A, $V_{DD} = 25$ V
$R_{GS} = 25\ \Omega$, $L = 340$ µH



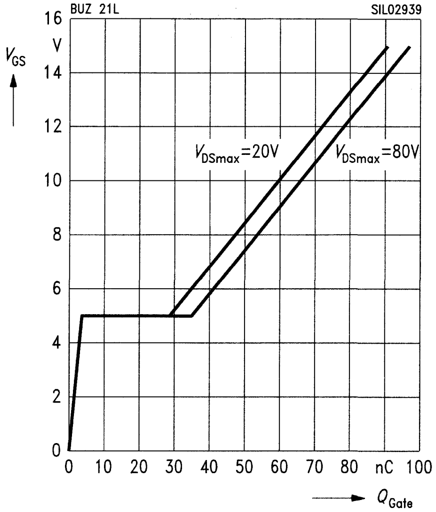
Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

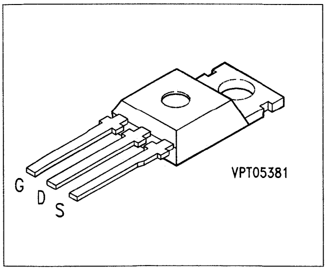
$V_{GS} = f(Q_{\text{Gate}})$
parameter: $I_{\text{D puls}} = 31.5$ A



SIEMENS

SIPMOS® Power Transistor **BUZ 22**

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 22	100 V	34 A	0.055 Ω	TO-220 AB	C67078-S1333-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 27 °C	I_D	**34**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**136**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**34**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**15**	mJ
Avalanche energy, single pulse I_D = 34 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 285.5 µH, T_j = 25 °C	E_{AS}	**220**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at $T_j = 25$ °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage $V_{GS} = 0$ V, $I_D = 0.25$ mA	$V_{(BR)\,DSS}$	100	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, $I_D = 1$ mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current $V_{DS} = 100$ V, $V_{GS} = 0$ V	I_{DSS}				µA
$T_j = 25$ °C		–	0.1	1.0	
$T_j = 125$ °C		–	10	100	
Gate-source leakage current $V_{GS} = 20$ V, $V_{DS} = 0$ V	I_{GSS}	–	10	100	nA
Drain-source on-resistance $V_{GS} = 10$ V, $I_D = 22$ A	$R_{DS\,(on)}$	–	0.05	0.055	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, $I_D = 22$ A	g_{fs}	10	17.5	–	S
Input capacitance $V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	C_{iss}	–	1400	1850	pF
Output capacitance $V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	C_{oss}	–	450	700	
Reverse transfer capacitance $V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	C_{rss}	–	230	370	
Turn-on time t_{on}, ($t_{on} = t_{d\,(on)} + t_r$) $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_D = 3$ A, $R_{GS} = 50\ \Omega$	$t_{d\,(on)}$	–	20	30	ns
	t_r	–	80	120	
Turn-off time t_{off}, ($t_{off} = t_{d\,(off)} + t_f$) $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_D = 3$ A, $R_{GS} = 50\ \Omega$	$t_{d\,(off)}$	–	230	300	
	t_f	–	120	160	

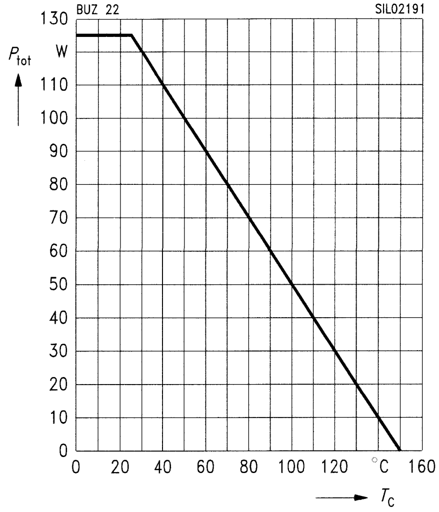
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	34	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	136	
Diode forward on-voltage I_S = 68 A, V_{GS} = 0 V	V_{SD}	–	1.4	1.8	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	130	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.7	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

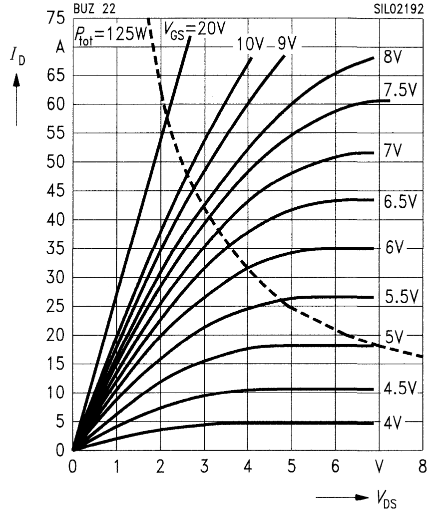
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

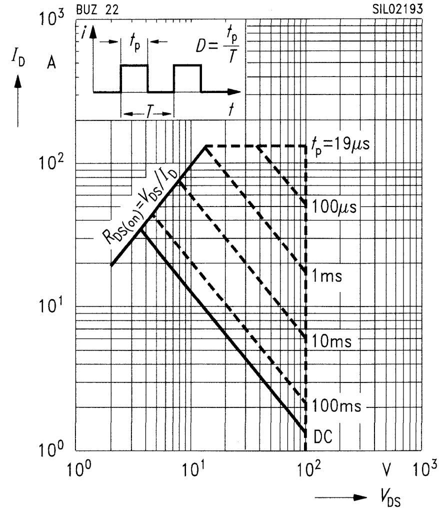
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

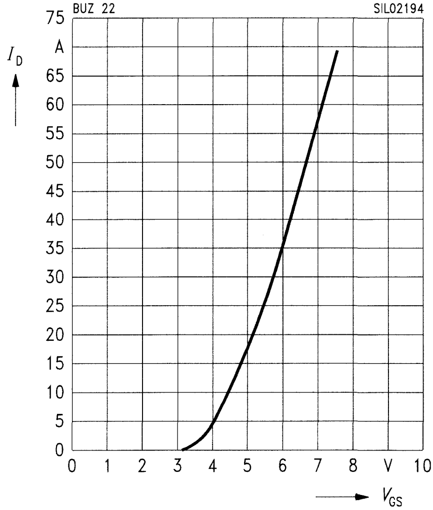
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

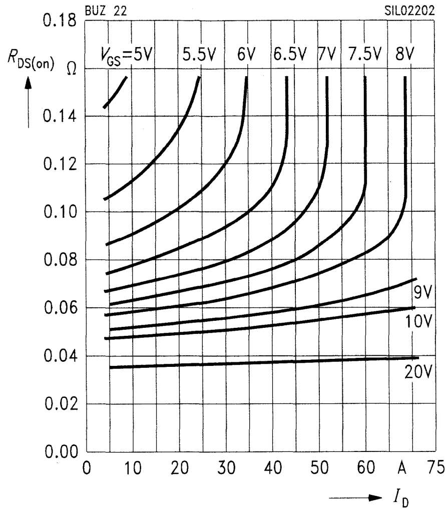
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



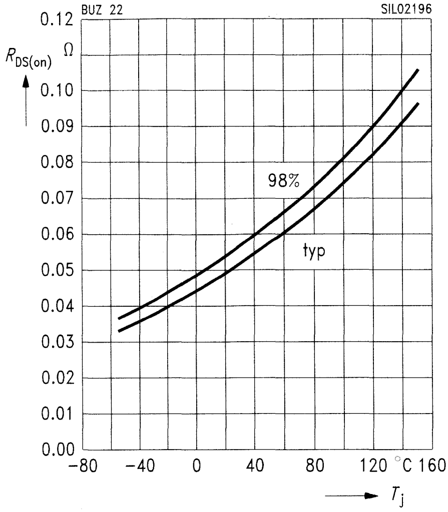
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



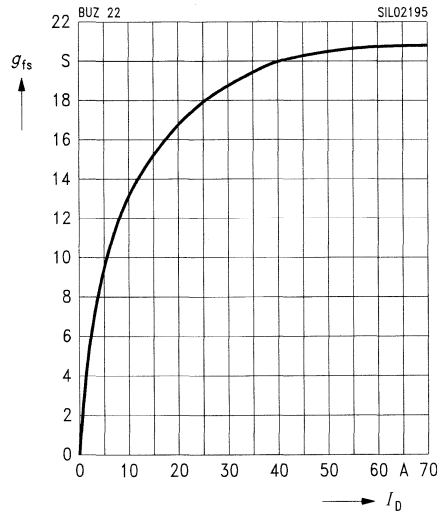
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 22 A, V_{GS} = 10 V, (spread)



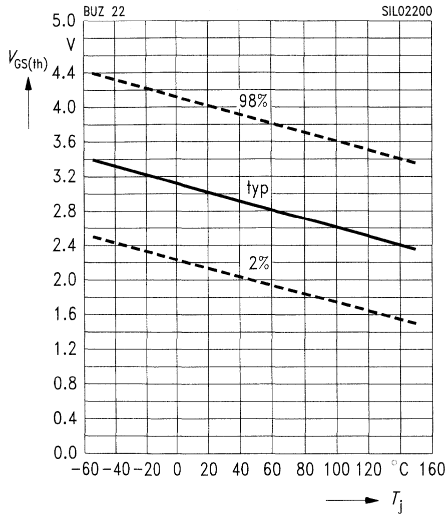
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs

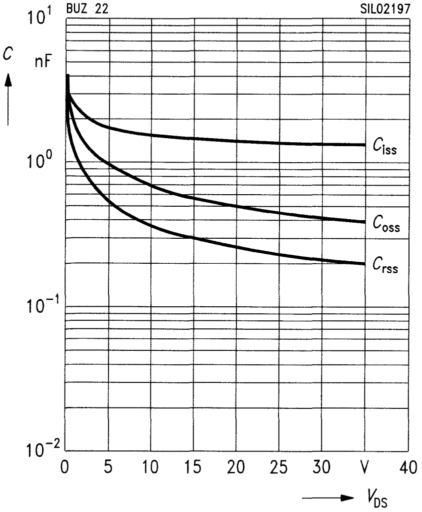


Gate threshold voltage

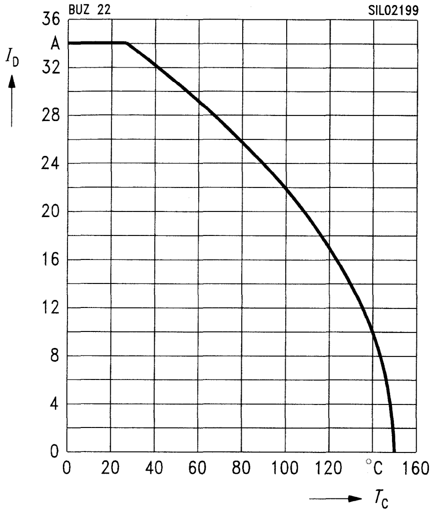
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



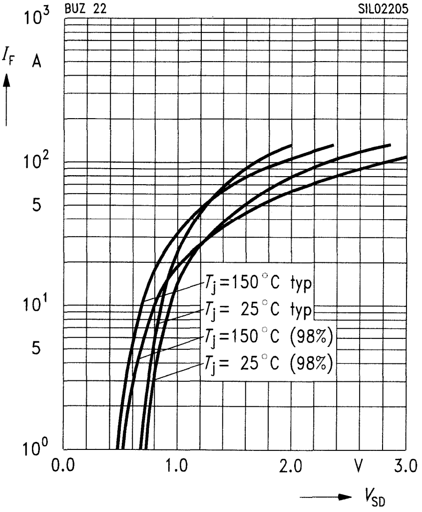
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



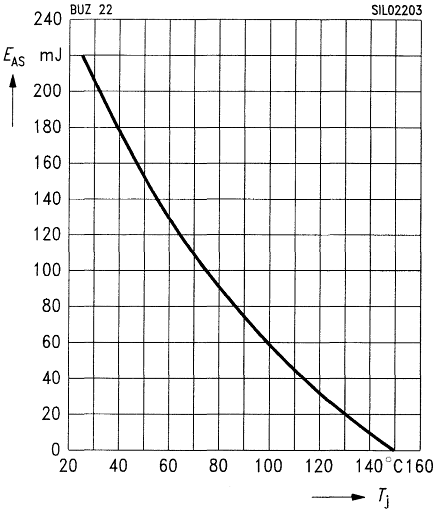
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs, (spread)



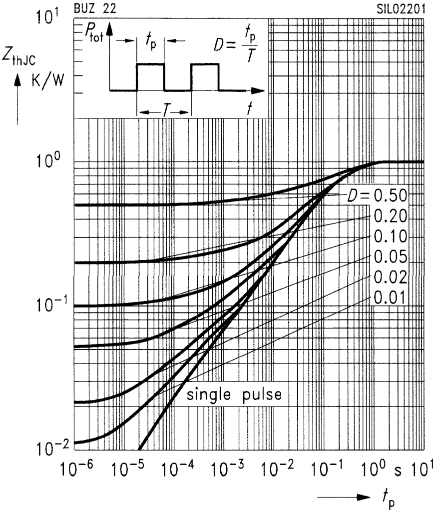
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 34$ A, $V_{DD} = 25$ V
$R_{GS} = 25\ \Omega$, $L = 285.5$ µH



Transient thermal impedance

$Z_{\text{th JC}} = f\,(t_p)$

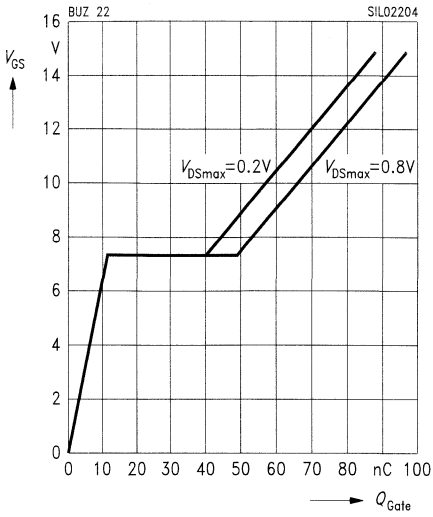
parameter: $D = t_p\,/\,T$



Typ. gate charge

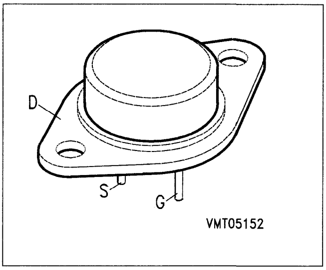
$V_{GS} = f\,(Q_{\text{Gate}})$

parameter: $I_{\text{D puls}} = 51.0$ A



SIPMOS® Power Transistor **BUZ 24**

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	**Package** [1]	**Ordering Code**
BUZ 24	100 V	32 A	0.06 Ω	TO-204 AE	C67078-S1003-A2

Maximum Ratings

Parameter	**Symbol**	**Values**	**Unit**
Continuous drain current, $T_C = 27$ °C	I_D	**32**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**128**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**32**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**15**	mJ
Avalanche energy, single pulse $I_D = 32$ A, $V_{DD} = 25$ V, $R_{GS} = 25\ \Omega$ $L = 322\ \mu$H, $T_j = 25$ °C	E_{AS}	**220**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, $T_C = 25$ °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040	–	**C**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	100	–	–	V
Gate threshold voltage V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 100 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 20 A	$R_{DS\,(on)}$	–	0.05	0.06	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 20 A	g_{fs}	10	17	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1400	1850	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	450	700	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	230	370	
Turn-on time t_{on}, ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	30	45	ns
	t_r	–	80	125	
Turn-off time t_{off}, ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	250	320	
	t_f	–	120	160	

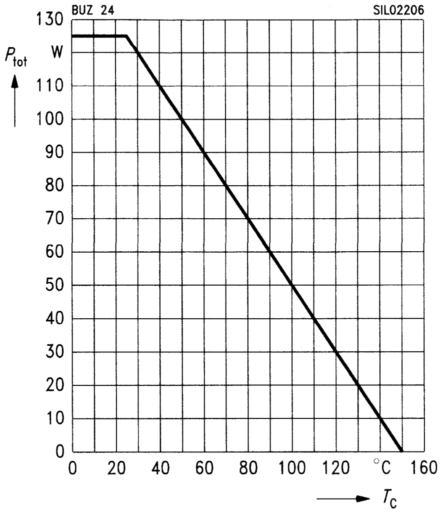
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	32	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	128	
Diode forward on-voltage I_S = 64 A, V_{GS} = 0 V	V_{SD}	–	1.4	1.7	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	130	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.7	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

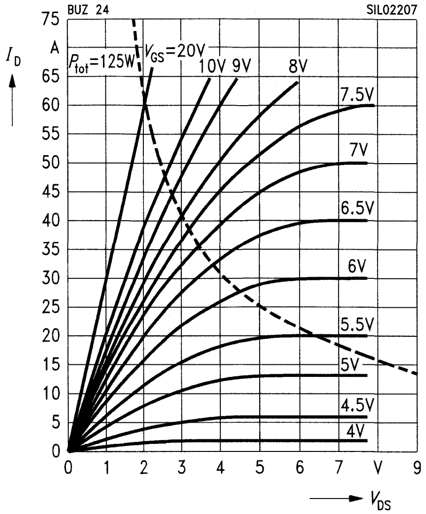
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

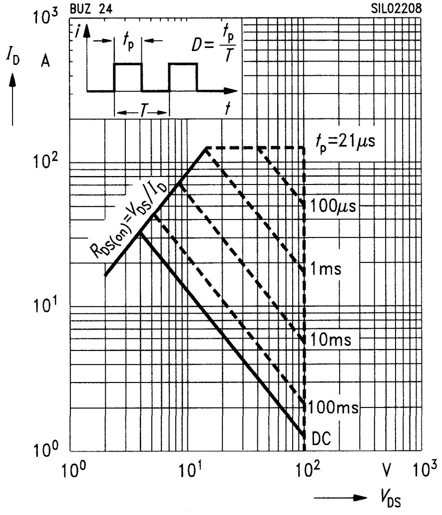
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

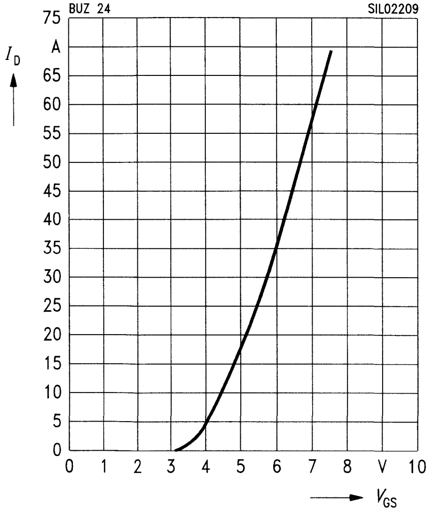
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

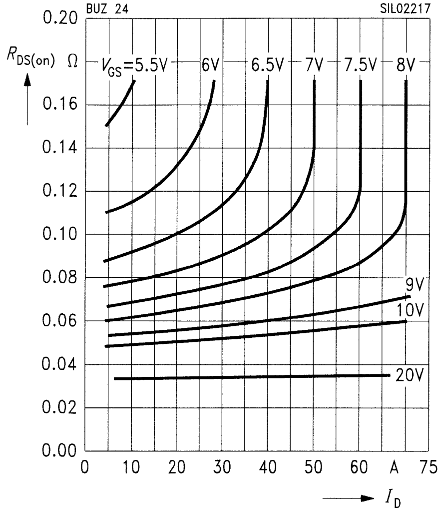
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



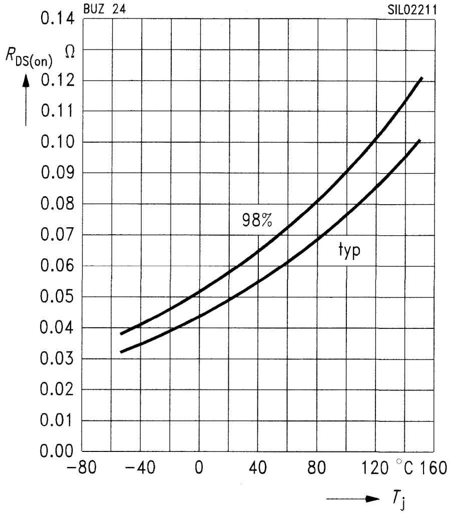
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



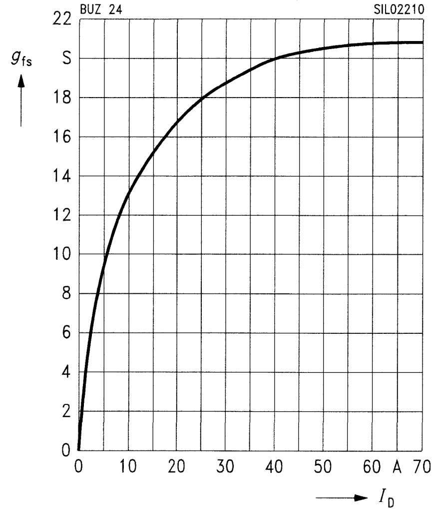
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 20 A, V_{GS} = 10 V, (spread)



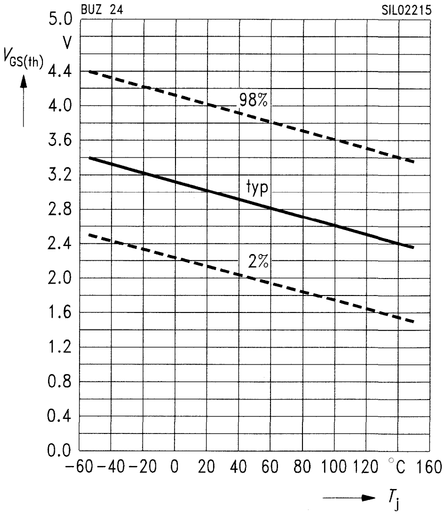
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

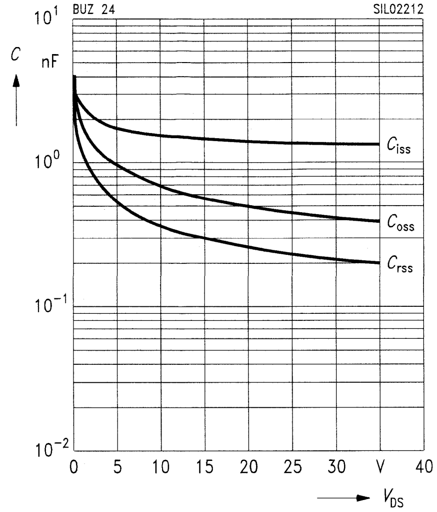
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

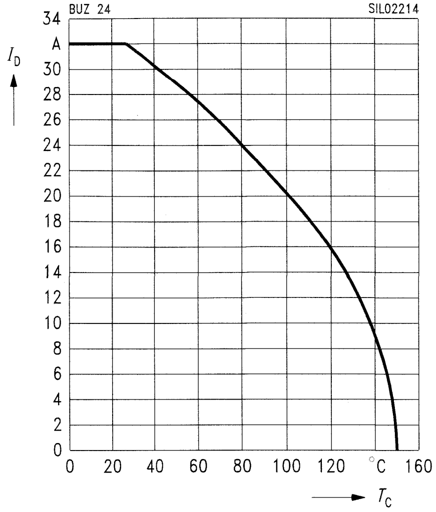
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

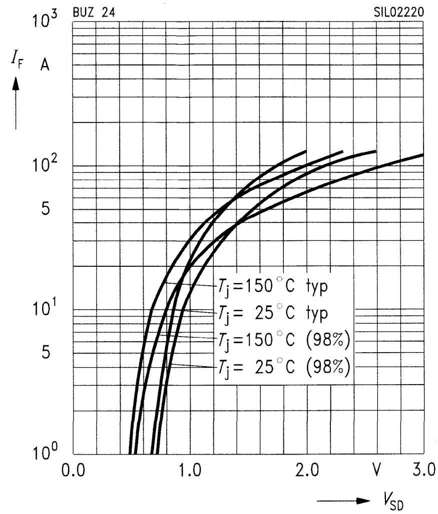
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

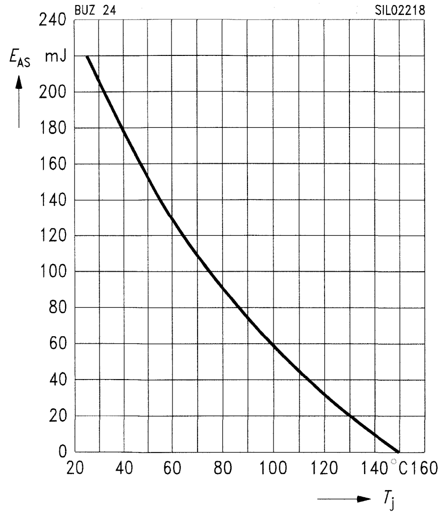
parameter: T_j, $t_p = 80$ µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

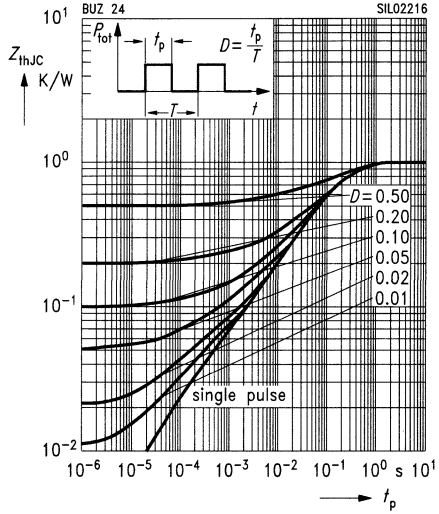
parameter: $I_D = 32$ A, $V_{DD} = 25$ V

$R_{GS} = 25\ \Omega$, $L = 322$ µH



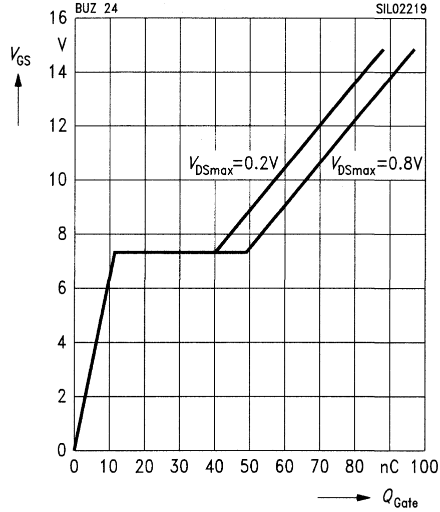
Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 51.0$ A

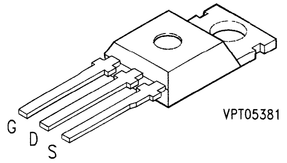


SIEMENS

SIPMOS® Power Transistor

BUZ 30 A

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	**Package 1)**	**Ordering Code**
BUZ 30 A	200 V	21 A	0.13 Ω	TO-220 AB	C67078-S1303-A3

Maximum Ratings

Parameter	**Symbol**	**Values**	**Unit**
Continuous drain current, T_C = 26 °C	I_D	**21**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**84**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**21**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**12**	mJ
Avalanche energy, single pulse I_D = 21 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 1.53 mH, T_j = 25 °C	E_{AS}	**450**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	200	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 200 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 13.5 A	$R_{DS(on)}$	–	0.10	0.13	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 13.5 A	g_{fs}	6	15	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1400	1900	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	280	400	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	130	200	
Turn-on time t_{on}, ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	30	45	ns
	t_r	–	70	110	
Turn-off time t_{off}, ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	250	320	
	t_f	–	90	120	

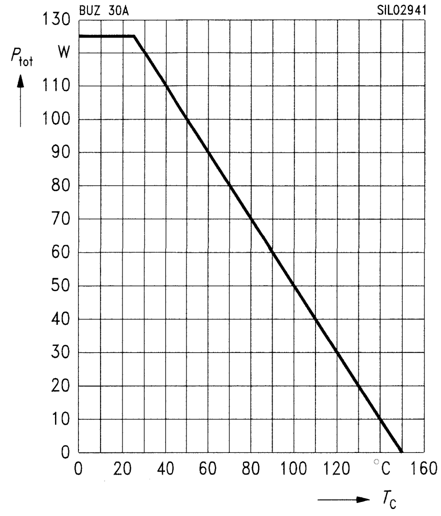
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	21	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	84	
Diode forward on-voltage I_S = 42 A, V_{GS} = 0 V	V_{SD}	–	1.2	1.6	V
Reverse recovery time V_R = 10 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	180	–	ns
Reverse recovery charge V_R = 10 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	1.2	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

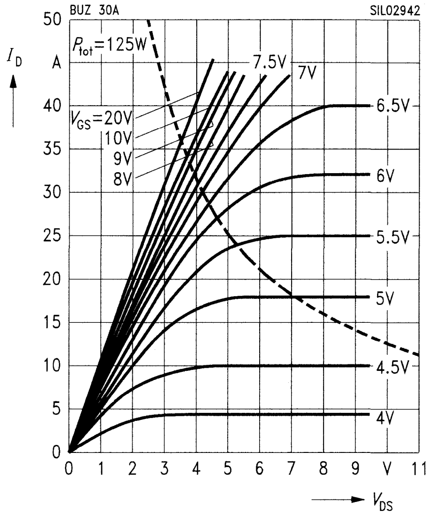
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

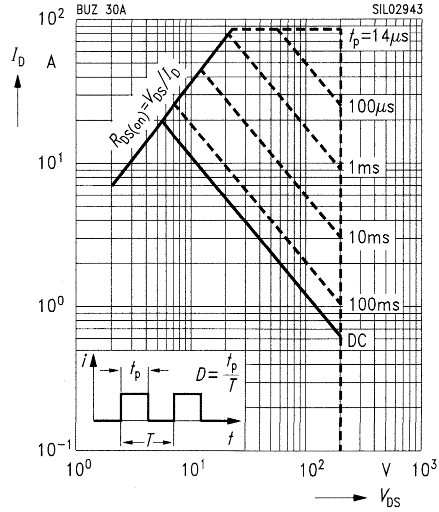
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

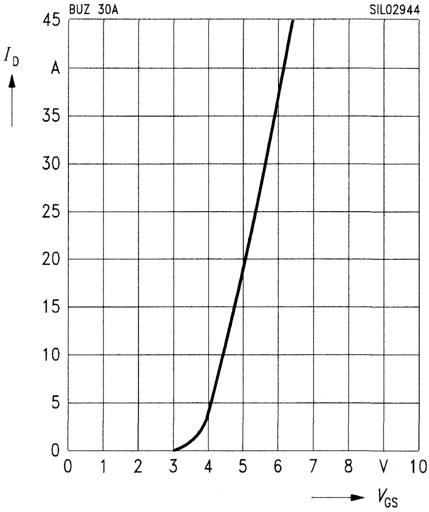
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

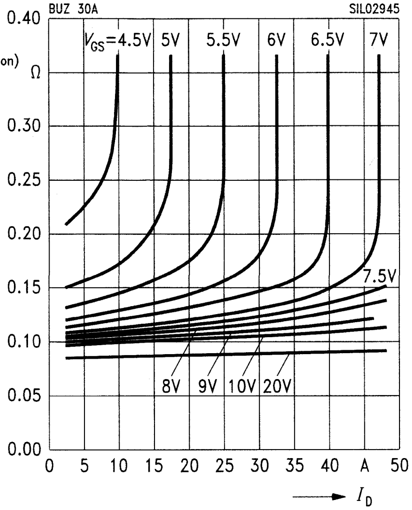
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

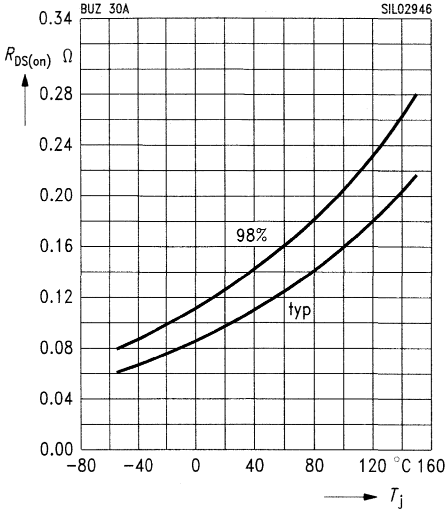
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

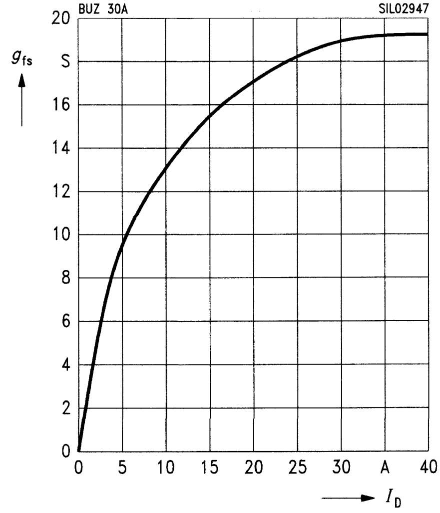
parameter: I_D = 13.5 A, V_{GS} = 10 V, (spread)



Typ. forward transconductance

$g_{fs} = f\,(I_D)$

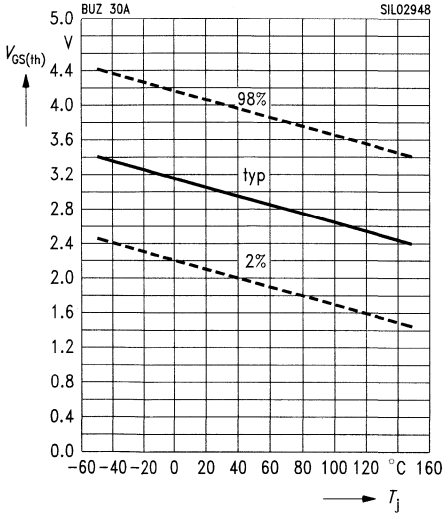
parameter: t_p = 80 µs



Gate threshold voltage

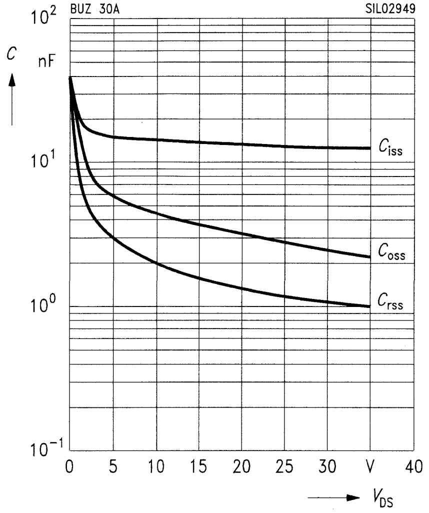
$V_{GS\,(th)} = f\,(T_j)$

parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



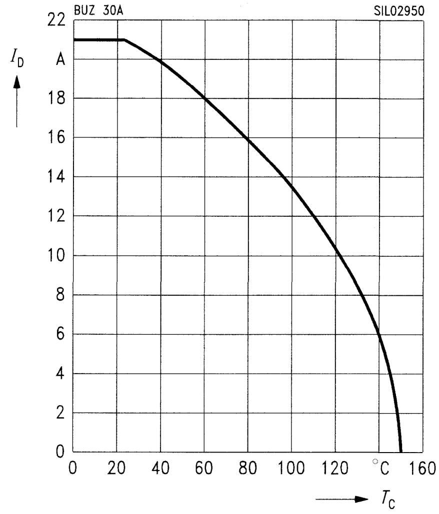
Typ. capacitances

$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



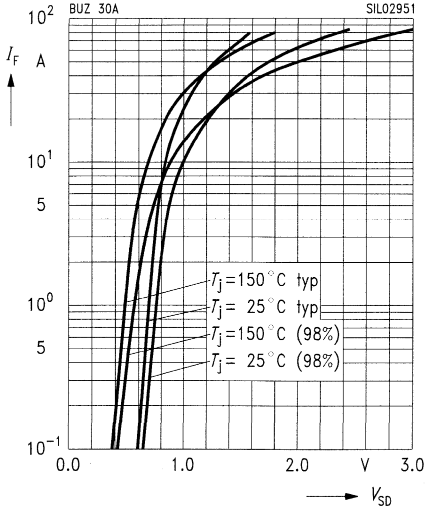
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



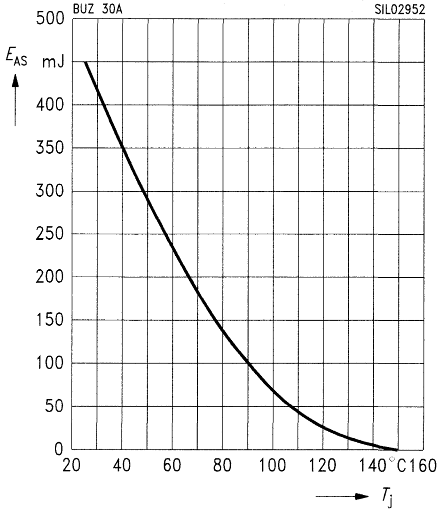
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

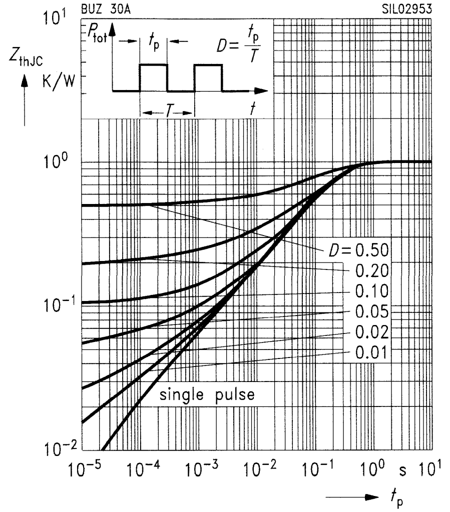
parameter: $I_D = 21$ A, $V_{DD} = 50$ V
$R_{GS} = 25\ \Omega$, $L = 1.53$ mH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

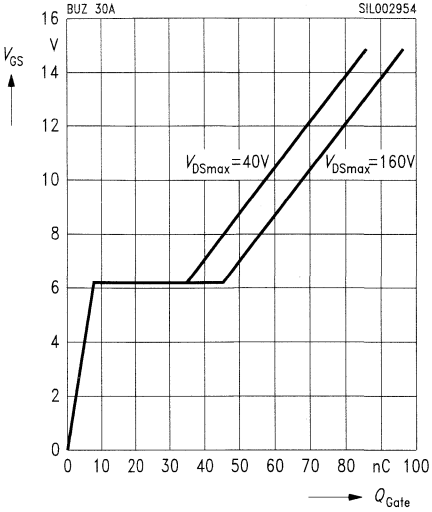
parameter: $D = t_p / T$



Typ. gate charge

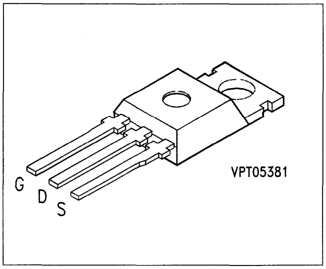
$V_{GS} = f(Q_{\text{Gate}})$

parameter: $I_{\text{D puls}}$ = 31.5 A



SIPMOS® Power Transistor **BUZ 31**

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 31	200 V	13.5 A	0.2 Ω	TO-220 AB	C67078-S1304-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, $T_C = 28$ °C	I_D	**13.5**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**54**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**13.5**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**9**	mJ
Avalanche energy, single pulse $I_D = 13.5$ A, $V_{DD} = 50$ V, $R_{GS} = 25\ \Omega$ $L = 1.65$ mH, $T_j = 25$ °C	E_{AS}	**200**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, $T_C = 25$ °C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	200	–	–	V
Gate threshold voltage V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 200 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 8.5 A	$R_{DS\,(on)}$	–	0.16	0.2	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 8.5 A	g_{fs}	5.0	10.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	960	1250	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	200	330	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	100	170	
Turn-on time t_{on}, ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	20	30	ns
	t_r	–	45	70	
Turn-off time t_{off}, ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	180	230	
	t_f	–	60	80	

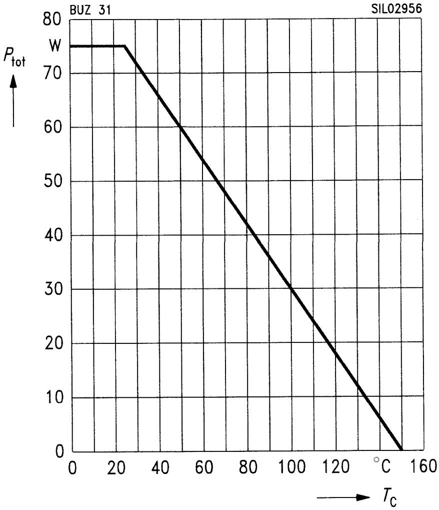
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	13.5	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	54	
Diode forward on-voltage I_S = 27 A, V_{GS} = 0 V	V_{SD}	–	1.1	1.6	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	180	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	1.2	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

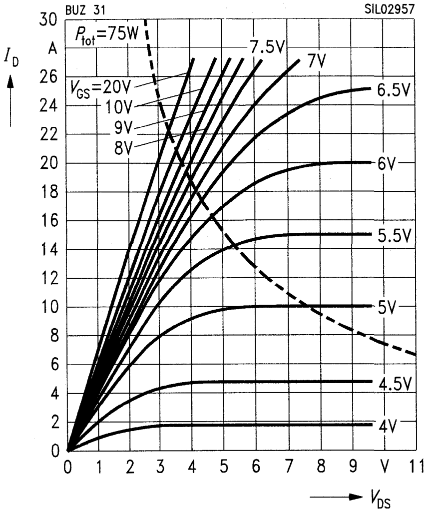
Total power dissipation

$P_{tot} = f(T_C)$



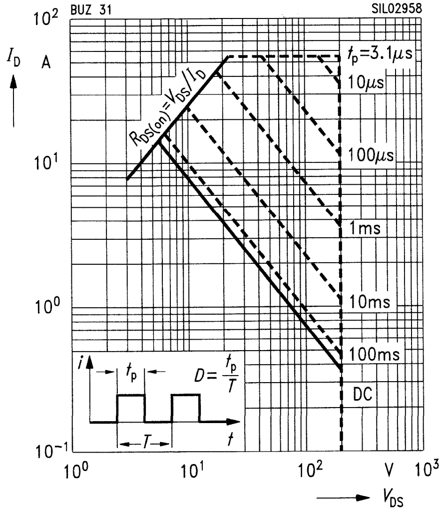
Typ. output characteristics

$I_D = f(V_{DS})$
parameter: t_p = 80 µs



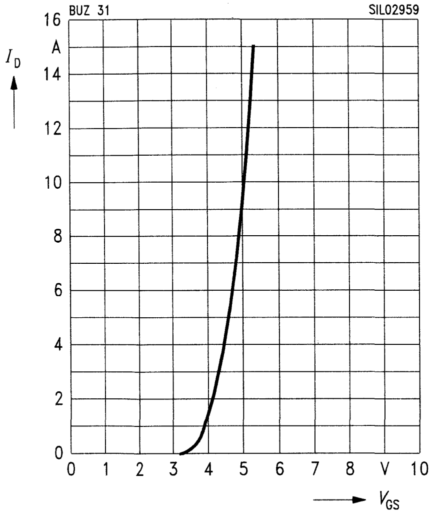
Safe operating area

$I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



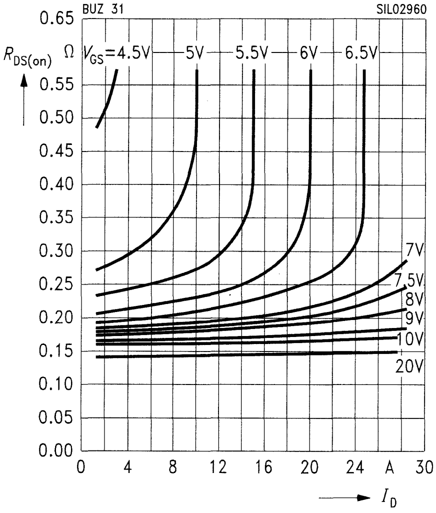
Typ. transfer characteristics

$I_D = f(V_{GS})$
parameter: t_p = 80 µs, V_{DS} = 25 V



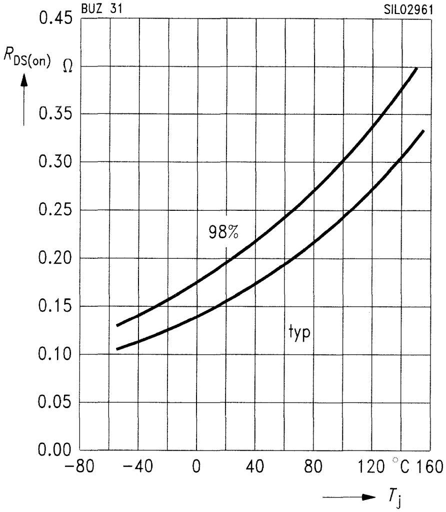
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



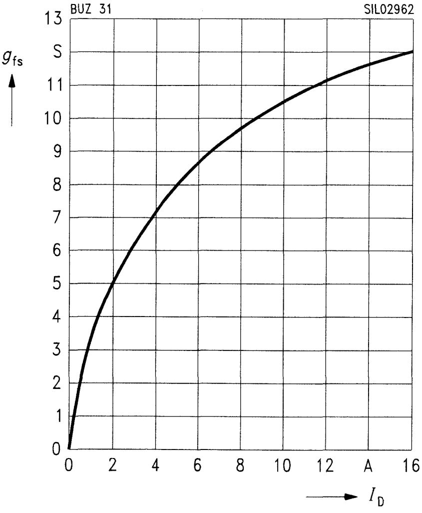
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 8.5 A, V_{GS} = 10 V, (spread)



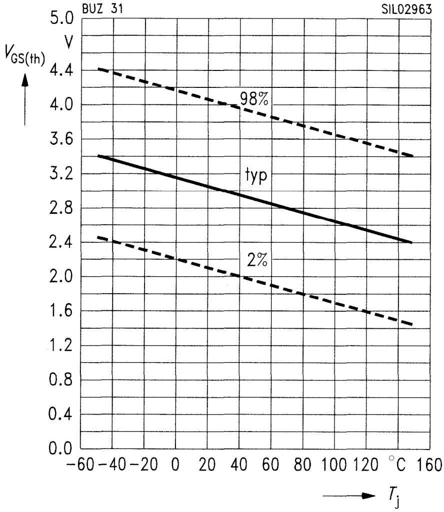
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

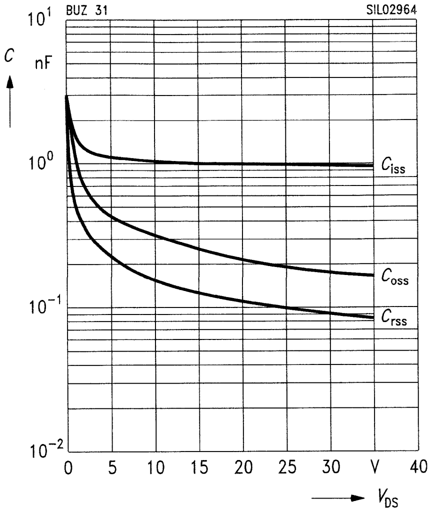
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

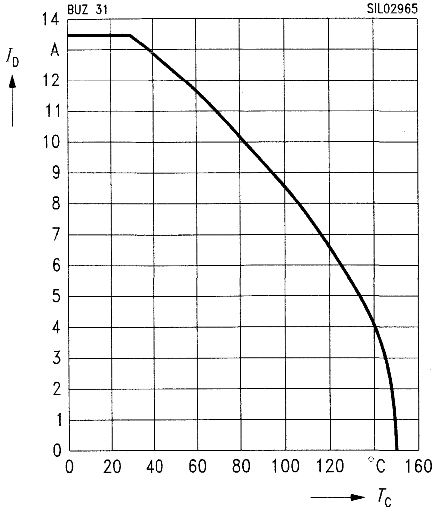
parameter: V_{GS} = 0 V, f = 1 MHz



Drain current

$I_D = f(T_C)$

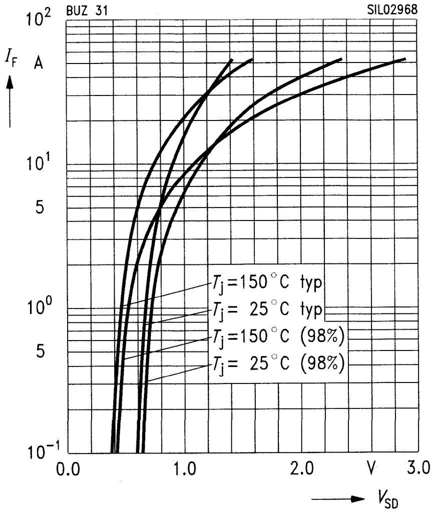
parameter: $V_{GS} \geq$ 10 V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

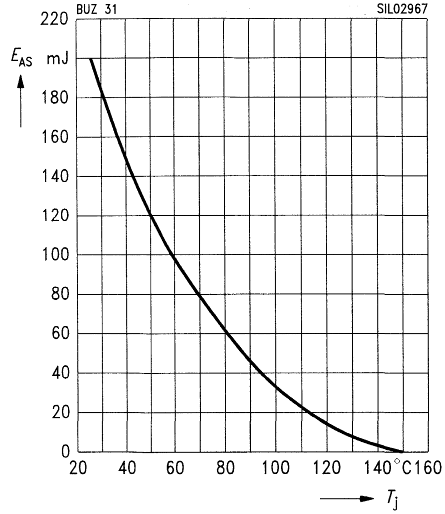
parameter: T_j, t_p = 80 µs, (spread)



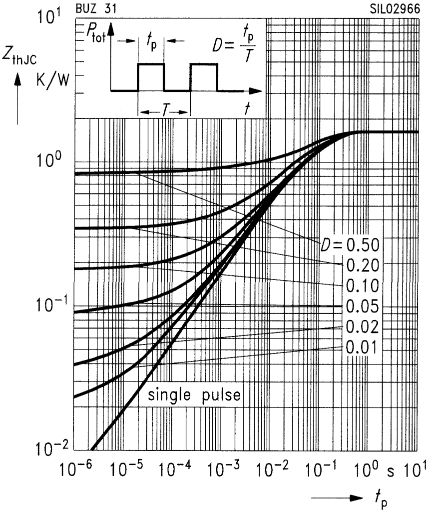
Avalanche energy $E_{AS} = f(T_j)$

parameter: I_D = 13.5 A, V_{DD} = 50 V

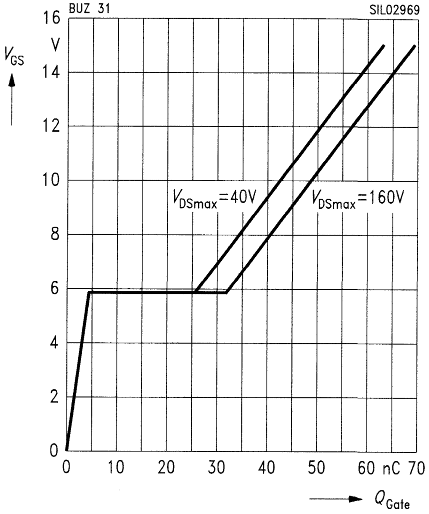
R_{GS} = 25 Ω, L = 1.65 mH



Transient thermal impedance
$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$

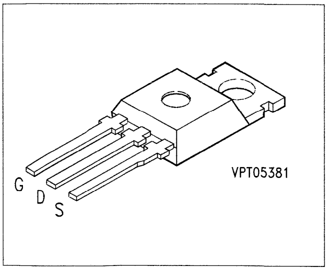


Typ. gate charge
$V_{GS} = f(Q_{\text{Gate}})$
parameter: $I_{\text{D puls}} = 20.3$ A



SIPMOS® Power Transistor **BUZ 32**

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	**Package** [1]	**Ordering Code**
BUZ 32	200 V	9.5 A	0.4 Ω	TO-220 AB	C67078-S1310-A2

Maximum Ratings

Parameter	**Symbol**	**Values**	**Unit**
Continuous drain current, T_C = 29 ˚C	I_D	**9.5**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**38**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**9.5**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**6.5**	mJ
Avalanche energy, single pulse I_D = 9.5 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 2.0 mH, T_j = 25 ˚C	E_{AS}	**120**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 ˚C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\ DSS}$	200	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\ (th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 200 V, V_{GS} = 0 V T_j = 25 °C T_j = 125 °C	I_{DSS}	 – –	 0.1 10	 1.0 100	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 6.0 A	$R_{DS\ (on)}$	–	0.3	0.4	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 6.0 A	g_{fs}	3.0	4.6	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	400	530	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	85	130	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	45	70	
Turn-on time t_{on} , ($t_{on} = t_{d\ (on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\ (on)}$	–	10	15	ns
	t_r	–	40	60	
Turn-off time t_{off} , ($t_{off} = t_{d\ (off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\ (off)}$	–	55	75	
	t_f	–	30	40	

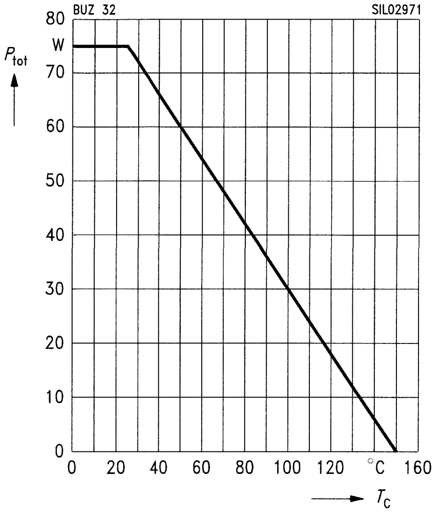
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	9.5	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	38	
Diode forward on-voltage I_S = 19 A, V_{GS} = 0 V	V_{SD}	–	1.4	1.7	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	200	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.60	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Total power dissipation

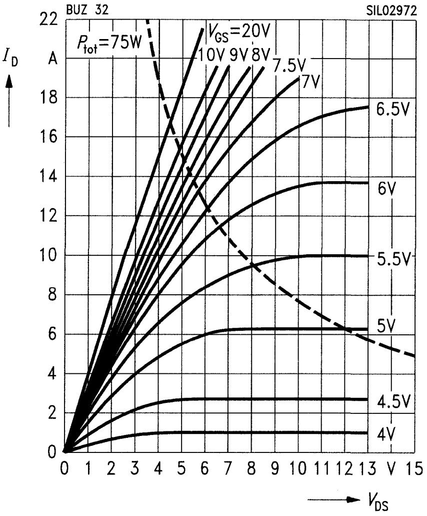
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

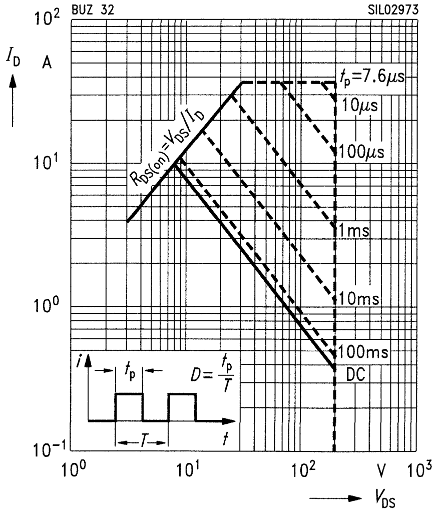
parameter: $t_p = 80$ µs



Safe operating area

$I_D = f(V_{DS})$

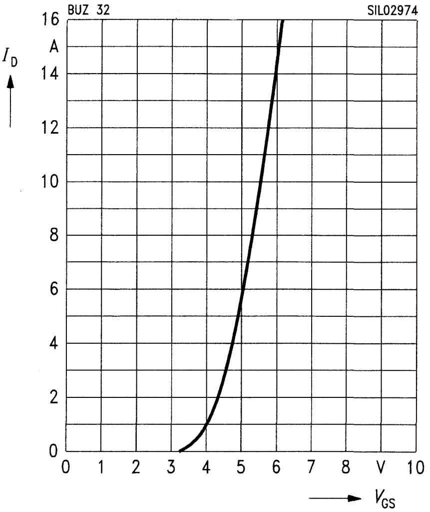
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

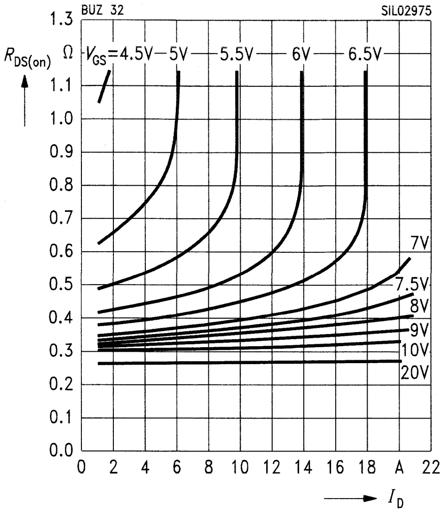
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

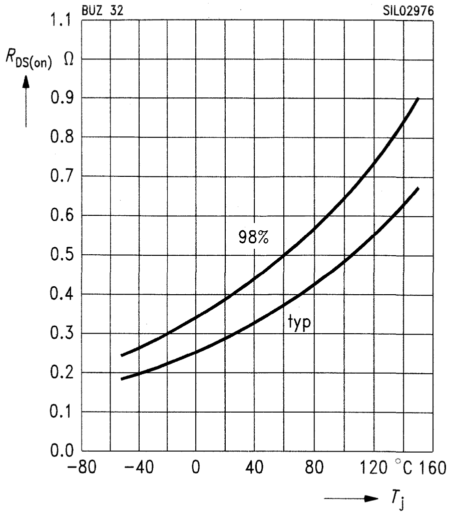
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

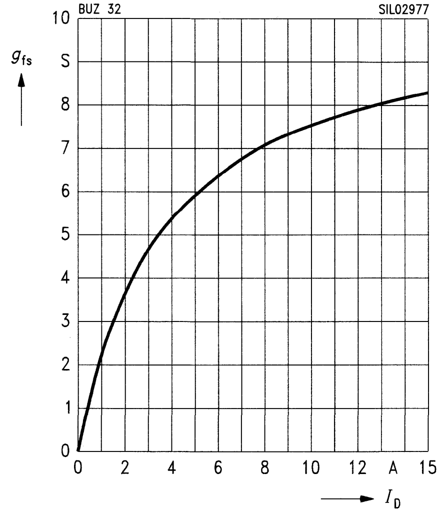
parameter: I_D = 6.0 A, V_{GS} = 10 V, (spread)



Typ. forward transconductance

$g_{fs} = f\,(I_D)$

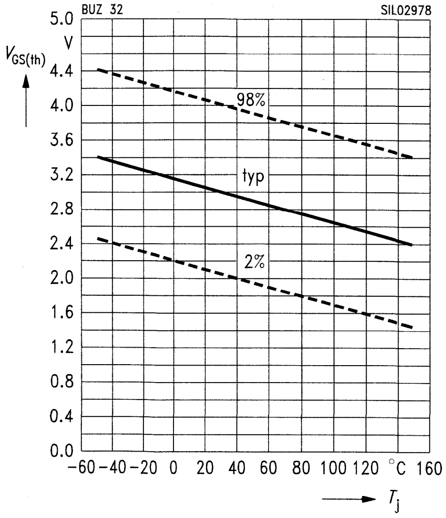
parameter: t_p = 80 µs



Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

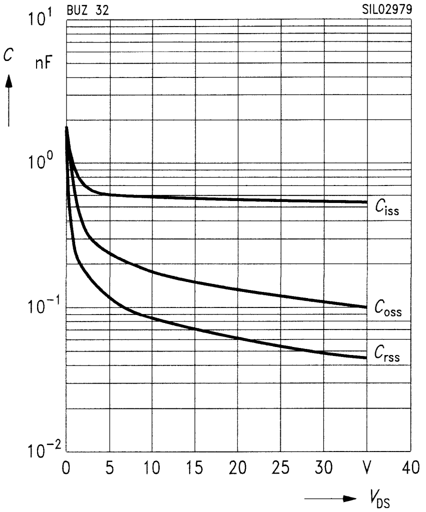
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

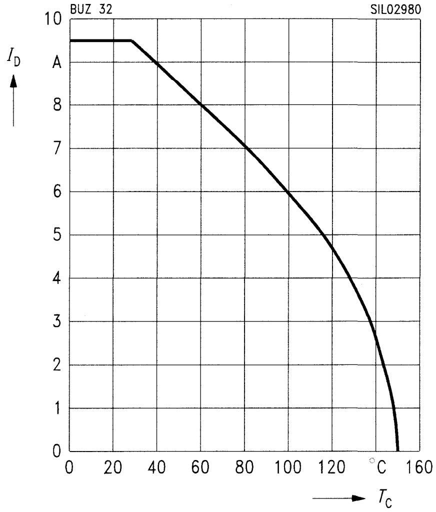
parameter: V_{GS} = 0 V, f = 1 MHz



Drain current

$I_D = f(T_C)$

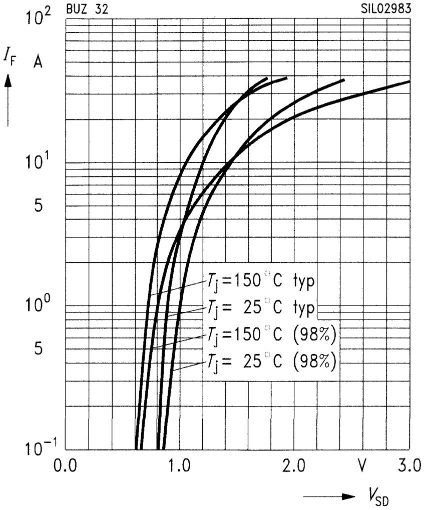
parameter: $V_{GS} \geq$ 10 V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

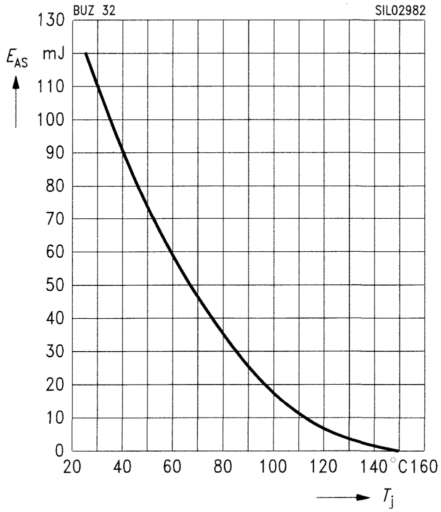
parameter: T_j, t_p = 80 µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

parameter: I_D = 9.5 A, V_{DD} = 50 V

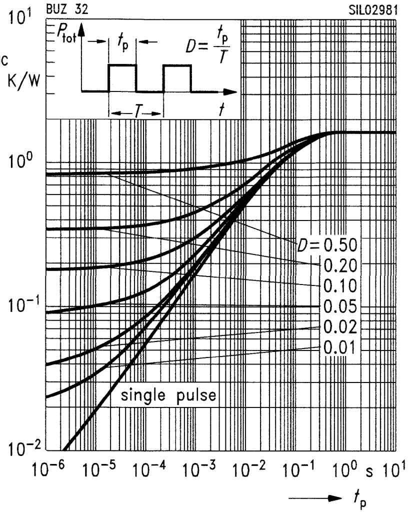
R_{GS} = 25 Ω, L = 2.0 mH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

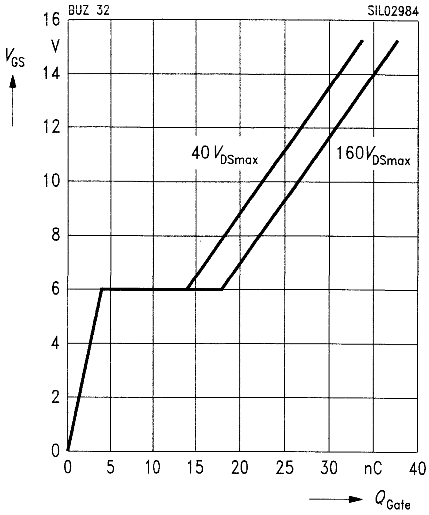
parameter: $D = t_p / T$



Typ. gate charge

$V_{\text{GS}} = f(Q_{\text{Gate}})$

parameter: $I_{\text{D puls}} = 13.5$ A

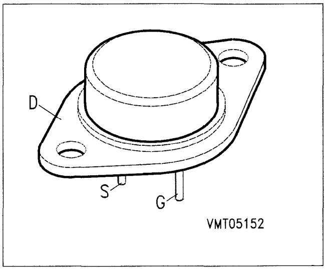


SIEMENS

SIPMOS® Power Transistor

BUZ 36

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 36	200 V	22 A	0.12 Ω	TO-204 AE	C67078-S1018-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, $T_C = 33$ °C	I_D	**22**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**88**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**22.0**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**13**	mJ
Avalanche energy, single pulse $I_D = 22$ A, $V_{DD} = 50$ V, $R_{GS} = 25$ Ω $L = 1.77$ mH, $T_j = 25$ °C	E_{AS}	**570**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, $T_C = 25$ °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**C**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	200	–	–	V
Gate threshold voltage V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 200 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 ˚C		–	0.1	1.0	
T_j = 125 ˚C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 14 A	$R_{DS(on)}$	–	0.09	0.12	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 14 A	g_{fs}	9.0	15	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1400	1900	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	280	400	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	130	200	
Turn-on time t_{on}, ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	30	45	ns
	t_r	–	70	110	
Turn-off time t_{off}, ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	250	320	
	t_f	–	90	120	

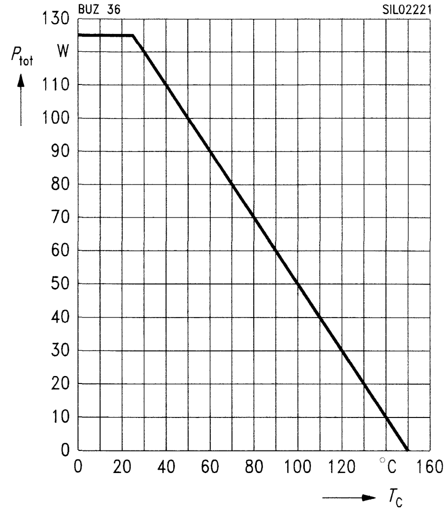
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	22	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	88	
Diode forward on-voltage I_S = 44 A, V_{GS} = 0 V	V_{SD}	–	1.2	1.7	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	180	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	1.2	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

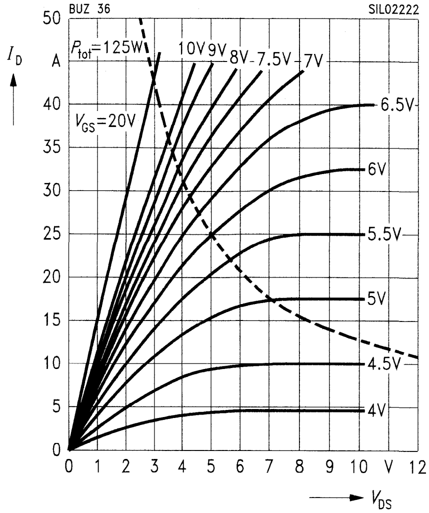
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

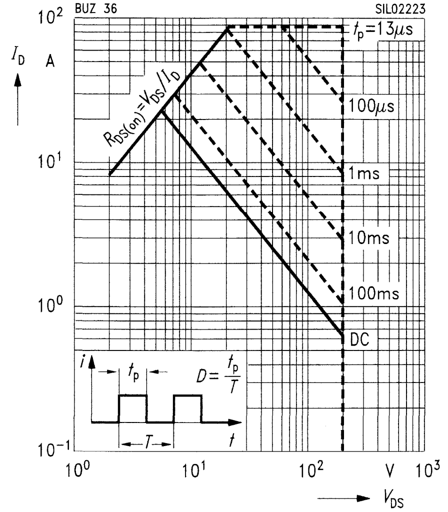
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

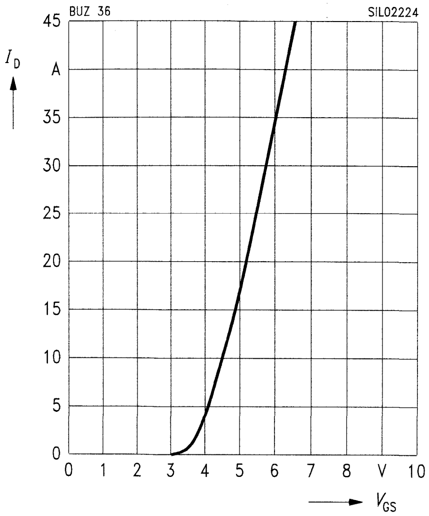
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

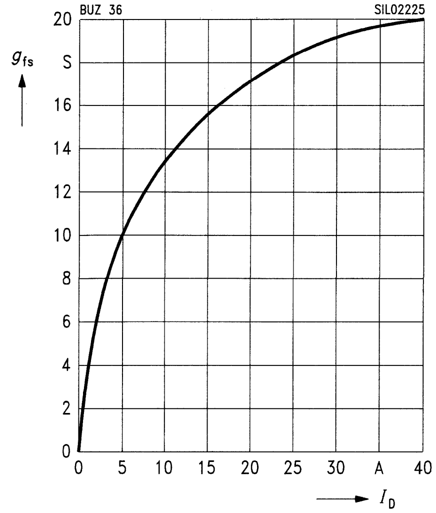
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. forward transconductance

$g_{fs} = f(I_D)$

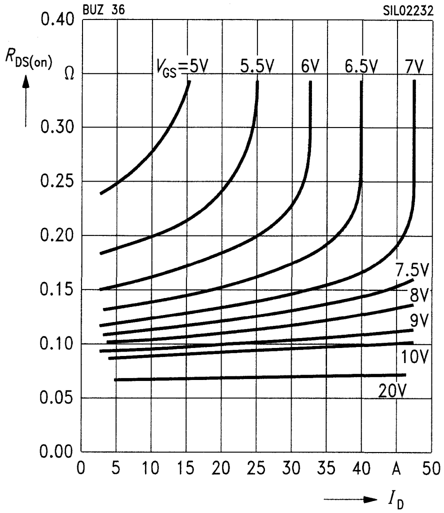
parameter: t_p = 80 µs



Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$

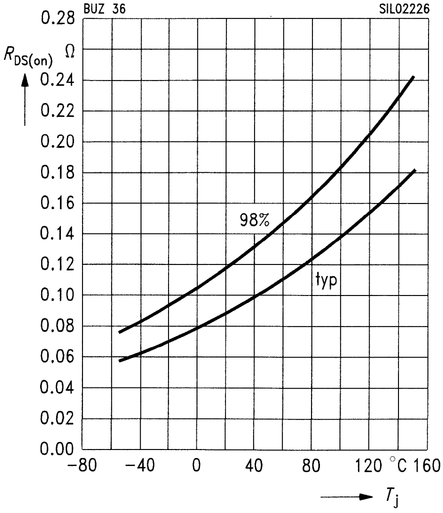
parameter: V_{GS}



Drain-source on-resistance

$R_{DS(on)} = f(T_j)$

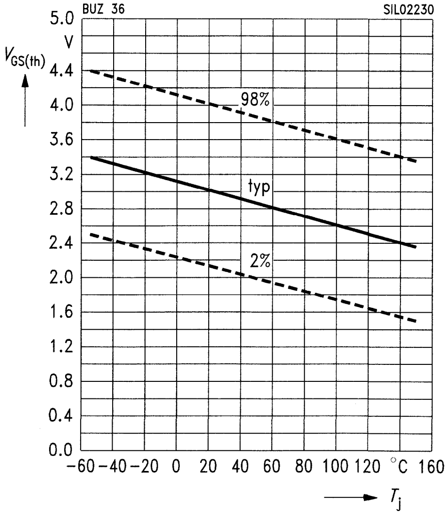
parameter: I_D = 14 A, V_{GS} = 10 V, (spread)



Gate threshold voltage

$V_{GS(th)} = f(T_j)$

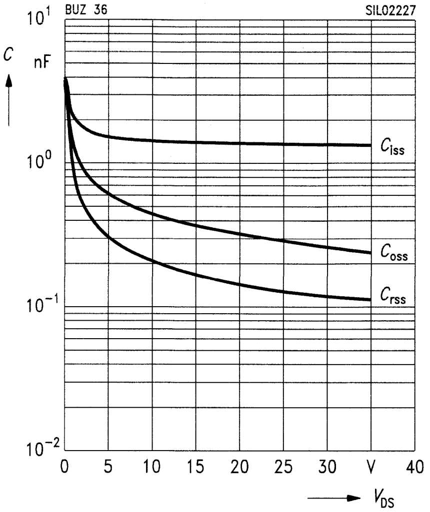
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

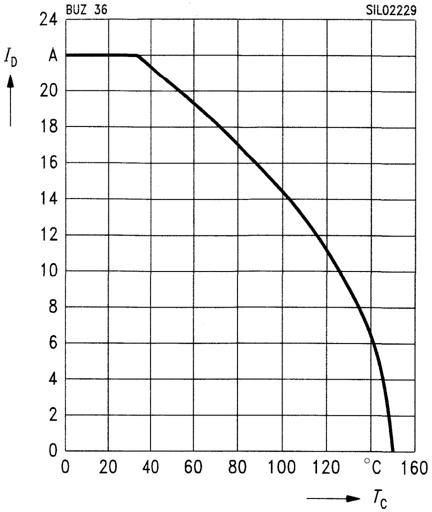
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

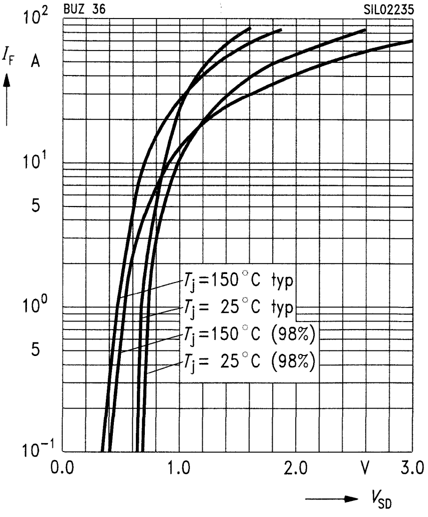
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

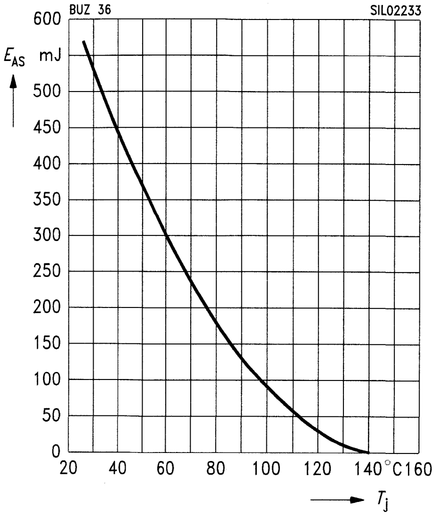
parameter: T_j , $t_p = 80$ µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

parameter: $I_D = 22$ A, $V_{DD} = 50$ V

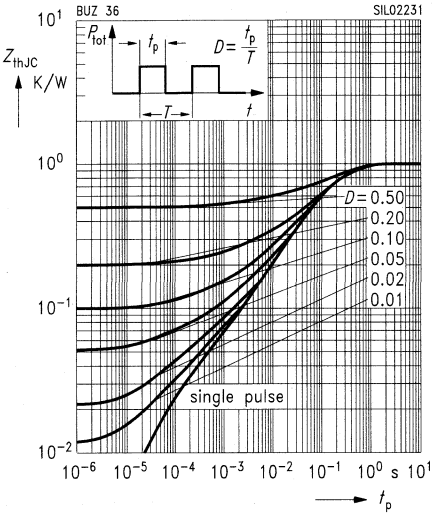
$R_{GS} = 25\ \Omega$, $L = 1.77$ mH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

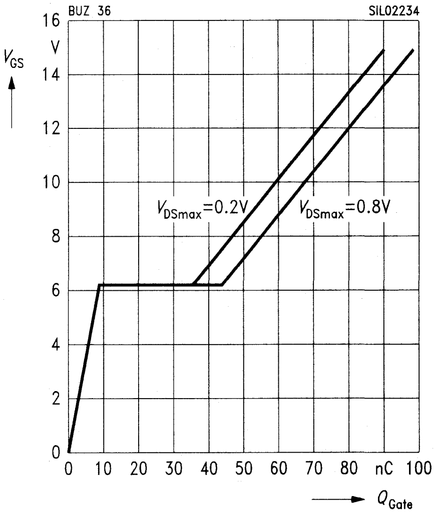
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{Gate})$

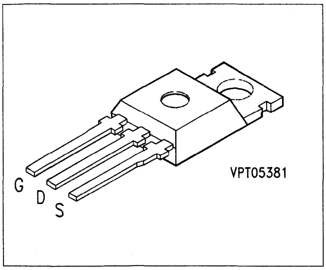
parameter: $I_{D\text{ puls}} = 33.0$ A



SIPMOS® Power Transistor

BUZ 40 B

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 40 B	500 V	8.5 A	0.8 Ω	TO-220 AB	C67078-S1305-A4

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, $T_C = 35$ °C	I_D	**8.5**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\ puls}$	**34**	
Avalanche current, limited by $T_{j\ max}$	I_{AR}	**10**	
Avalanche energy, periodic limited by $T_{j\ (max)}$	E_{AR}	**13**	mJ
Avalanche energy, single pulse $I_D = 10$ A, $V_{DD} = 50$ V, $R_{GS} = 25\ \Omega$ $L = 10.3$ mH, $T_j = 25$ °C	E_{AS}	**570**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, $T_C = 25$ °C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\ JC}$	**≤ 0.83**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	500	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 500 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 5.5 A	$R_{DS\,(on)}$	–	0.6	0.8	W
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 5.5 A	g_{fs}	5.0	8.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1500	2300	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	180	270	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	65	100	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	20	30	ns
	t_r	–	70	110	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	260	340	
	t_f	–	80	100	

Electrical Characteristics (cont'd)

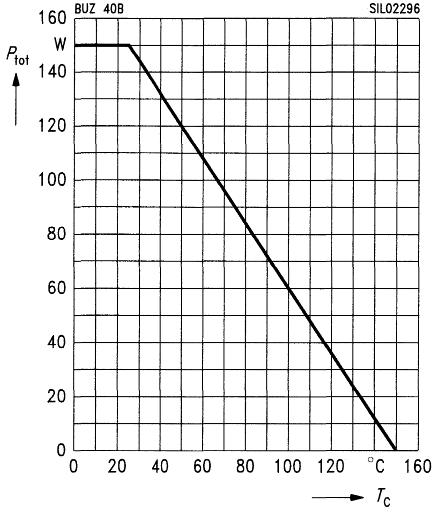
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	8.5	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	34	
Diode forward on-voltage I_S = 20 A, V_{GS} = 0 V	V_{SD}	–	1.1	1.3	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	380	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	4	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Total power dissipation

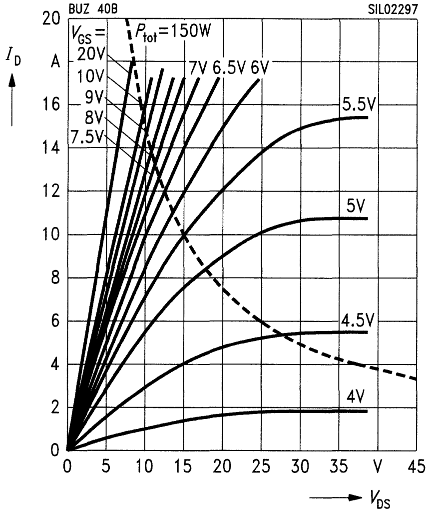
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

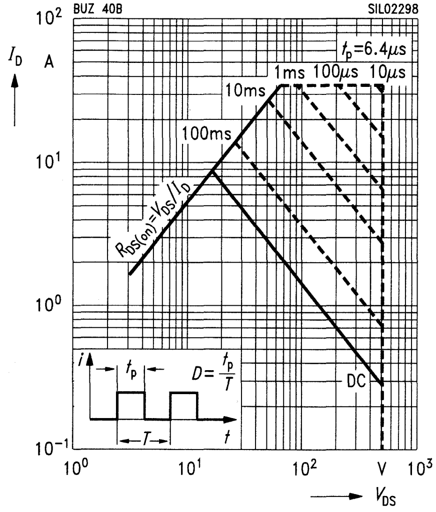
parameter: $t_p = 80$ µs



Safe operating area

$I_D = f(V_{DS})$

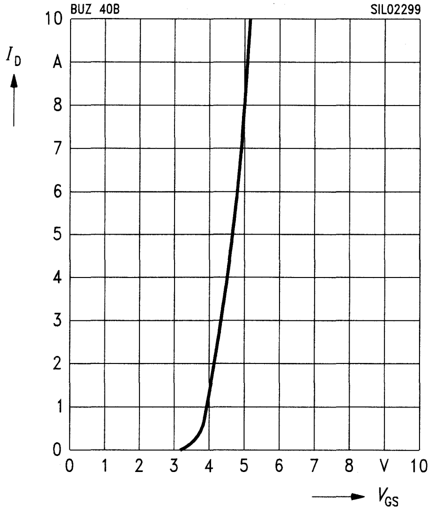
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

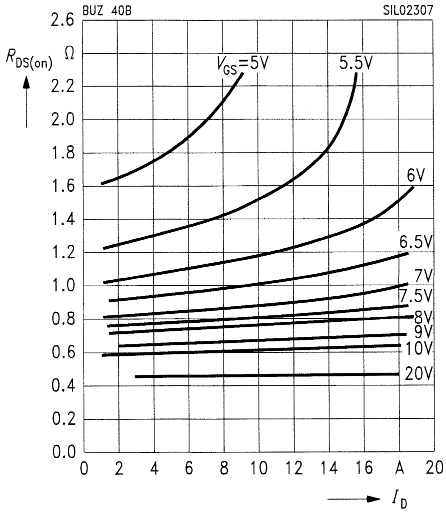
$I_D = f(V_{GS})$

parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



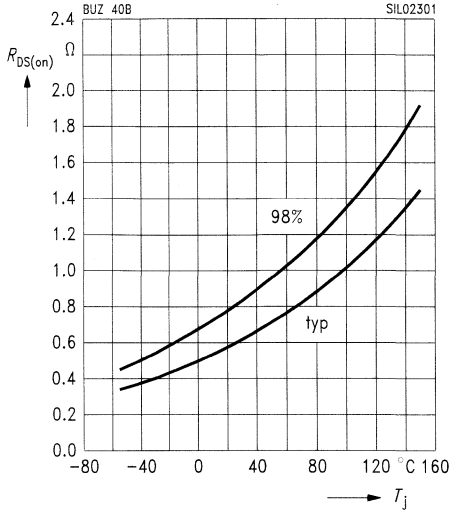
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



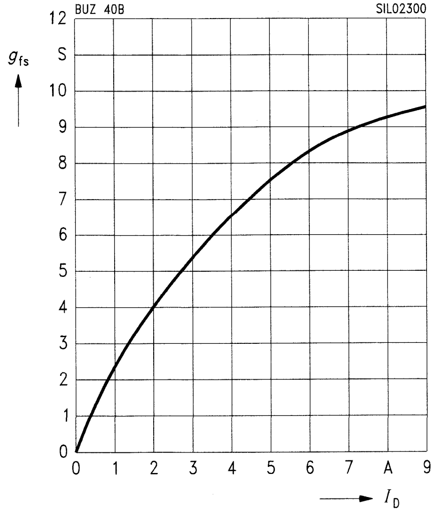
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 5,5 A, V_{GS} = 10 V, (spread)



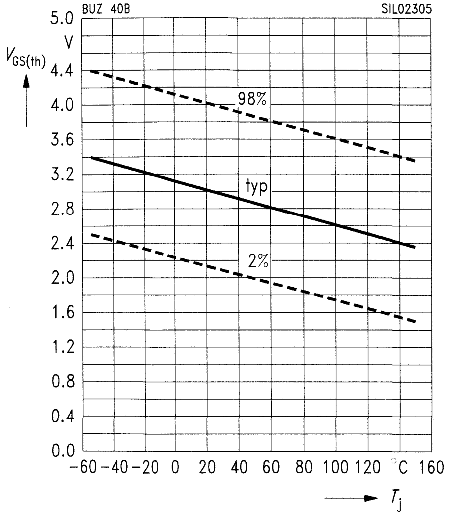
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs

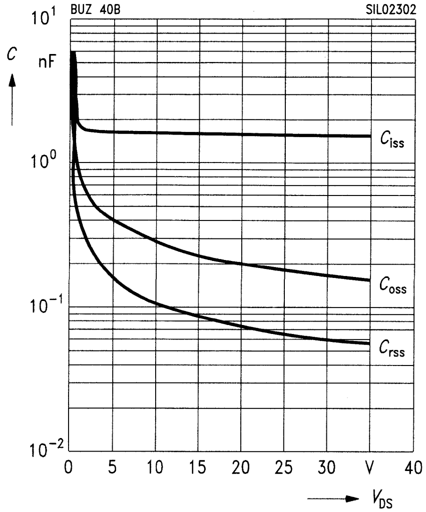


Gate threshold voltage

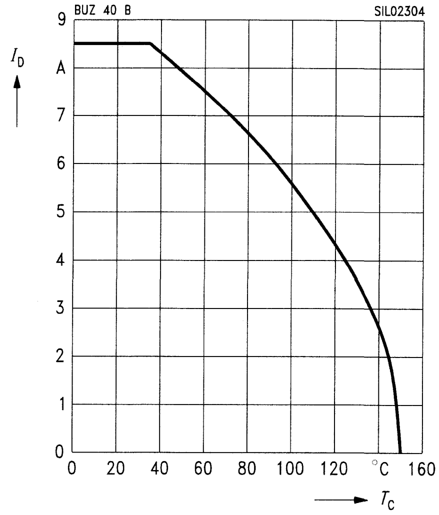
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



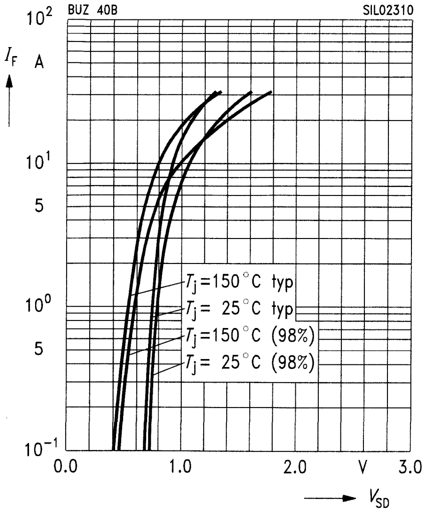
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



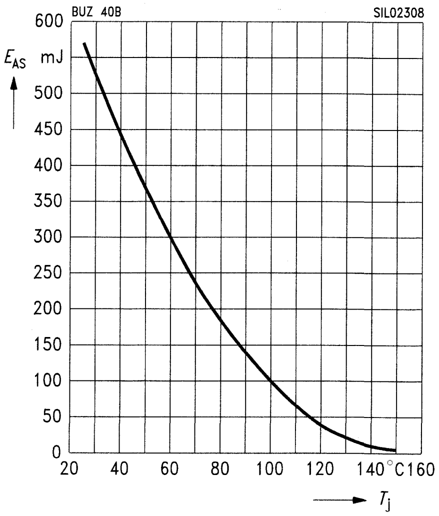
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j , $t_p = 80$ µs, (spread)



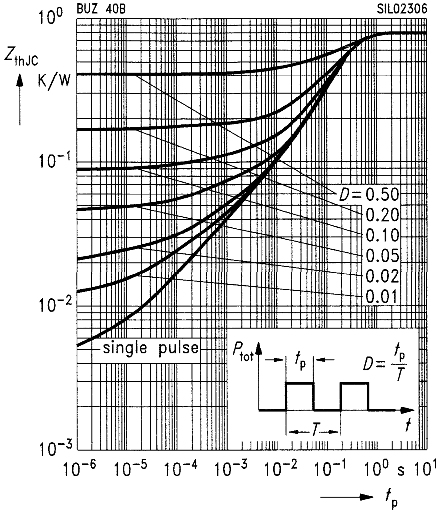
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 10$ A, $V_{DD} = 50$ V
$R_{GS} = 25\ \Omega$, $L = 10.3$ mH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

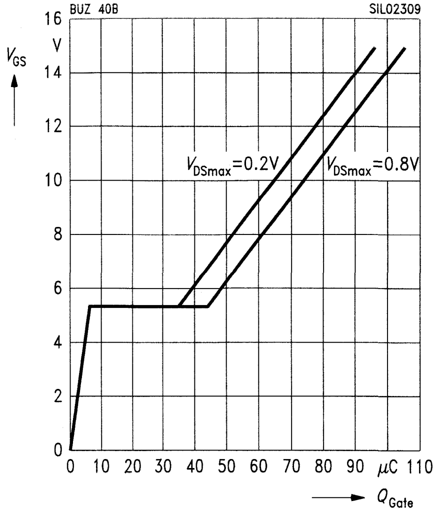
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{Gate})$

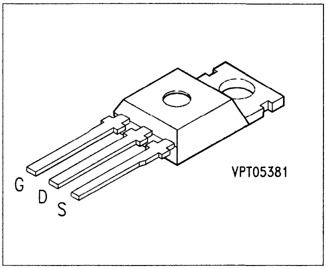
parameter: $I_{D\,puls} = 12.0$ A



SIPMOS® Power Transistor

BUZ 41 A

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package 1)	Ordering Code
BUZ 41 A	500 V	4.5 A	1.5 Ω	TO-220 AB	C67078-S1306-A3

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 36 °C	I_D	**4.5**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**18**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**4.5**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**8**	mJ
Avalanche energy, single pulse I_D = 4.5 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 28.4 mH, T_j = 25 °C	E_{AS}	**320**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	500	–	–	V
Gate threshold voltage V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 500 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 3.0 A	$R_{DS(on)}$	–	1.3	1.5	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 3.0 A	g_{fs}	2.5	4.3	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	850	1300	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	100	150	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	40	60	
Turn-on time t_{on}, ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.6 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	15	20	ns
	t_r	–	50	70	
Turn-off time t_{off}, ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.6 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	140	190	
	t_f	–	50	70	

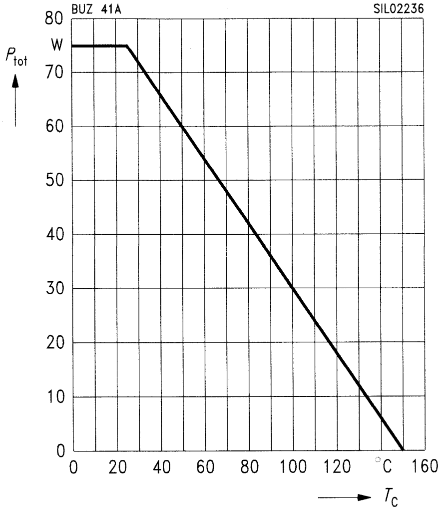
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	4.5	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	18	
Diode forward on-voltage I_S = 9 A, V_{GS} = 0 V	V_{SD}	–	1.0	1.2	V
Reverse recovery time V_R = 100 V, I_F = I_S, di_F / dt = 100 A/µs	t_{rr}	–	350	–	ns
Reverse recovery charge V_R = 100 V, I_F = I_S, di_F / dt = 100 A/µs	Q_{rr}	–	3	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Total power dissipation

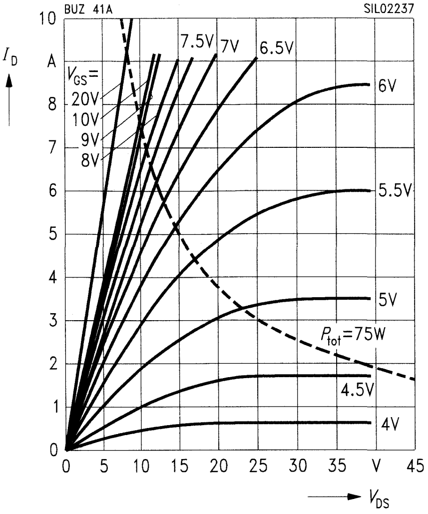
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

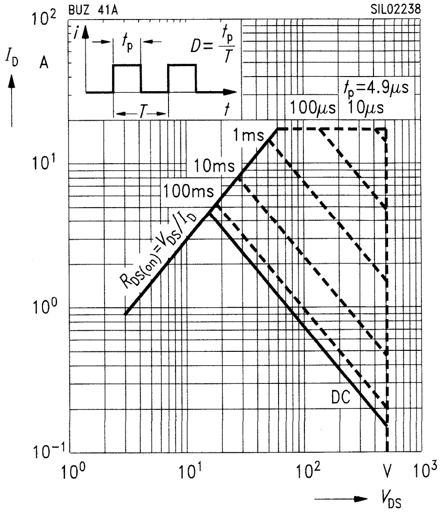
parameter: $t_p = 80$ µs



Safe operating area

$I_D = f(V_{DS})$

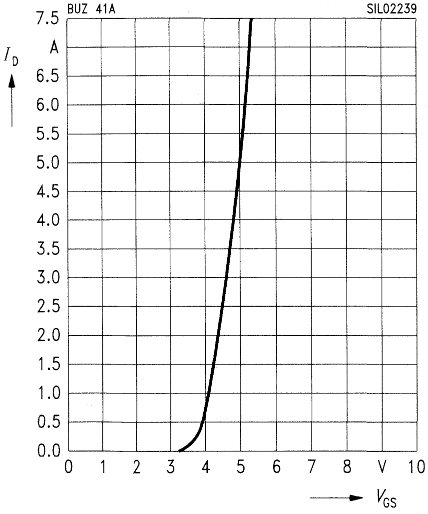
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

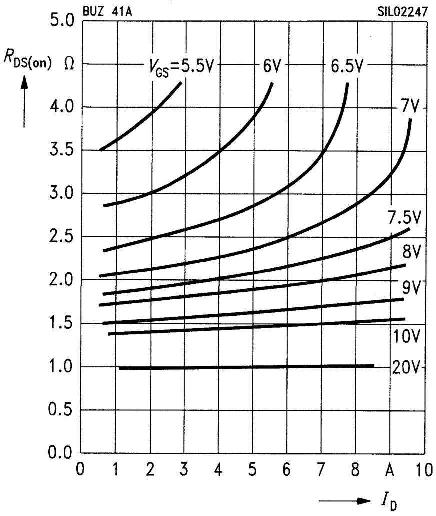
$I_D = f(V_{GS})$

parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



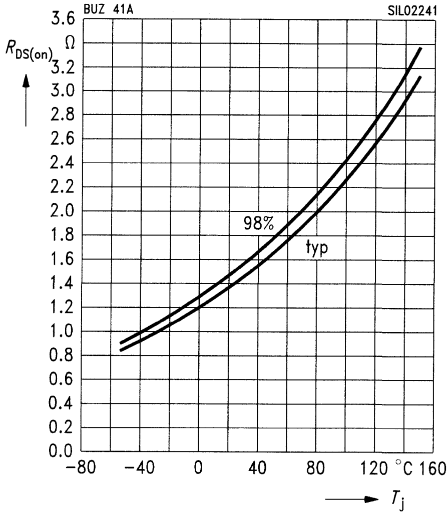
Typ. drain-source on-resistance

$R_{\mathrm{DS\,(on)}} = f\,(I_\mathrm{D})$
parameter: V_GS



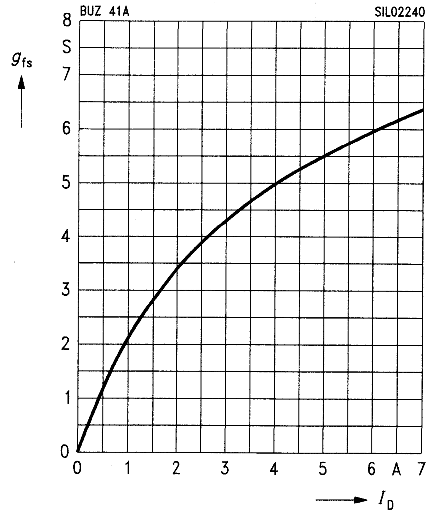
Drain-source on-resistance

$R_{\mathrm{DS\,(on)}} = f\,(T_\mathrm{j})$
parameter: I_D = 2.5 A, V_GS = 10 V, (spread)



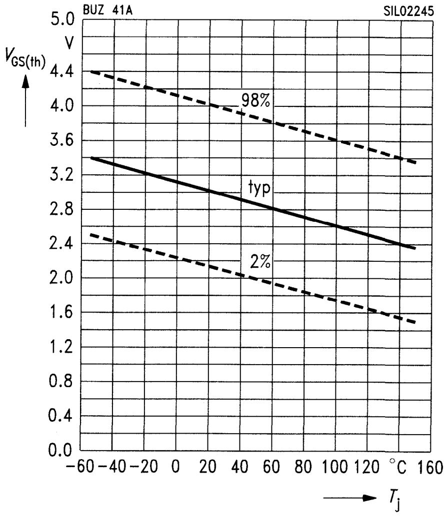
Typ. forward transconductance

$g_\mathrm{fs} = f\,(I_\mathrm{D})$
parameter: t_p = 80 µs



Gate threshold voltage

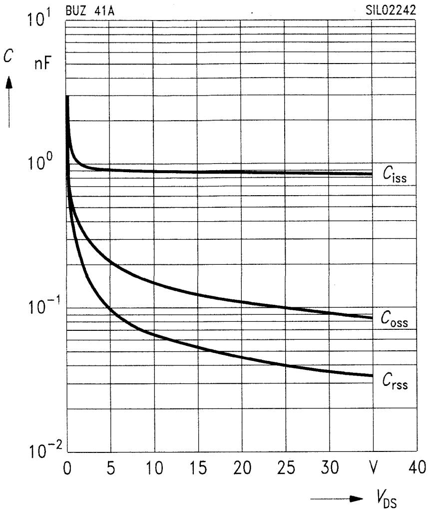
$V_{\mathrm{GS\,(th)}} = f\,(T_\mathrm{j})$
parameter: $V_\mathrm{GS} = V_\mathrm{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

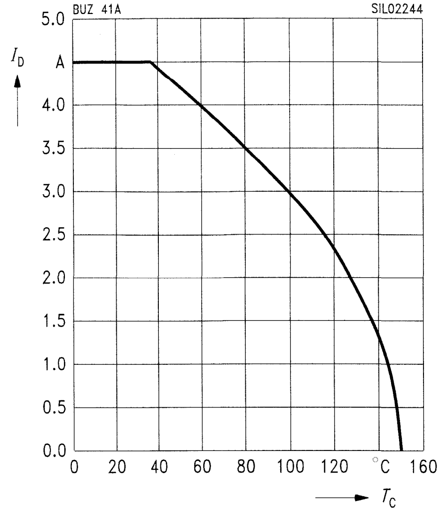
parameter: V_{GS} = 0 V, f = 1 MHz



Drain current

$I_D = f(T_C)$

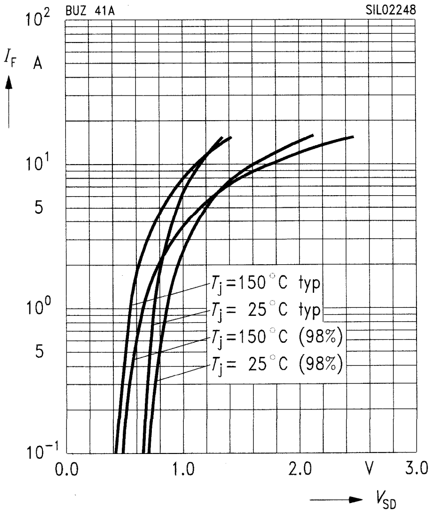
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

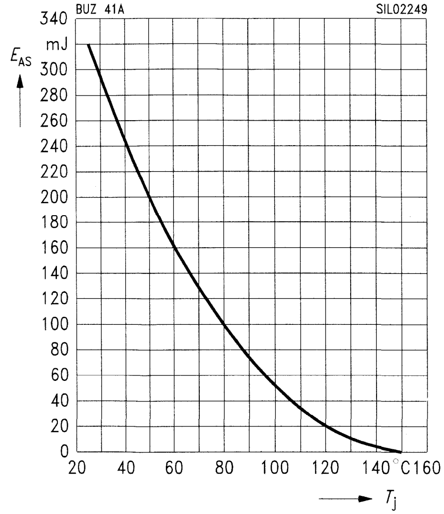
parameter: T_j , t_p = 80 µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

parameter: I_D = 4.5 A, V_{DD} = 50 V

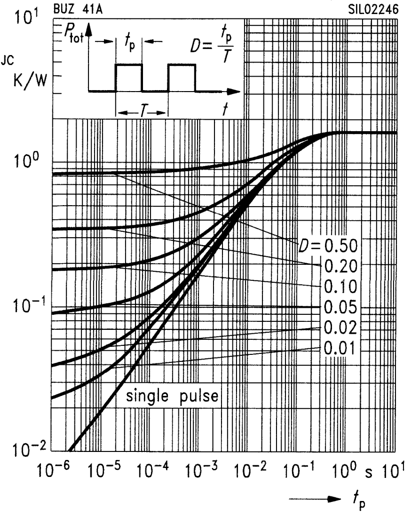
R_{GS} = 25 Ω, L = 28.4 mH



Transient thermal impedance

$Z_{\mathrm{th\,JC}} = f(t_p)$

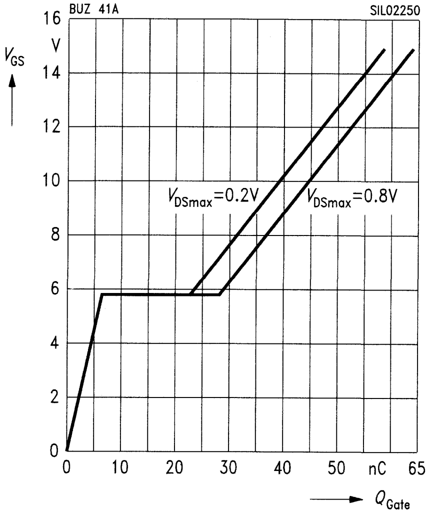
parameter: $D = t_p / T$



Typ. gate charge

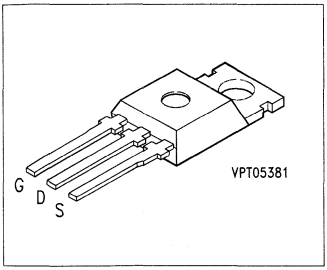
$V_{GS} = f(Q_{Gate})$

parameter: $I_{D\,puls} = 6.75$ A



SIPMOS® Power Transistor **BUZ 42**

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 42	500 V	4.0 A	2.0 Ω	TO-220 AB	C67078-S1311-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 30 °C	I_D	**4.0**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**16**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**4.0**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**6**	mJ
Avalanche energy, single pulse I_D = 4.0 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 24.8 mH, T_j = 25 °C	E_{AS}	**220**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	500	–	–	V
Gate threshold voltage V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 500 V, V_{GS} = 0 V T_j = 25 °C T_j = 125 °C	I_{DSS}	 – –	 0.1 10	 1.0 100	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 2.6 A	$R_{DS\,(on)}$	–	1.6	2.0	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 2.6 A	g_{fs}	1.5	2.8	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	600	900	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	65	100	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	25	40	
Turn-on time t_{on}, ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	10	15	ns
	t_r	–	50	70	
Turn-off time t_{off}, ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	70	95	
	t_f	–	40	55	

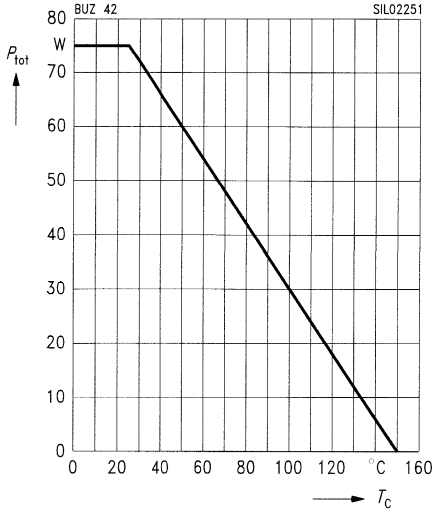
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	4.0	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	16	
Diode forward on-voltage I_S = 8.0 A, V_{GS} = 0 V	V_{SD}	–	1.0	1.4	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	300	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	2.5	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Total power dissipation

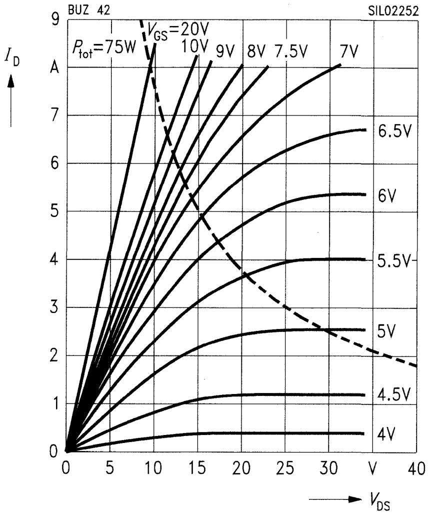
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

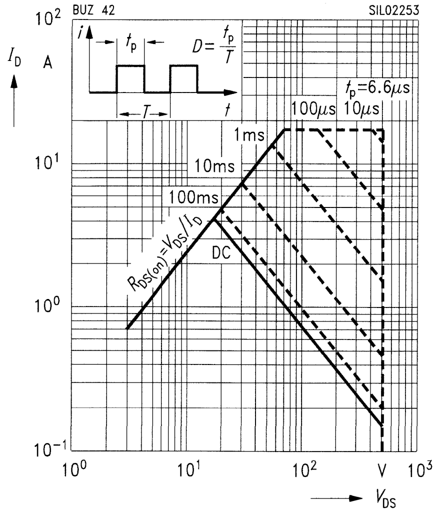
parameter: $t_p = 80$ µs



Safe operating area

$I_D = f(V_{DS})$

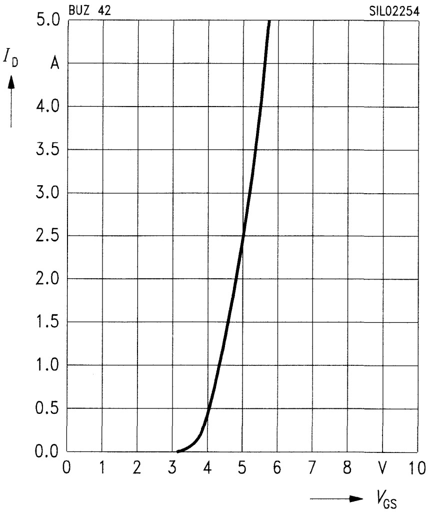
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

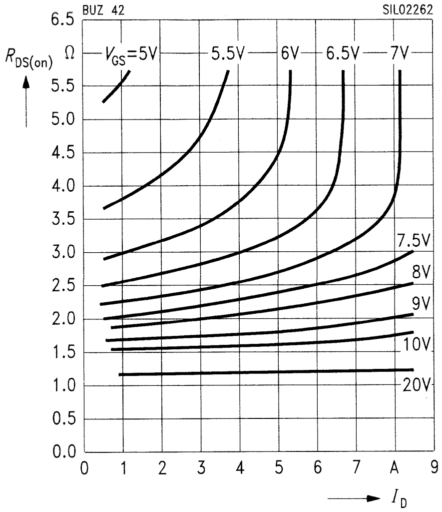
$I_D = f(V_{GS})$

parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



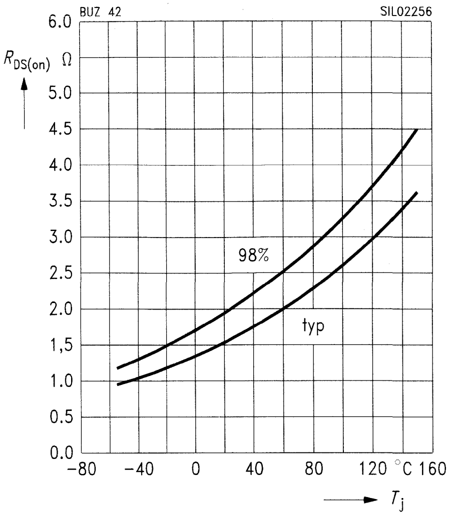
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



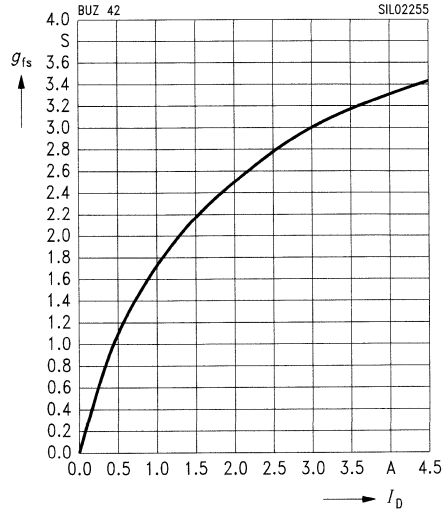
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 2.6 A, V_{GS} = 10 V, (spread)



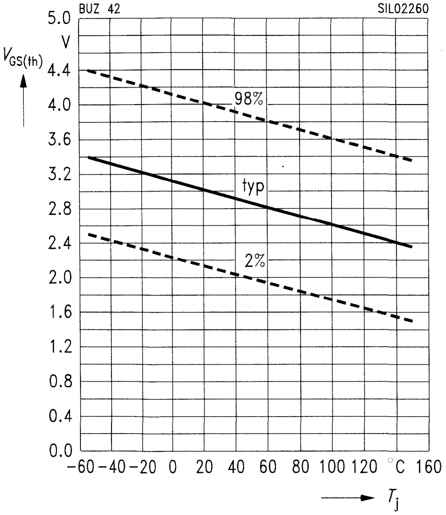
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

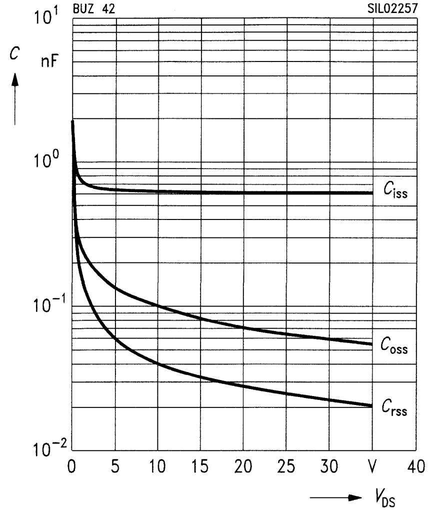
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

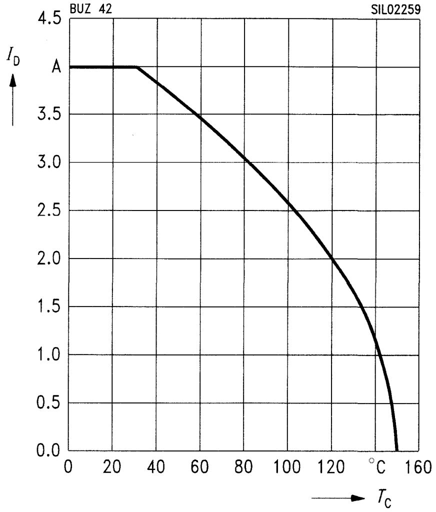
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

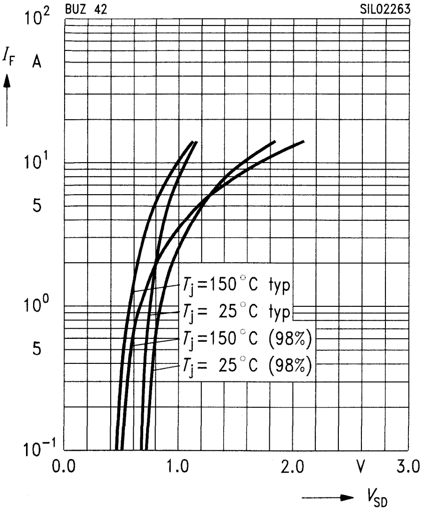
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

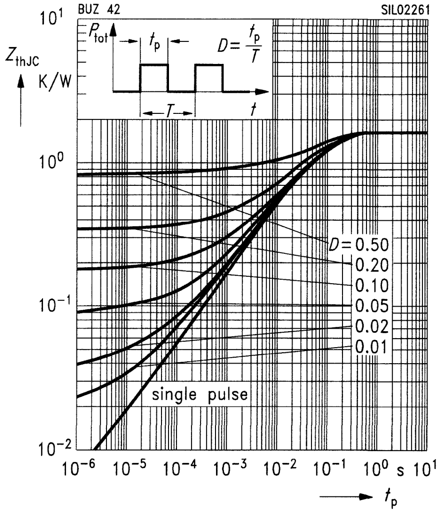
parameter: T_j , $t_p = 80$ µs, (spread)



Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

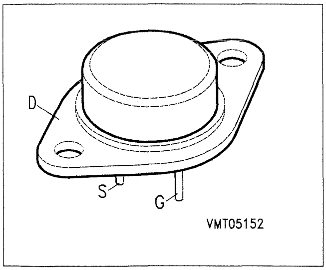
parameter: $D = t_p / T$



SIPMOS® Power Transistors

BUZ 45
BUZ 45 A, BUZ 45 B

- N channel
- Enhancement mode



Type	V_{DS}	I_D	T_C	$R_{DS(on)}$	Package [1)]	Ordering Code
BUZ 45	500 V	9.6 A	25 °C	0.6 Ω	TO-204 AA	C67078-A1008-A8
BUZ 45 A	500 V	8.3 A	25 °C	0.8 Ω	TO-204 AA	C67078-A1008-A9
BUZ 45 B	500 V	10.0 A	40 °C	0.5 Ω	TO-204 AA	C67078-A1008-A10

Maximum Ratings

Parameter	Symbol	BUZ 45	BUZ 45 A	BUZ 45 B	Unit
Continuous drain current	I_D	**9.6**	**8.3**	**10**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**38**	**33**	**40**	
Drain-source voltage	V_{DS}	**500**			V
Drain-gate voltage, R_{GS} = 20 kΩ	V_{DGR}	**500**			
Gate-source voltage	V_{GS}	**± 20**			
Power dissipation, T_C = 25 °C	P_{tot}	**125**			W
Operating and storage temperature range	T_j, T_{stg}	**– 55 ... + 150**			°C

Parameter	Symbol	Value	Unit
Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**C**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	500	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 500 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	20	250	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS(on)}$				Ω
V_{GS} = 10 V, I_D = 5 A BUZ 45		–	0.55	0.6	
BUZ 45 A		–	0.7	0.8	
BUZ 45 B		–	0.49	0.5	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 5 A	g_{fs}	2.7	5.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	3800	4900	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	250	400	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	100	170	
Turn-on time t_{on}, ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.8 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	50	75	ns
	t_r	–	80	120	
Turn-off time t_{off}, ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.8 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	330	430	
	t_f	–	110	140	

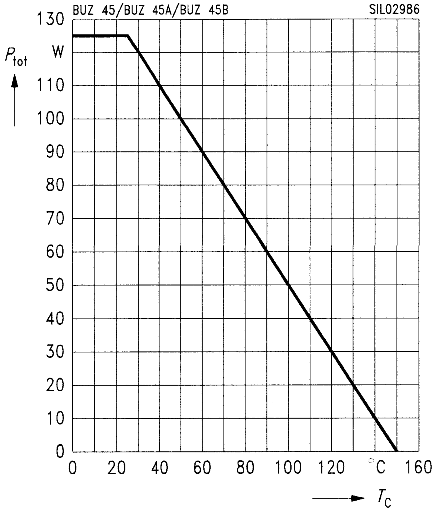
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter		Symbol	Values			Unit
			min.	typ.	max.	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 ˚C	BUZ 45		–	–	9.6	
	BUZ 45 A		–	–	8.3	
	BUZ 45 B		–	–	10	
Pulsed reverse drain current		I_{SM}				A
T_C = 25 ˚C	BUZ 45		–	–	38	
	BUZ 45 A		–	–	33	
	BUZ 45 B		–	–	40	
Diode forward on-voltage I_S = 21 A, V_{GS} = 0 V		V_{SD}	–	1.3	1.7	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		t_{rr}	–	1.2	–	µs
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		Q_{rr}	–	12	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

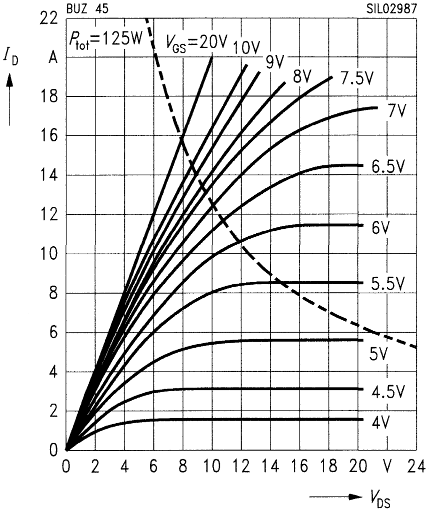
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 45**

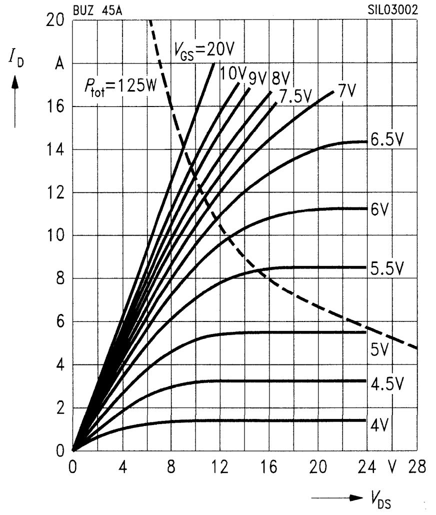
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 45 A**

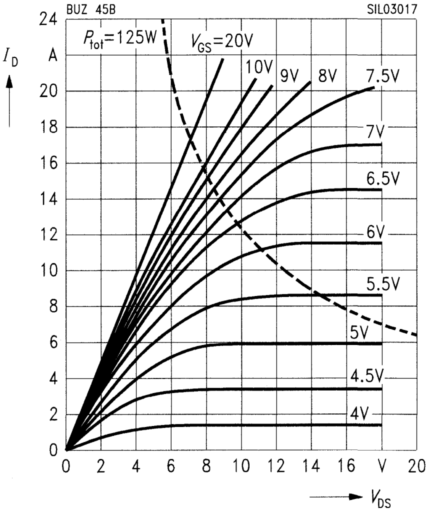
parameter: t_p = 80 µs



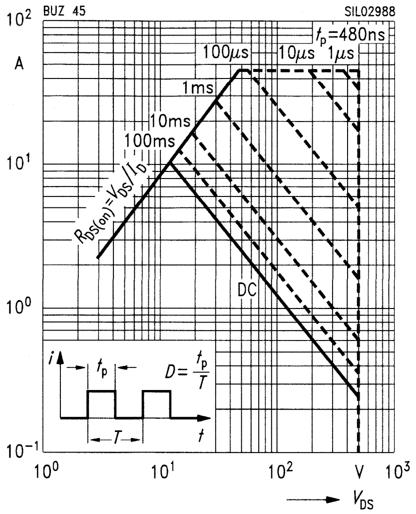
Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 45 B**

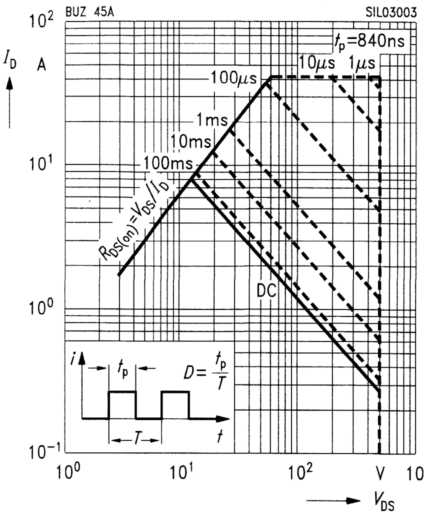
parameter: t_p = 80 µs



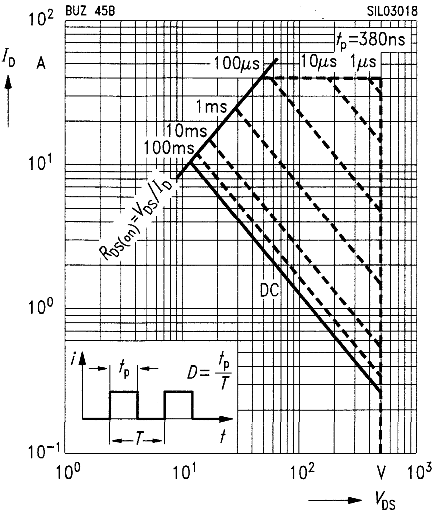
Safe operating area
$I_D = f(V_{DS})$ **BUZ 45**
parameter: $D = 0.01$, $T_C = 25$ °C



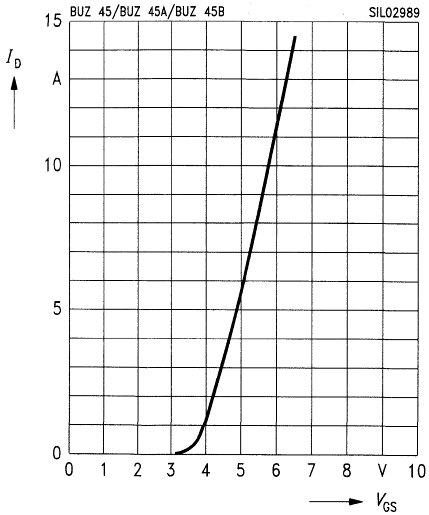
Safe operating area
$I_D = f(V_{DS})$ **BUZ 45 A**
parameter: $D = 0.01$, $T_C = 25$ °C



Safe operating area
$I_D = f(V_{DS})$ **BUZ 45 B**
parameter: $D = 0.01$, $T_C = 25$ °C

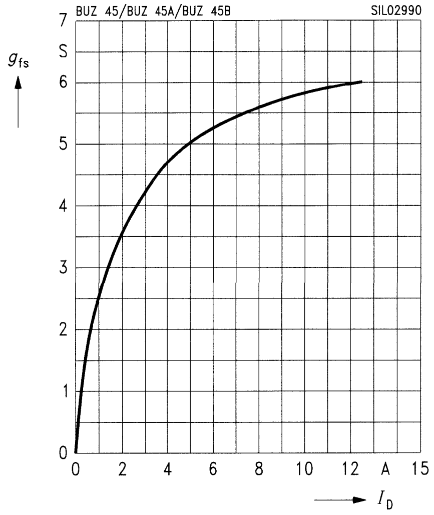


Typ. transfer characteristics
$I_D = f(V_{GS})$
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



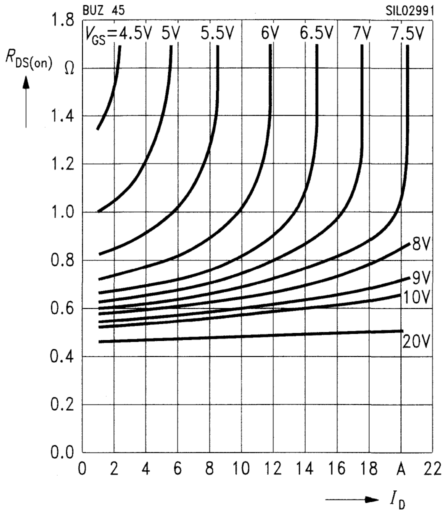
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: t_p = 80 µs



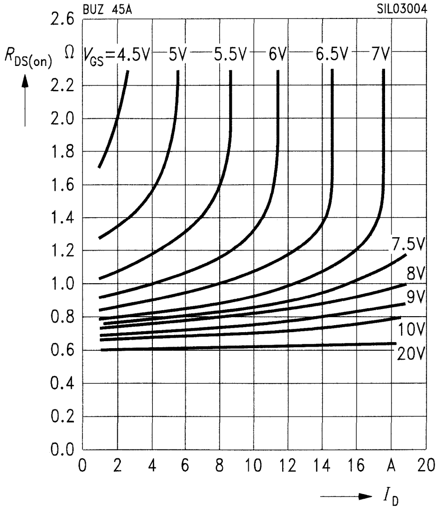
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 45**
parameter: V_{GS}



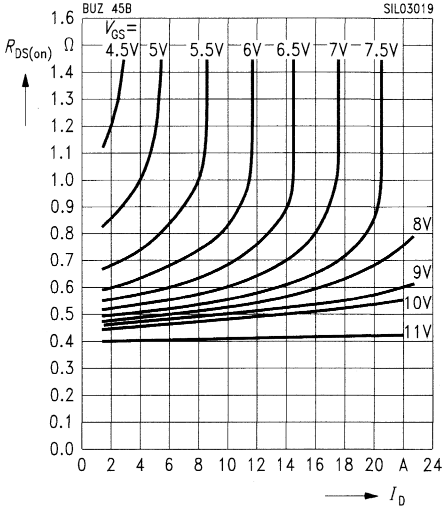
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 45 A**
parameter: V_{GS}



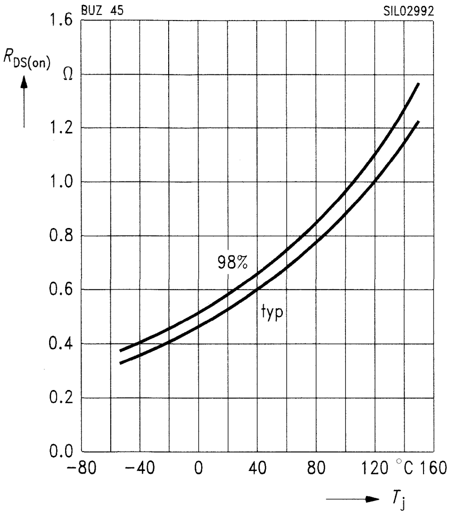
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 45 B**
parameter: V_{GS}



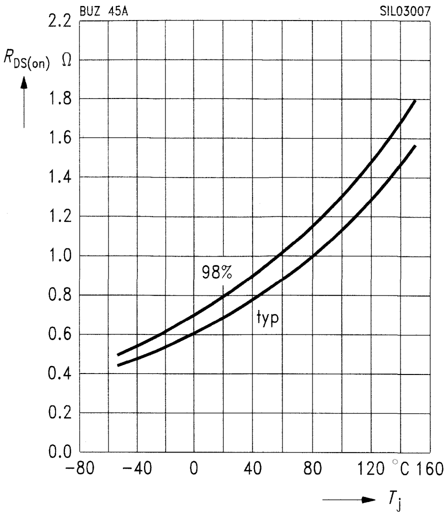
Drain-source on-resistance

$R_{DS(on)} = f(T_j)$ **BUZ 45**
parameter: I_D = 5 A, V_{GS} = 10 V



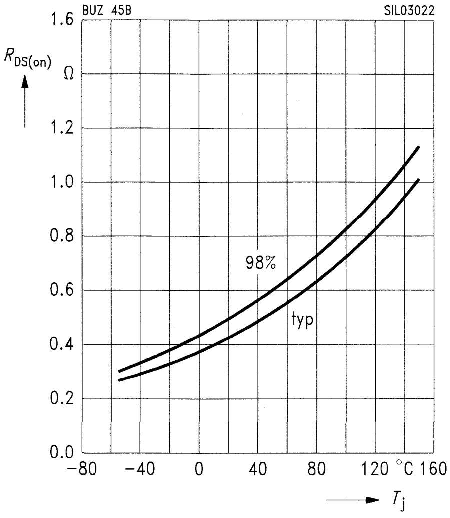
Drain-source on-resistance

$R_{DS(on)} = f(T_j)$ **BUZ 45 A**
parameter: I_D = 5 A, V_{GS} = 10 V



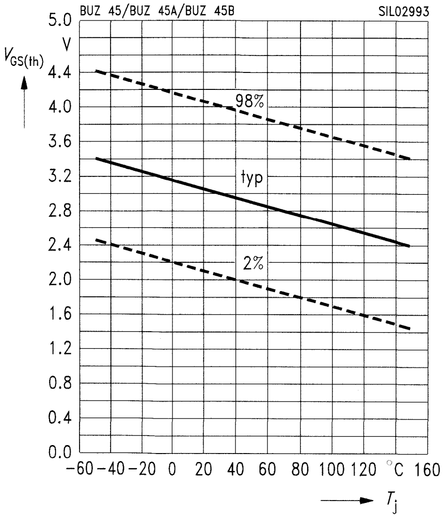
Drain-source on-resistance

$R_{DS(on)} = f(T_j)$ **BUZ 45 B**
parameter: I_D = 5 A, V_{GS} = 10 V



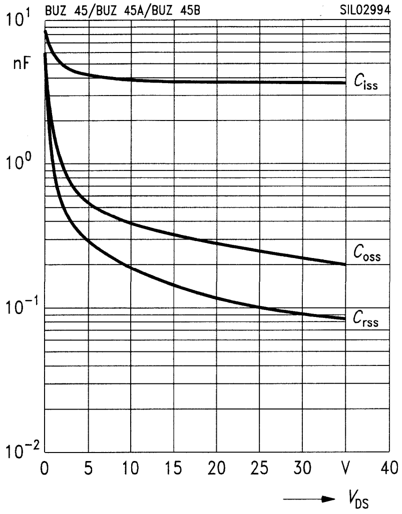
Gate threshold voltage

$V_{GS(th)} = f(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA



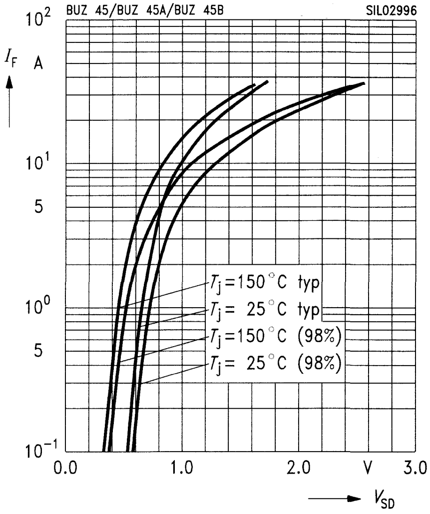
Typ. capacitances

$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



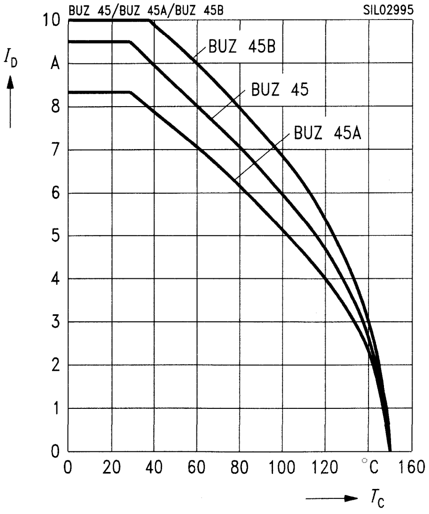
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: T_j , $t_p = 80$ µs



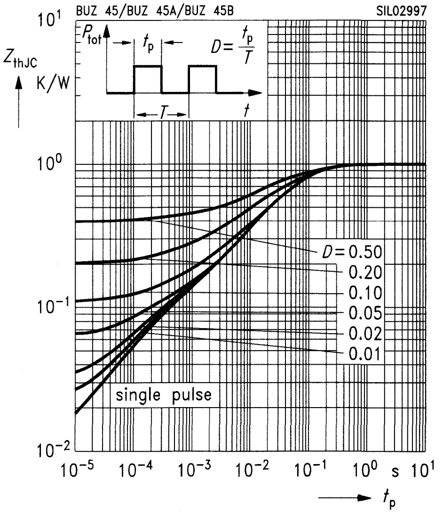
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V

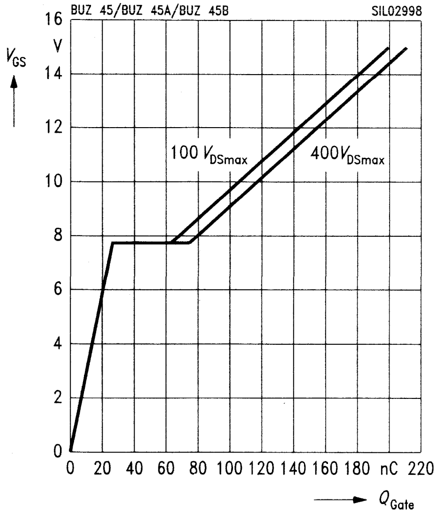


Transient thermal impedance

$Z_{thJC} = f(t_p)$
parameter: $D = t_p / T$



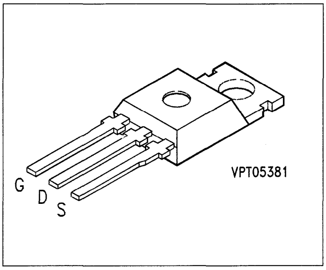
Typ. gate charge
$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 14.4$ A



SIPMOS® Power Transistors

BUZ 50 A
BUZ 50 B, BUZ 50 C

- N channel
- Enhancement mode



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 50 A	1000 V	2.5 A	5.0 Ω	TO-220 AB	C67078-A1307-A3
BUZ 50 B	1000 V	2.0 A	8.0 Ω	TO-220 AB	C67078-A1307-A4
BUZ 50 C	1000 V	2.3 A	6.0 Ω	TO-220 AB	C67078-A1307-A5

Maximum Ratings

Parameter	Symbol	BUZ			Unit
		50 A	50 B	50 C	
Continuous drain current $T_C = 25$ °C	I_D	**2.5**	**2.0**	**2.3**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**10.0**	**8.0**	**9.0**	
Drain-source voltage	V_{DS}	**1000**			V
Drain-gate voltage, $R_{GS} = 20$ kΩ	V_{DGR}	**1000**			
Gate-source voltage	V_{GS}	**± 20**			
Power dissipation, $T_C = 25$ °C	P_{tot}	**75**			W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**			°C

Parameter	Symbol	Value	Unit
Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	1000	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} =1000 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	20	250	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS(on)}$				Ω
V_{GS} = 10 V, I_D = 1.5 A BUZ 50 A		–	4.5	5.0	
I_D = 1.5 A BUZ 50 B		–	6.5	8.0	
I_D = 1.5 A BUZ 50 C		–	5.0	6.0	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D =1.5 A	g_{fs}	0.7	1.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1600	2100	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	70	120	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	30	55	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	30	45	ns
	t_r	–	40	60	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	110	140	
	t_f	–	60	80	

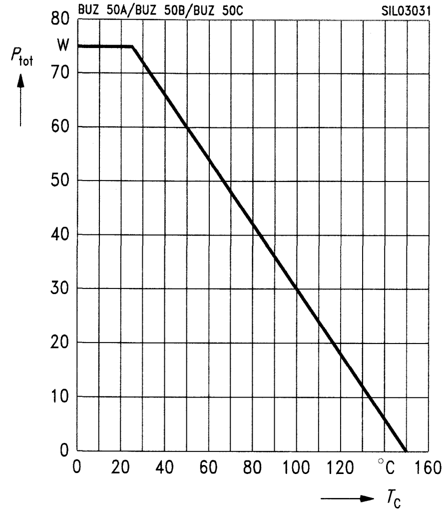
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter		Symbol	Values			Unit
			min.	typ.	max.	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 °C	BUZ 50 A		–	–	2.5	
	BUZ 50 B		–	–	2.0	
	BUZ 50 C		–	–	2.3	
Pulsed reverse drain current		I_{SM}				A
T_C = 25 °C	BUZ 50 A		–	–	10.0	
	BUZ 50 B		–	–	8.0	
	BUZ 50 C		–	–	9.0	
Diode forward on-voltage I_S = 6 A, V_{GS} = 0 V		V_{SD}	–	1.05	1.3	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		t_{rr}	–	2.0	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		Q_{rr}	–	15	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

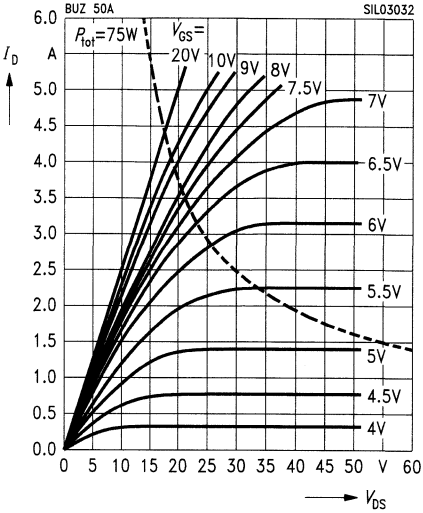
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 50 A**

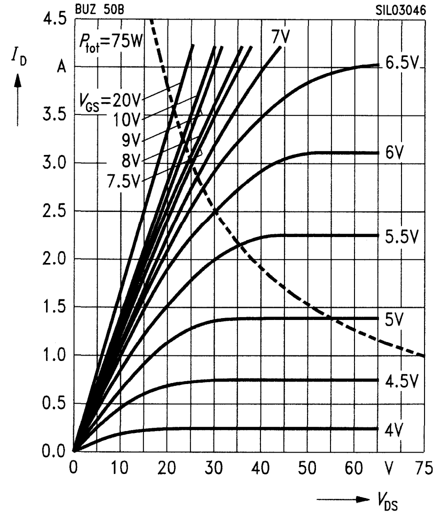
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 50 B**

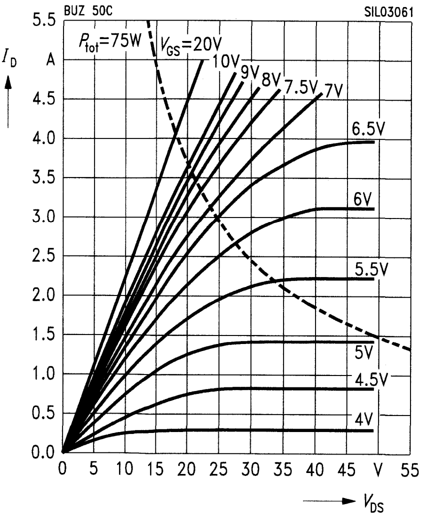
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 50 C**

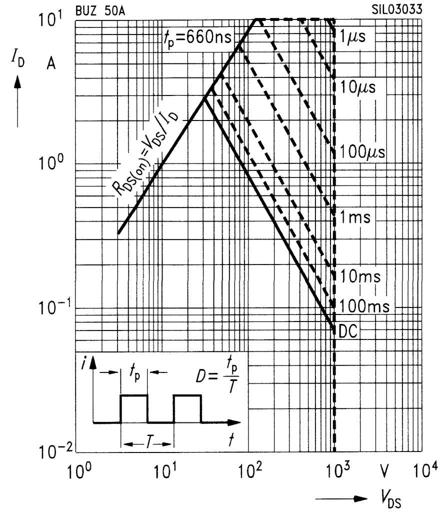
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$ **BUZ 50 A**

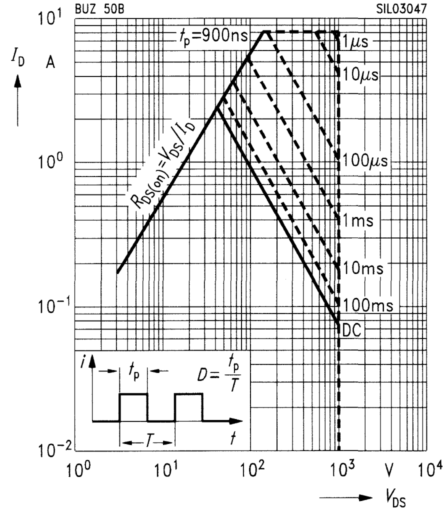
parameter: D = 0.01, T_C = 25 °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 50 B**

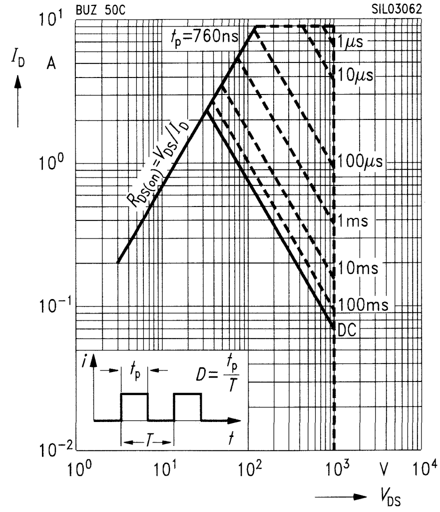
parameter: D = 0.01, T_C = 25 °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 50 C**

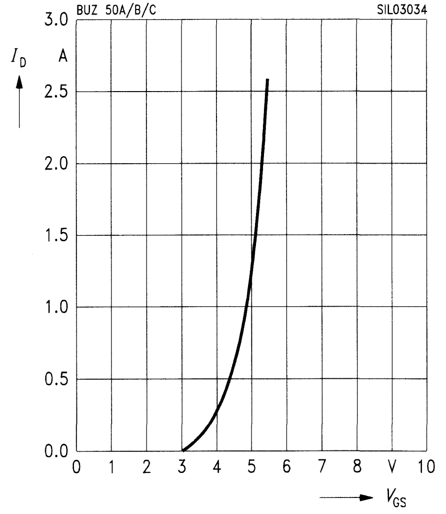
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

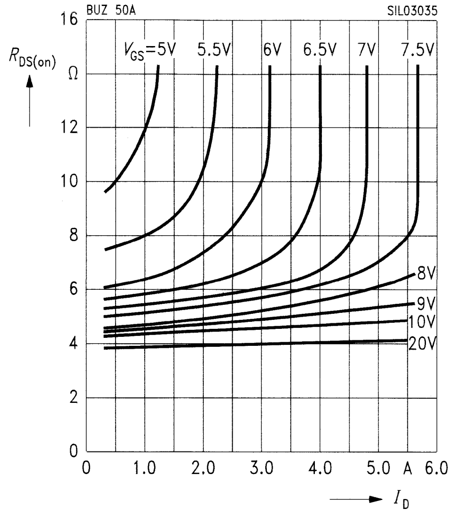
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



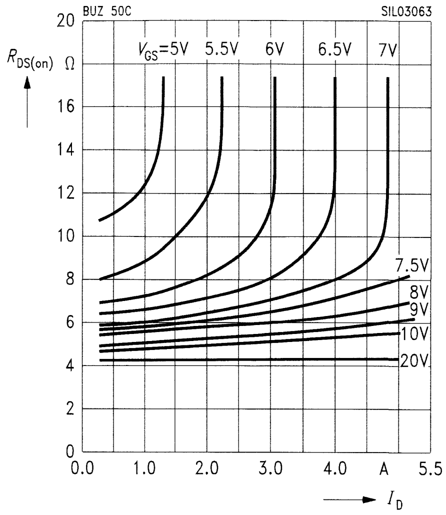
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 50 A**
parameter: V_{GS}



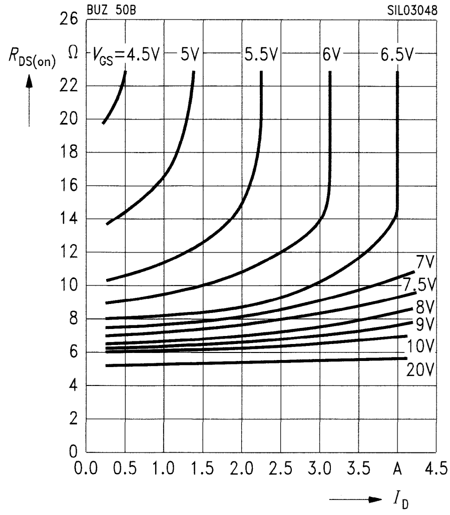
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 50 C**
parameter: V_{GS}



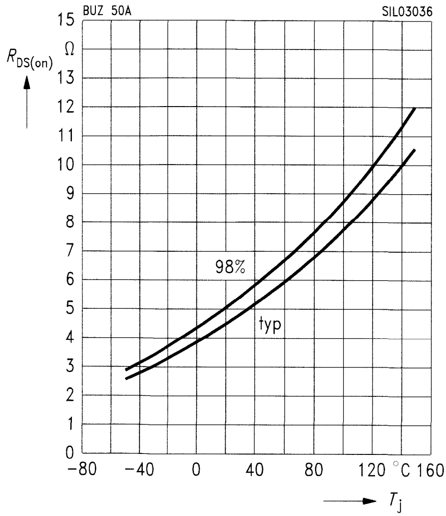
Drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 50 B**
parameter: V_{GS}



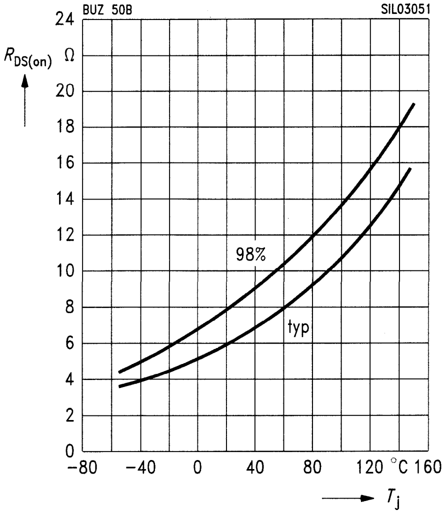
Drain-source on-resistance

$R_{DS\,(on)} = f\,(Tj)$ **BUZ 50 A**
parameter: V_{GS} = 10 V, I_D = 1.5 A



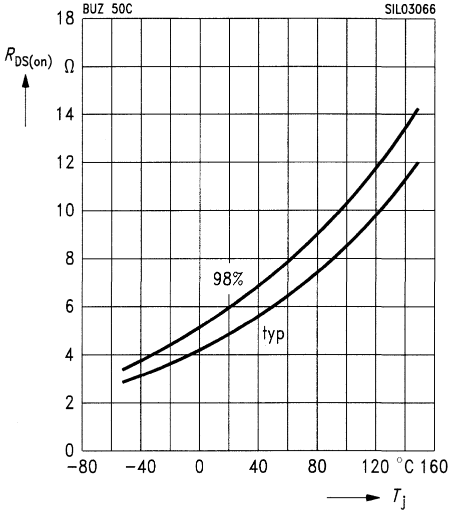
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 50 B**
parameter: V_{GS} = 10 V, I_D = 1.5 A



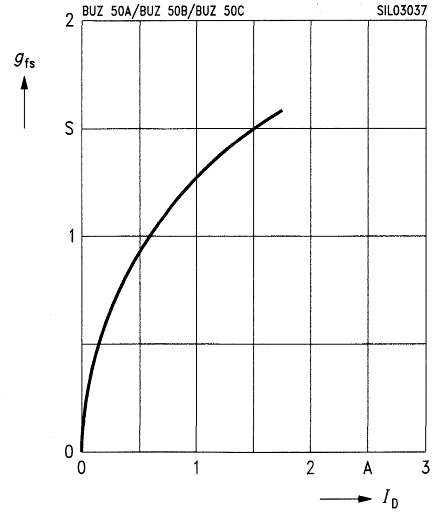
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 50 C**
parameter: V_{GS} = 10 V, I_D = 1.5 A



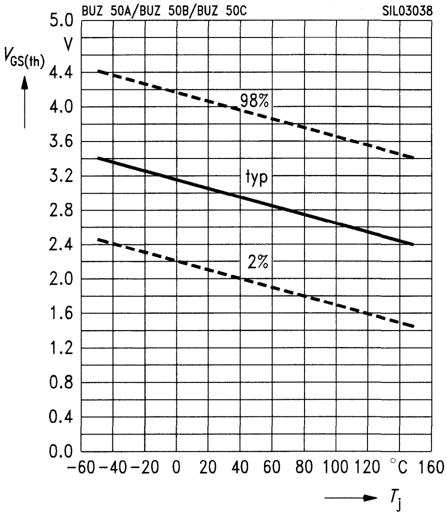
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

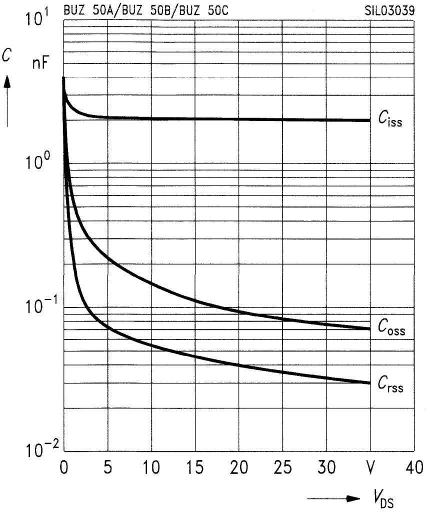
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

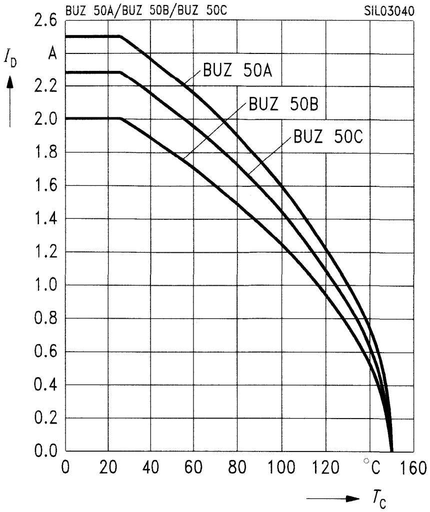
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

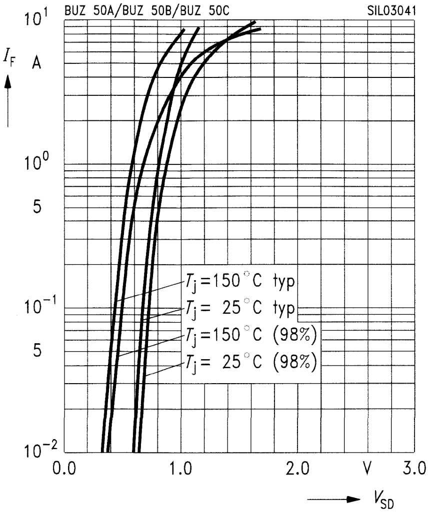
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

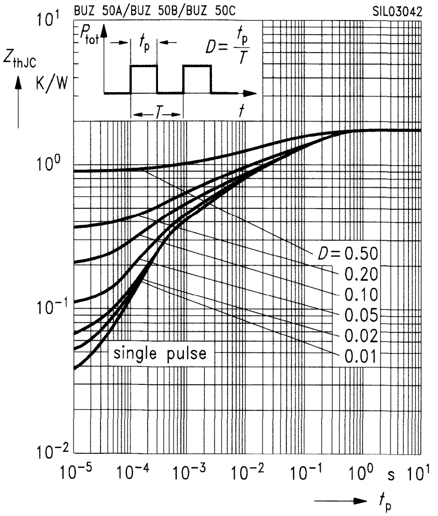
parameter: T_j, $t_p = 80$ µs, (spread)



Transient thermal impedance

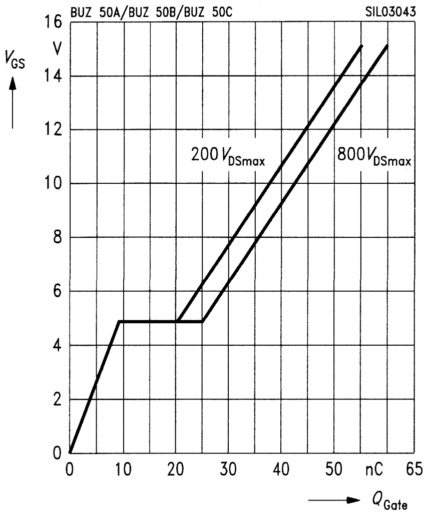
$Z_{th\,JC} = f(t_p)$

parameter: $D = t_p / T$



Typ. gate charge

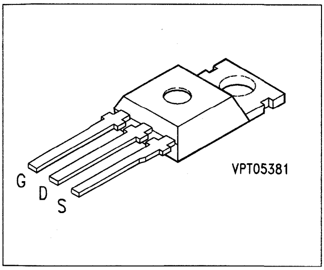
$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls}$ = 3.75 A



SIPMOS® Power Transistor

BUZ 51

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS(on)}$	**Package** [1]	**Ordering Code**
BUZ 51	1000 V	3.4 A	4.0 Ω	TO-220 AB	C67078-S1344-A2

Maximum Ratings

Parameter	**Symbol**	**Values**	**Unit**
Continuous drain current, T_C = 29 °C	I_D	**3.4**	A
Pulsed drain current, T_C = 25 °C	$I_{D\ puls}$	**13.5**	
Avalanche current, limited by $T_{j\ max}$	I_{AR}	**3.4**	
Avalanche energy, periodic limited by $T_{j\ (max)}$	E_{AR}	**12.0**	mJ
Avalanche energy, single pulse I_D = 3.4 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 67 mH, T_j = 25 °C	E_{AS}	**410**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\ JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	1000	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 1000 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 ˚C		–	0.1	1.0	
T_j = 125 ˚C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 2.2 A	$R_{DS\,(on)}$	–	3.6	4.0	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 2.2 A	g_{fs}	1.0	3.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	980	1300	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	85	130	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	45	70	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.1 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	15	25	ns
	t_r	–	70	105	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.1 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	175	235	
	t_f	–	70	95	

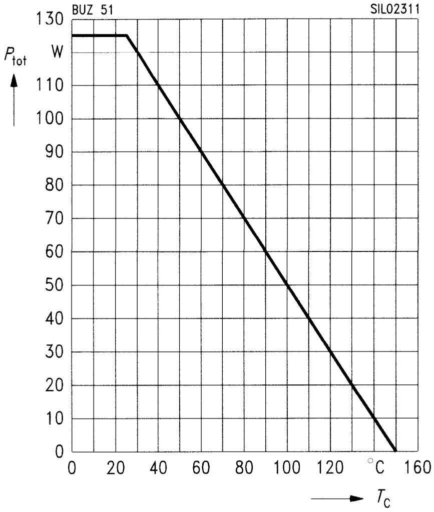
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	3.4	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	13.5	
Diode forward on-voltage I_S = 6.8 A, V_{GS} = 0 V	V_{SD}	–	0.95	1.4	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	0.3	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	2.5	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

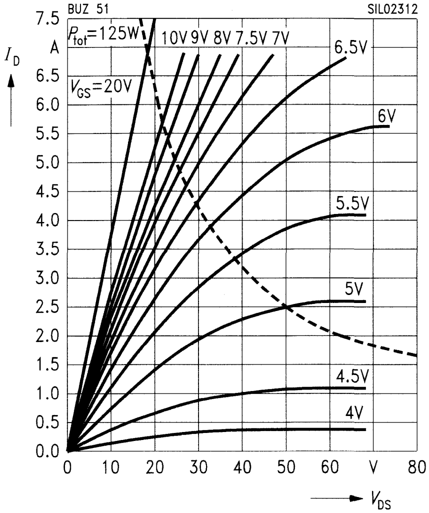
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

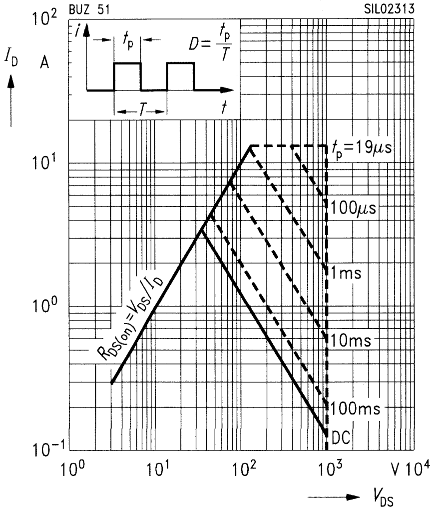
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

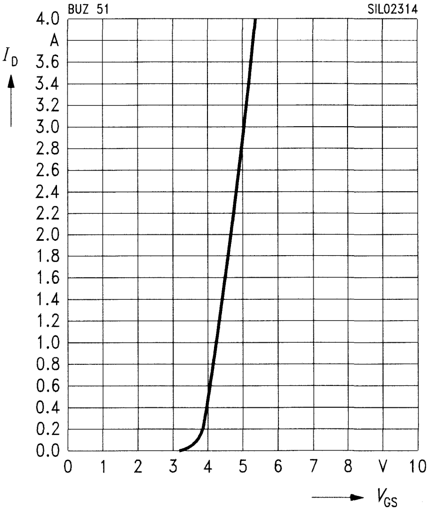
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

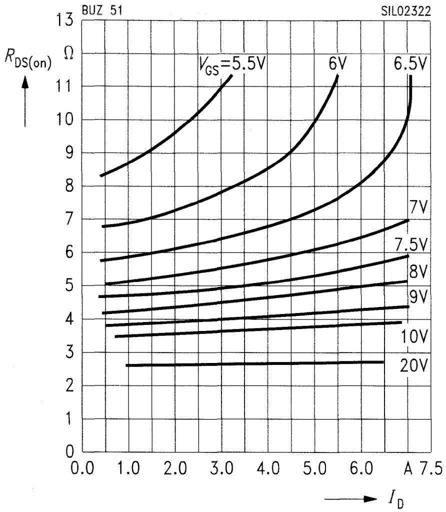
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

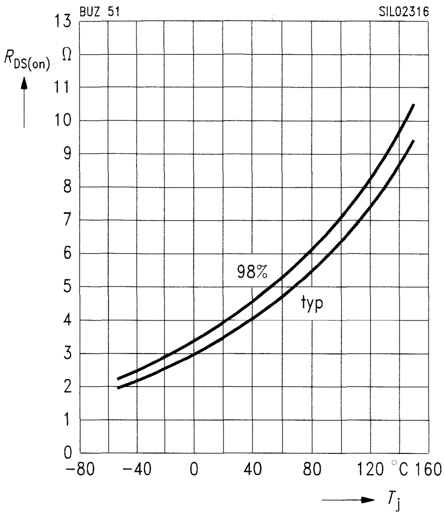
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

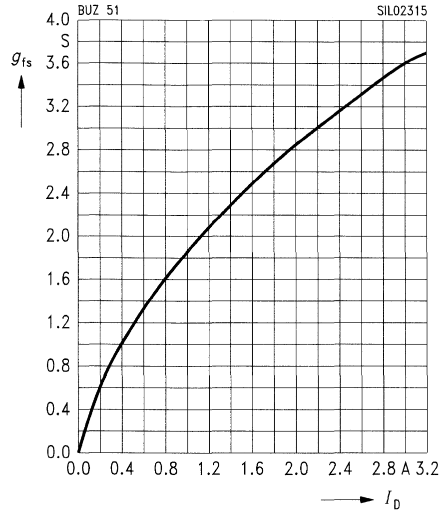
parameter: I_D = 2.2 A, V_{GS} = 10 V, (spread)



Typ. forward transconductance

$g_{fs} = f\,(I_D)$

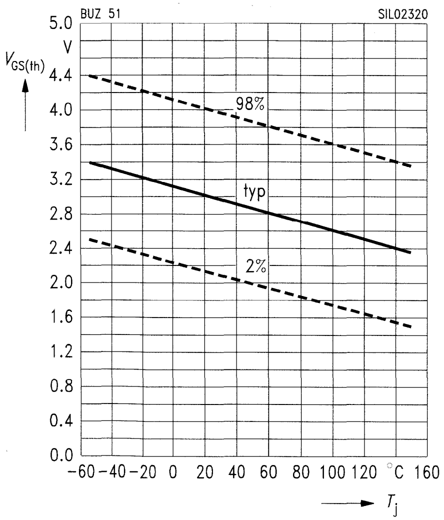
parameter: t_p = 80 µs



Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

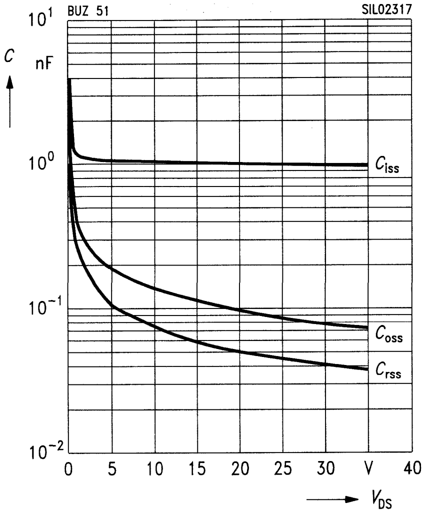
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

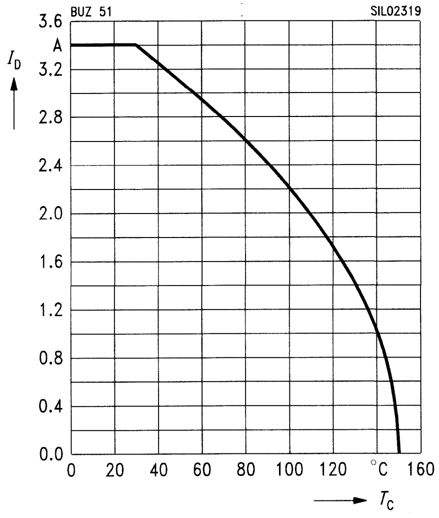
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

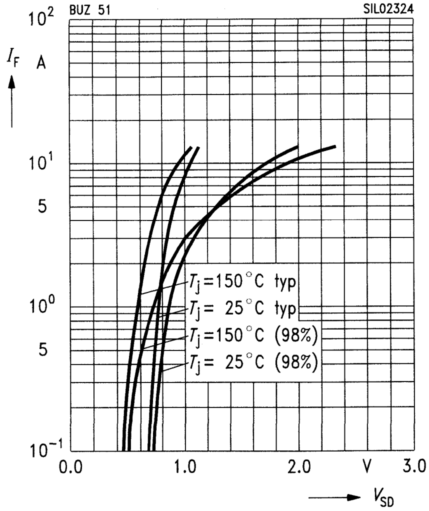
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

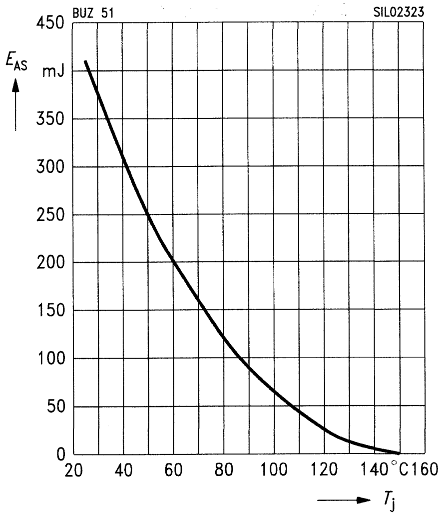
parameter: T_j, $t_p = 80$ µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

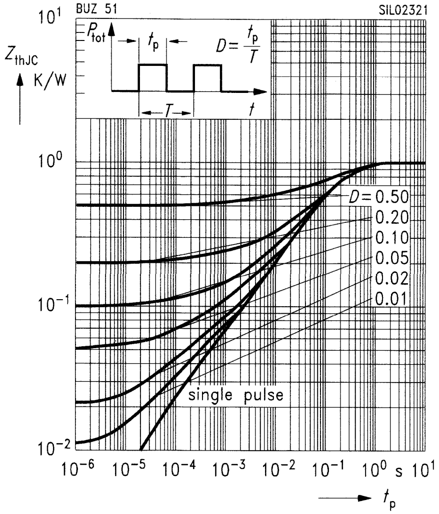
parameter: $I_D = 3.4$ A, $V_{DD} = 50$ V

$R_{GS} = 25\ \Omega$, $L = 67$ mH



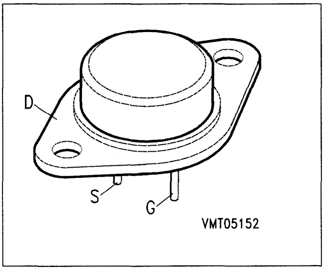
Transient thermal impedance

$Z_{\mathrm{th\,JC}} = f\,(t_p)$
parameter: $D = t_p\,/\,T$



SIPMOS® Power Transistor **BUZ 53 A**

- N channel
- Enhancement mode



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 53 A	1000 V	2.5 A	5.0 Ω	TO-204 AA	C67078-A1009-A3

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current T_C = 25 °C	I_D	**2.5**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**10.0**	
Drain-source voltage	V_{DS}	**1000**	V
Drain-gate voltage, R_{GS} = 20 kΩ	V_{DGR}	**1000**	
Gate-source voltage	V_{GS}	**± 20**	
Power dissipation, T_C = 25 °C	P_{tot}	**78**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.6**	K/W
DIN humidity category, DIN 40 040		**C**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	1000	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} =1000 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	20	250	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 1.5 A	$R_{DS(on)}$	–	4.5	5.0	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D =1.5 A	g_{fs}	0.7	1.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1600	2100	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	70	120	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	30	55	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	30	45	ns
	t_r	–	40	60	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	110	140	
	t_f	–	60	80	

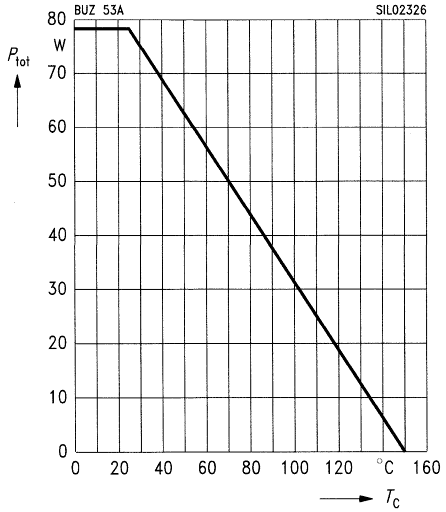
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	2.5	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	10.0	A
Diode forward on-voltage I_S = 6 A, V_{GS} = 0 V	V_{SD}	–	1.05	1.3	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	2.0	–	µs
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	15	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

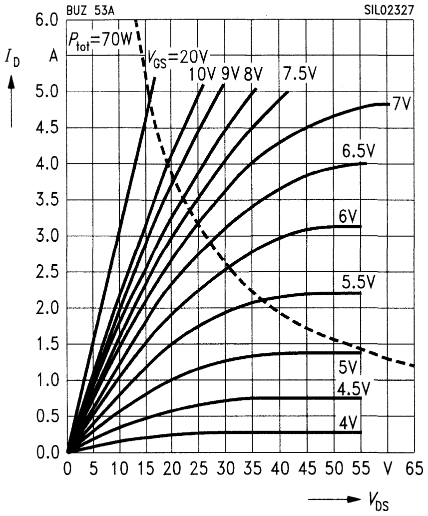
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

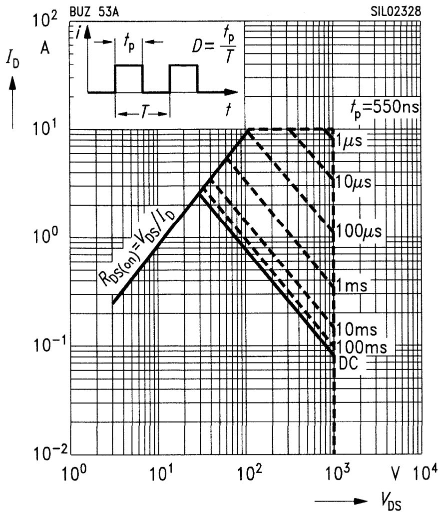
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

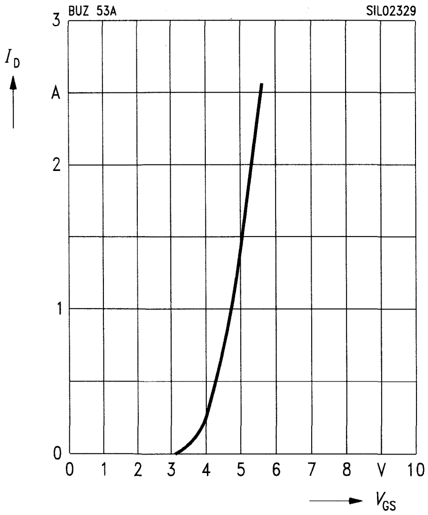
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

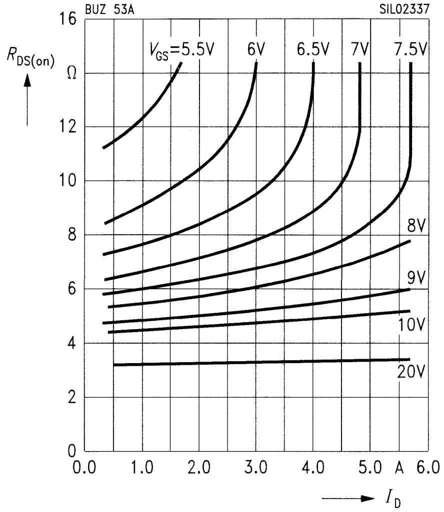
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



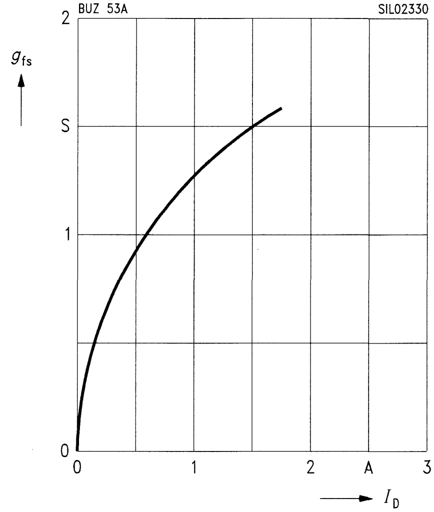
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



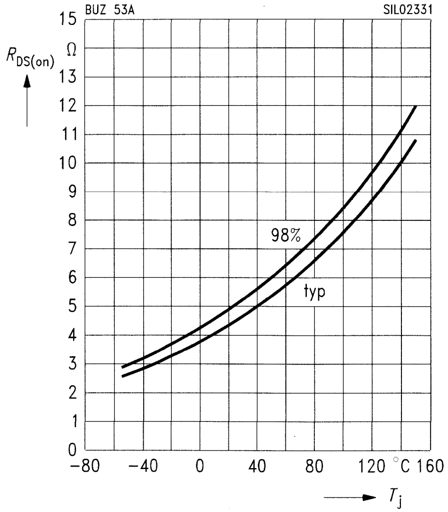
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



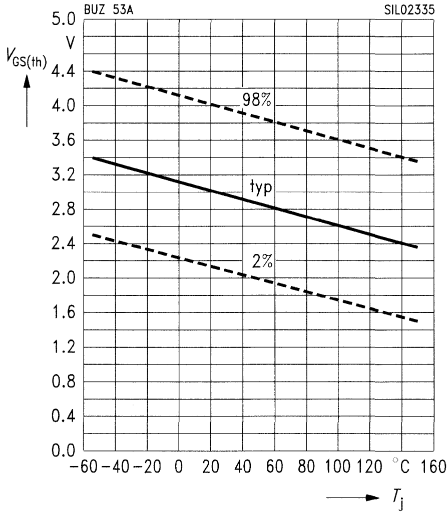
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: V_{GS} = 10 V, I_D = 1.5 A



Gate threshold voltage

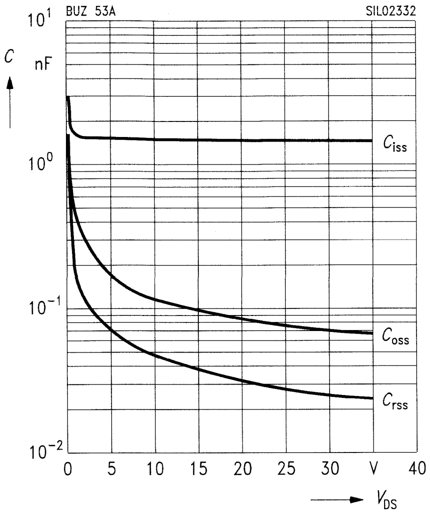
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

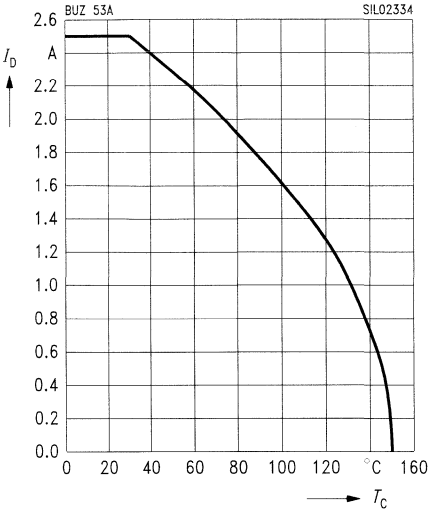
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

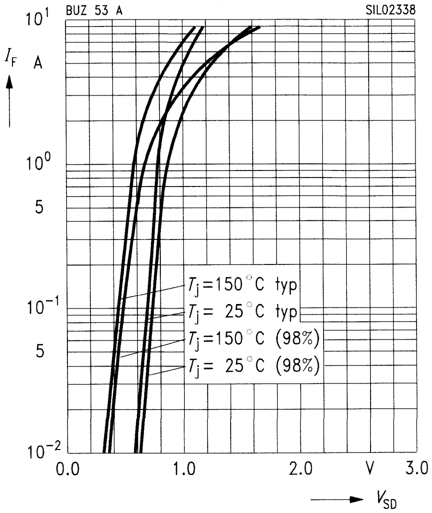
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

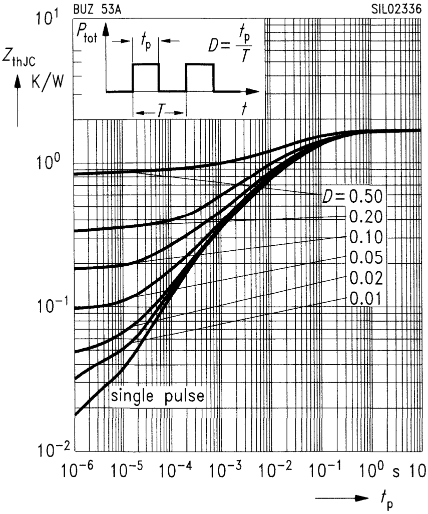
parameter: T_j, $t_p = 80$ µs, (spread)



Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

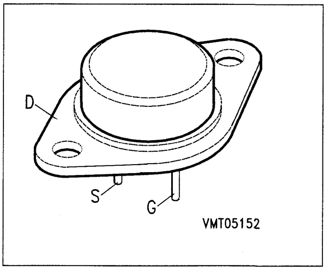
parameter: $D = t_p / T$



SIPMOS® Power Transistors

BUZ 54
BUZ 54 A

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 54	1000 V	5.1 A	2.0 Ω	TO-204 AA	C67078-S1010-A2
BUZ 54 A	1000 V	4.5 A	2.6 Ω	TO-204 AA	C67078-S1010-A3

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		54	**54 A**	
Continuous drain current, T_C = 25 ˚C	I_D	**5.1**	**4.5**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**20**	**18**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**5.1**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**18**		mJ
Avalanche energy, single pulse I_D = 5.1 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 62 mH, T_j = 25 ˚C	E_{AS}	**850**		
Gate-source voltage	V_{GS}	**± 20**		V
Power dissipation, T_C = 25 ˚C	P_{tot}	**125**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**C**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	1000	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 1000 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS\,(on)}$				Ω
V_{GS} = 10 V, I_D = 3.2 A BUZ 54		–	1.7	2.0	
BUZ 54 A		–	2.3	2.6	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 3.2 A	g_{fs}	2.5	5.2	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1700	2200	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	170	300	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	80	40	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	30	45	ns
	t_r	–	100	160	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	400	520	
	t_f	–	130	170	

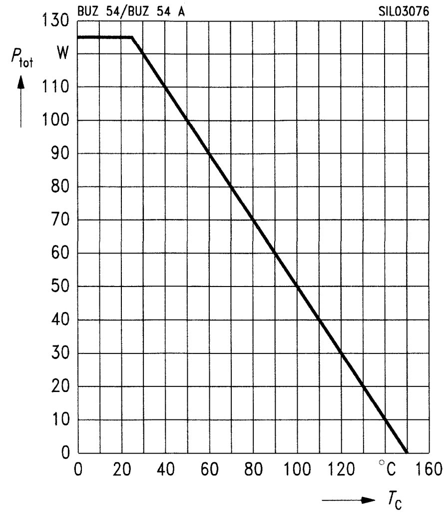
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter		**Symbol**	**Values**			**Unit**
			min.	**typ.**	**max.**	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 °C	BUZ 54		–	–	5.1	
	BUZ 54 A		–	–	4.5	
Pulsed reverse drain current		I_{SM}				
T_C = 25 °C	BUZ 54		–	–	20	
	BUZ 54 A		–	–	18	
Diode forward on-voltage I_S =10 A, V_{GS} = 0 V		V_{SD}	–	1.0	1.2	V
Reverse recovery time V_R = 100 V, I_F = I_S , di_F / dt = 100 A/µs		t_{rr}	–	1.5	–	µs
Reverse recovery charge V_R = 100 V, I_F = I_S , di_F / dt = 100 A/µs		Q_{rr}	–	6.5	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

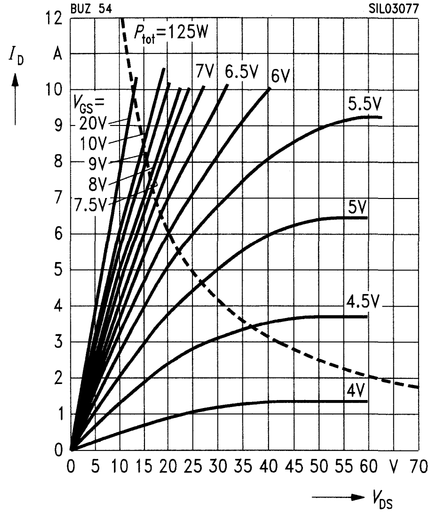
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 54**

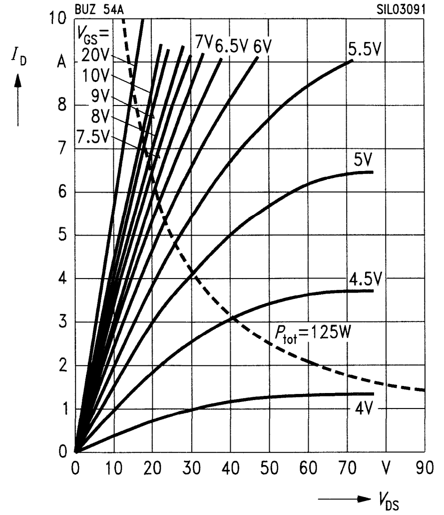
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 54 A**

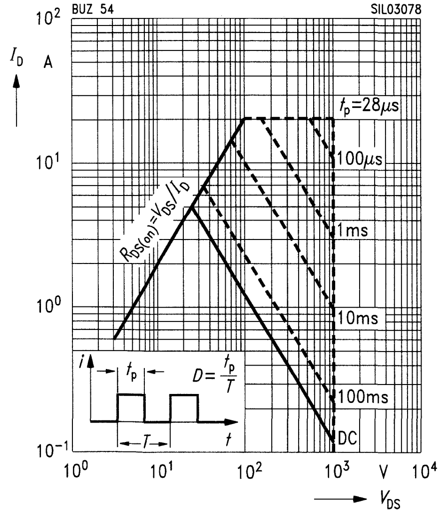
parameter: t_p = 80 µs



Safe operating area

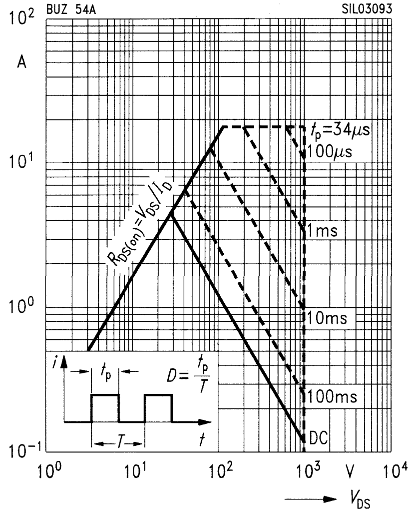
$I_D = f(V_{DS})$ **BUZ 54**

parameter: D = 0.01, T_C = 25 °C



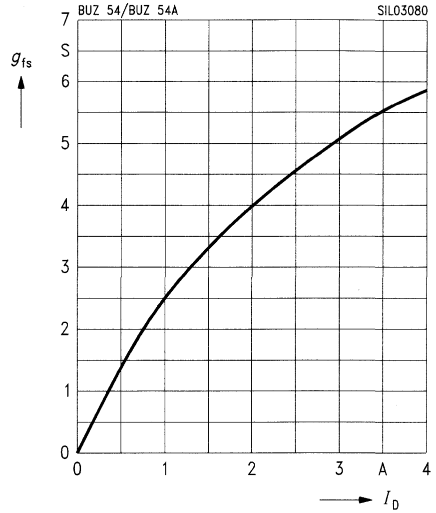
Safe operating area

$I_D = f(V_{DS})$ **BUZ 54 A**
parameter: $D = 0.01$, $T_C = 25$ °C



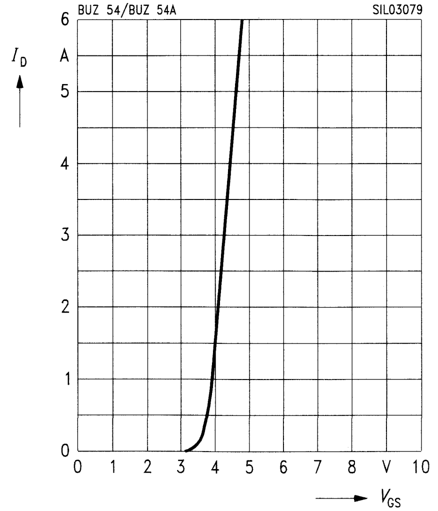
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: $t_p = 80$ µs



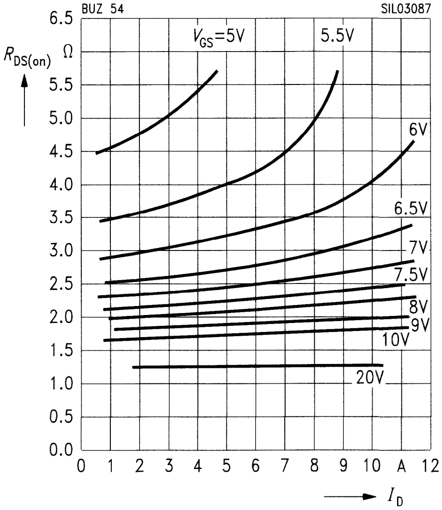
Typ. transfer characteristics

$I_D = f(V_{GS})$
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



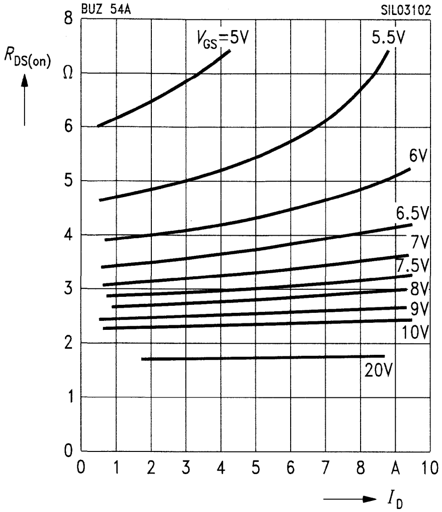
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 54**
parameter: V_{GS}



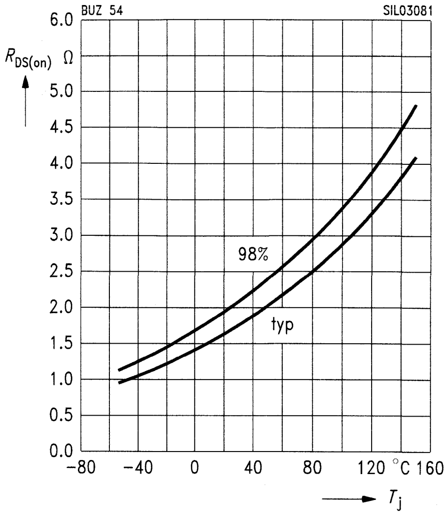
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 54 A**
parameter: V_{GS}



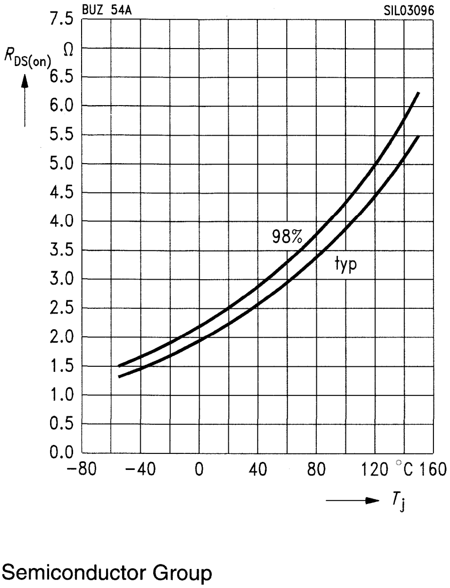
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 54**
parameter: I_D = 3.2 A, V_{GS} = 10 V, (spread)



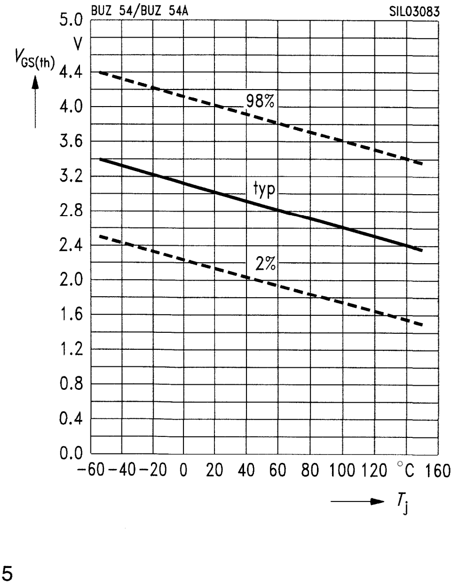
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 54 A**
parameter: I_D = 3.2 A, V_{GS} = 10 V, (spread)



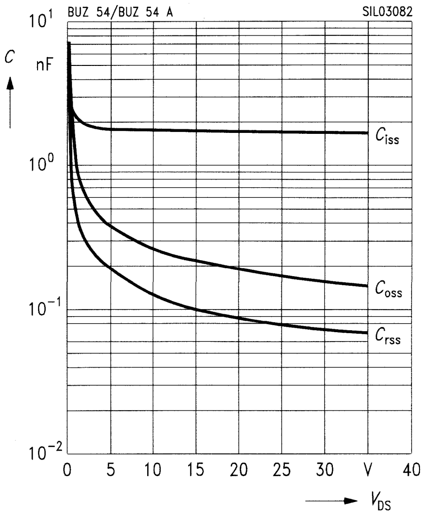
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



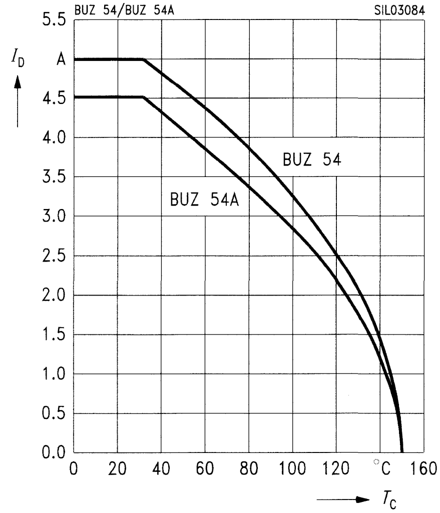
Typ. capacitances

$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



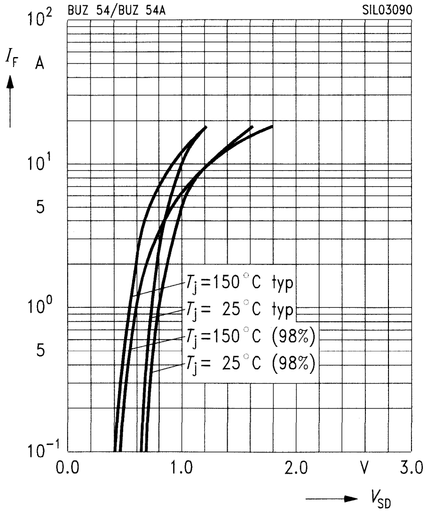
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



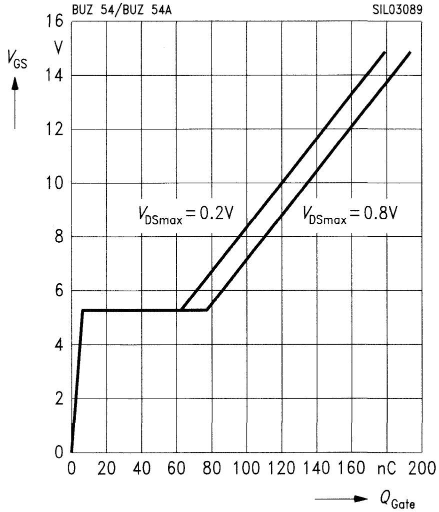
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs, (spread)

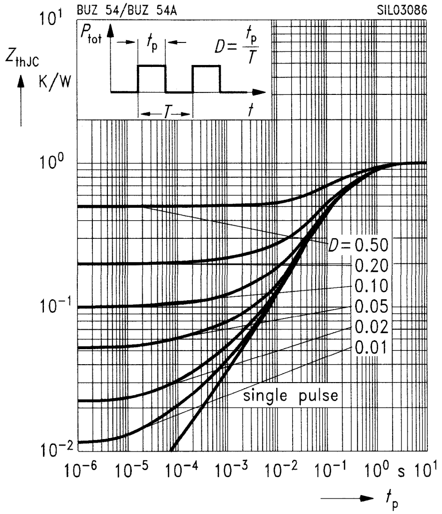


Typ. gate charge

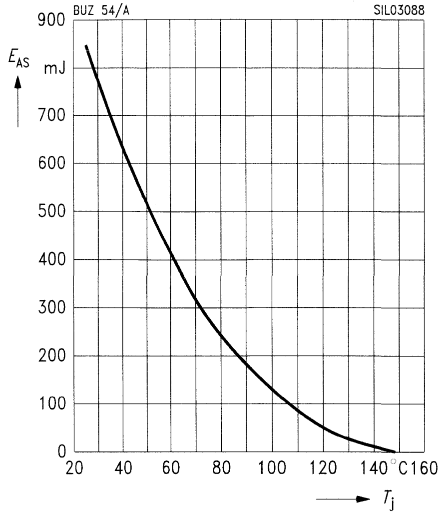
$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 7.5$ A



Transient thermal impedance
$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$

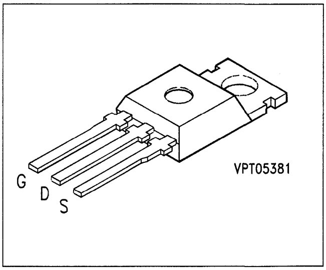


Avalanche energy $E_{\text{AS}} = f(T_j)$
parameter: I_D = 5 A, V_{DD} = 50 V
R_{GS} = 25 Ω, L = 64.6 mH



SIPMOS® Power Transistor **BUZ 60**

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	**Package** [1]	**Ordering Code**
BUZ 60	400 V	5.5 A	1.0 Ω	TO-220 AB	C67078-S1312-A2

Maximum Ratings

Parameter	**Symbol**	**Values**	**Unit**
Continuous drain current, T_C = 36 °C	I_D	**5.5**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**22**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**5.5**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**8**	mJ
Avalanche energy, single pulse I_D = 5.5 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 18.5 mH, T_j = 25 °C	E_{AS}	**320**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at $T_j = 25\ ^\circ C$, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage $V_{GS} = 0$ V, $I_D = 0.25$ mA	$V_{(BR)DSS}$	400	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, $I_D = 1$ mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current $V_{DS} = 400$ V, $V_{GS} = 0$ V	I_{DSS}				µA
$T_j = 25\ ^\circ C$		–	0.1	1.0	
$T_j = 125\ ^\circ C$		–	10	100	
Gate-source leakage current $V_{GS} = 20$ V, $V_{DS} = 0$ V	I_{GSS}	–	10	100	nA
Drain-source on-resistance $V_{GS} = 10$ V, $I_D = 3.5$ A	$R_{DS(on)}$	–	0.65	1.0	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, $I_D = 3.5$ A	g_{fs}	2.5	4.3	–	S
Input capacitance $V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	C_{iss}	–	780	1050	pF
Output capacitance $V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	C_{oss}	–	120	180	
Reverse transfer capacitance $V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	C_{rss}	–	50	80	
Turn-on time t_{on}, ($t_{on} = t_{d(on)} + t_r$) $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_D = 2.7$ A, $R_{GS} = 50\ \Omega$	$t_{d(on)}$	–	20	30	ns
	t_r	–	50	75	
Turn-off time t_{off}, ($t_{off} = t_{d(off)} + t_f$) $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_D = 2.7$ A, $R_{GS} = 50\ \Omega$	$t_{d(off)}$	–	130	150	
	t_f	–	70	90	

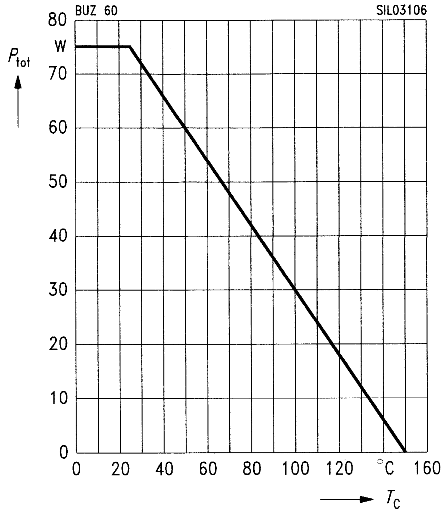
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	5.5	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	22	
Diode forward on-voltage I_S = 11 A, V_{GS} = 0 V	V_{SD}	–	1.0	1.2	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	1.0	–	µs
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	5	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

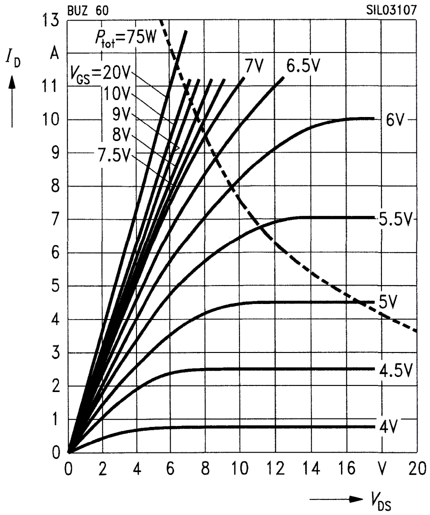
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

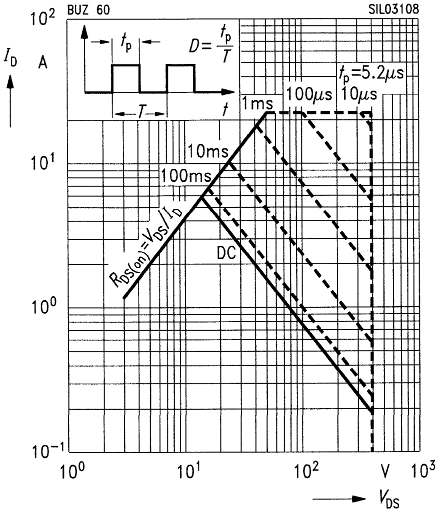
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

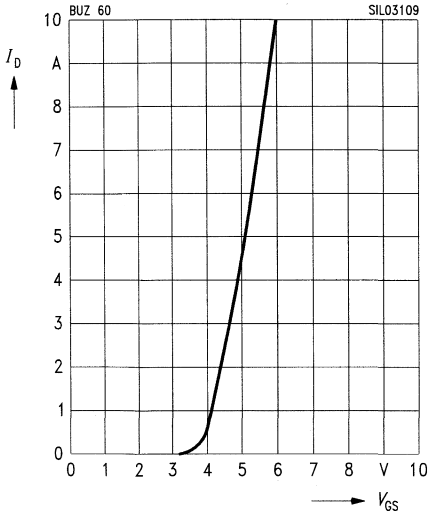
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

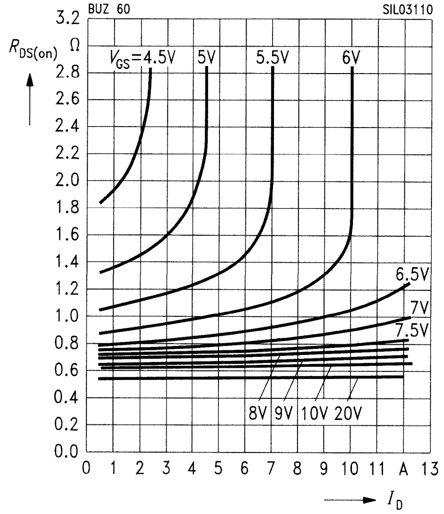
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

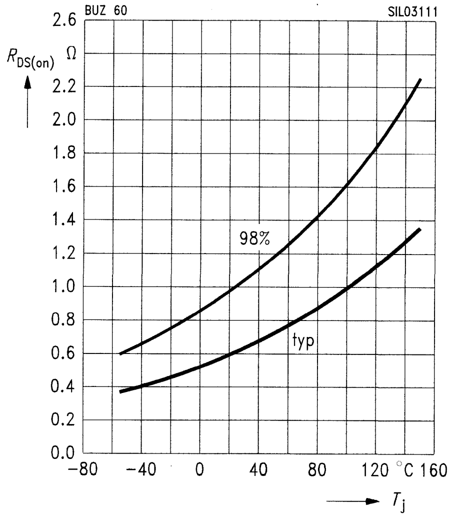
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

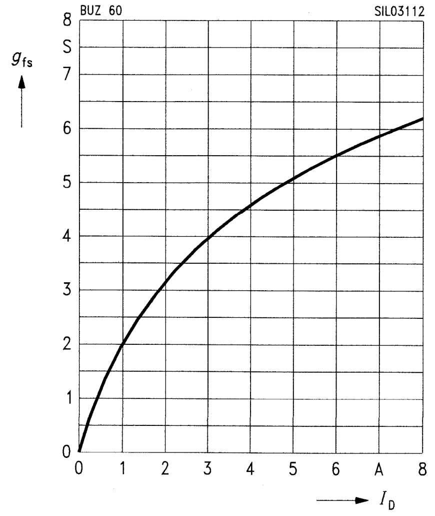
parameter: I_D = 3.5 A, V_{GS} = 10 V, (spread)



Typ. forward transconductance

$g_{fs} = f\,(I_D)$

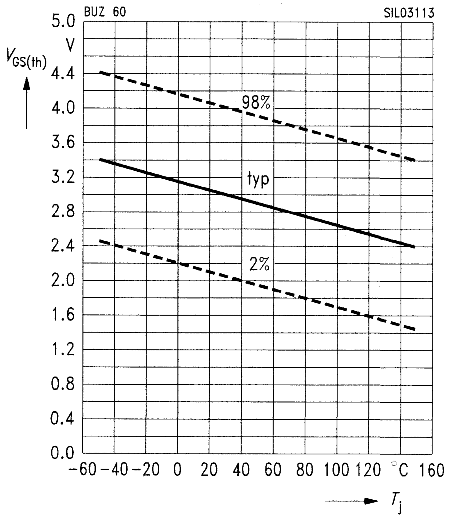
parameter: t_p = 80 µs



Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

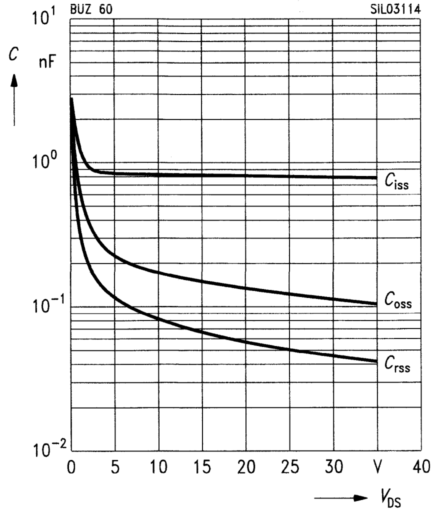
parameter: V_{GS} = V_{DS} , I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

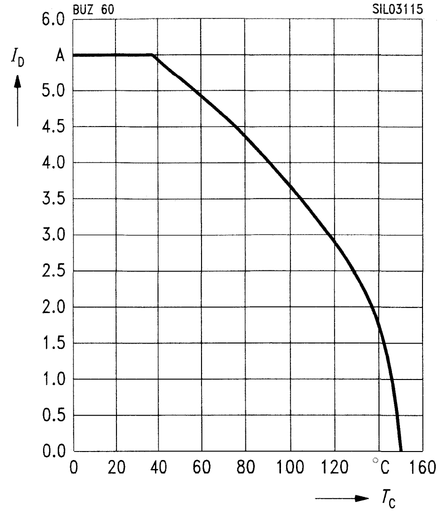
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

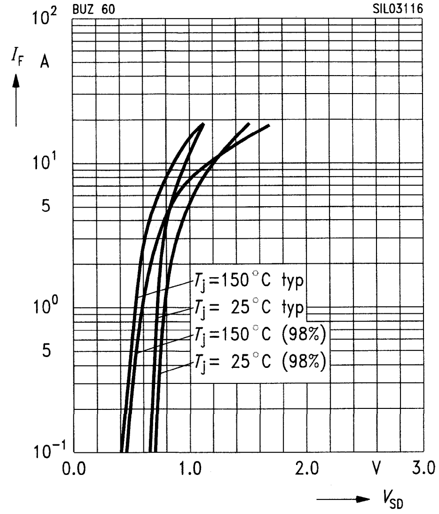
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

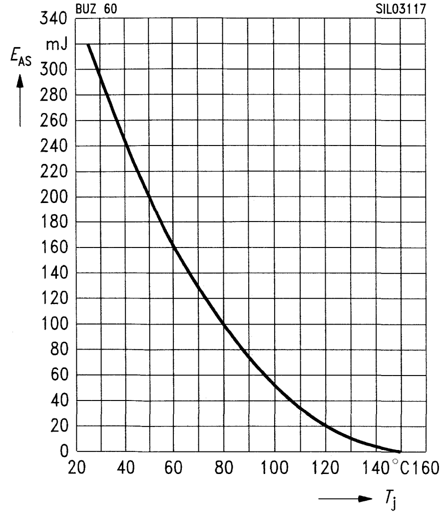
parameter: T_j, $t_p = 80$ µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

parameter: $I_D = 5.5$ A, $V_{DD} = 50$ V

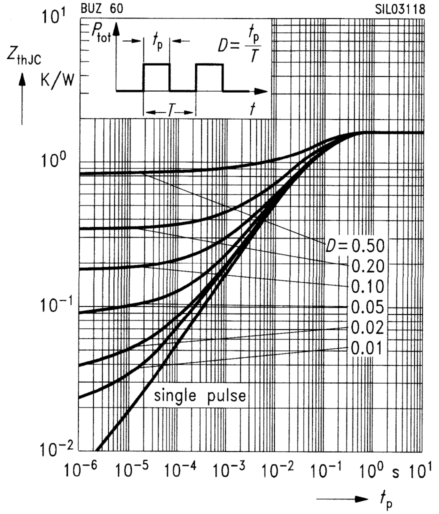
$R_{GS} = 25\ \Omega$, $L = 18.5$ mH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

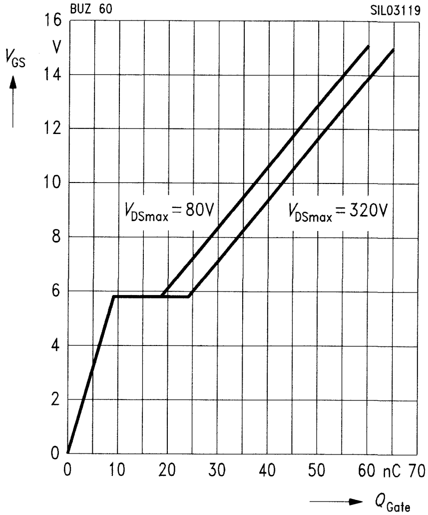
parameter: $D = t_p / T$



Typ. gate charge

$V_{\text{GS}} = f(Q_{\text{Gate}})$

parameter: $I_{\text{D puls}} = 8.3$ A

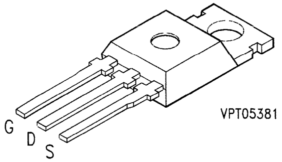


SIEMENS

SIPMOS® Power Transistors

BUZ 61
BUZ 61 A

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package[1]	Ordering Code
BUZ 61	400 V	12.5 A	0.4 Ω	TO-220 AB	C67078-S1341-A2
BUZ 61 A	400 V	11 A	0.5 Ω	TO-220 AB	C67078-S1341-A3

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		61	61 A	
Continuous drain current, $T_C = 27$ °C	I_D	**12.5**	**11**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**50**	**44**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**12.5**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**13**		mJ
Avalanche energy, single pulse $I_D = 12.5$ A, $V_{DD} = 50$ V, $R_{GS} = 25$ Ω $L = 6.38$ mH, $T_j = 25$ °C	E_{AS}	**570**		
Gate-source voltage	V_{GS}	**± 20**		V
Power dissipation, $T_C = 25$ °C	P_{tot}	**150**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 0.83**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\ DSS}$	400	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\ (th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 400 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS\ (on)}$				Ω
V_{GS} = 10 V, I_D = 8 A BUZ 61		–	0.35	0.4	
BUZ 61 A		–	0.4	0.5	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$ I_D = 8.0 A	g_{fs}	5.0	11.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1500	2250	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	210	315	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	75	110	
Turn-on time t_{on} , ($t_{on} = t_{d\ (on)} + t_r$) V_{DD}= 30 V, V_{GS} = 10 V, I_D =3.0 A, R_{GS} = 50 Ω	$t_{d\ (on)}$	–	20	30	ns
	t_r	–	65	100	
Turn-off time t_{off} , ($t_{off} = t_{d\ (off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\ (off)}$	–	260	340	
	t_f	–	75	100	

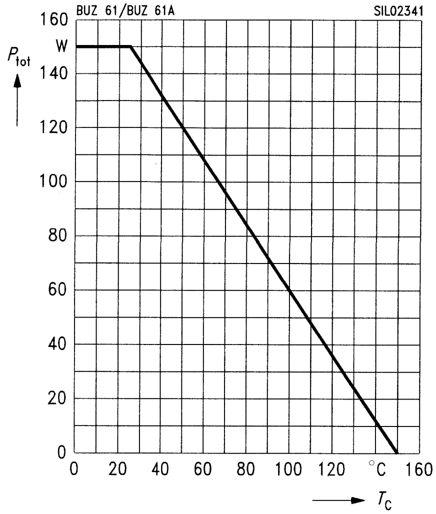
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C BUZ 61 BUZ 61 A	I_S	– –	– –	12.5 11.0	A
Pulsed reverse drain current T_C = 25 °C BUZ 61 BUZ 61 A	I_{SM}	– –	– –	50 44	
Diode forward on-voltage I_S = 25 A, V_{GS} = 0 V	V_{SD}	–	1.1	1.4	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	280	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	3	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

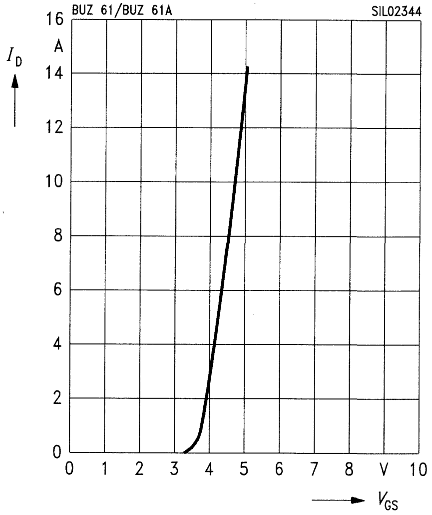
$P_{tot} = f(T_C)$



Typ. transfer characteristics

$I_D = f(V_{GS})$

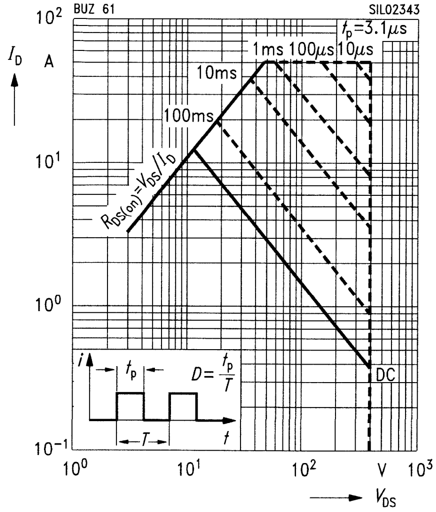
parameter: t_p = 80 µs, V_{DS} = 25 V



Safe operating area

$I_D = f(V_{DS})$ **BUZ 61**

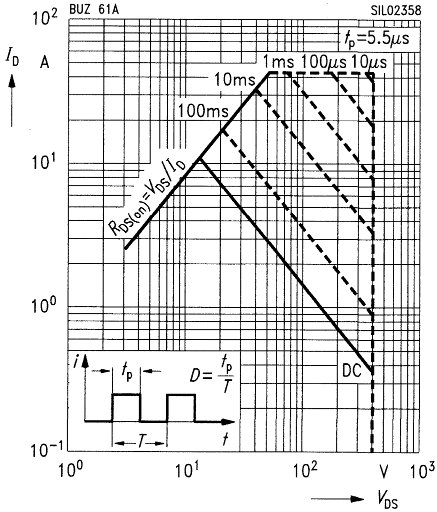
parameter: D = 0.01, T_C = 25 °C



Safe operating area

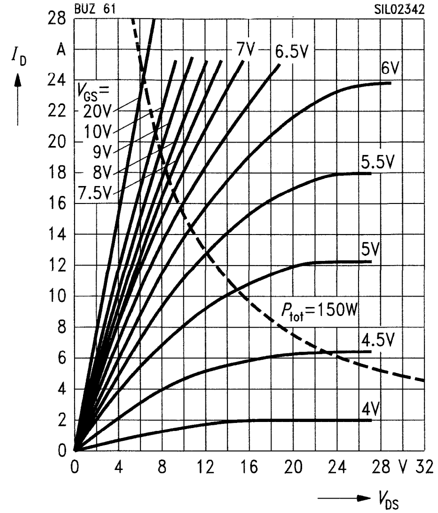
$I_D = f(V_{DS})$ **BUZ 61 A**

parameter: D = 0.01, T_C = 25 °C



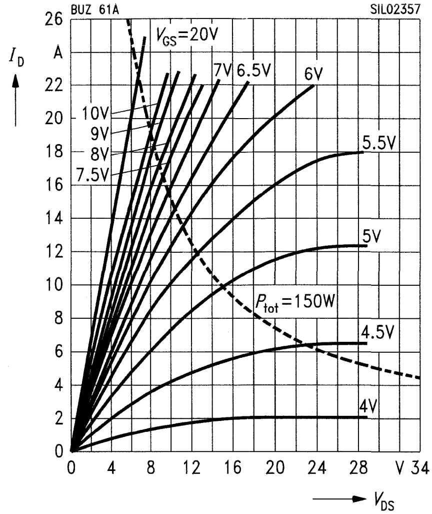
Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 61**
parameter: t_p = 80 µs



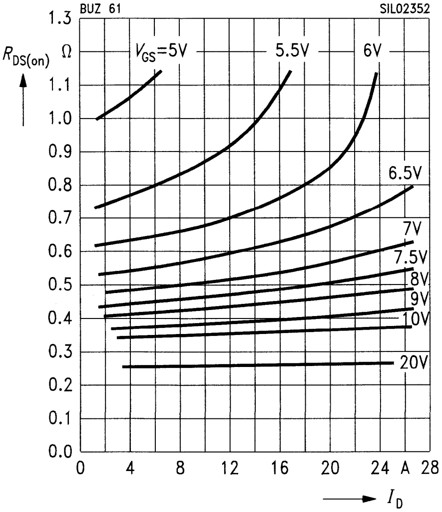
Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 61 A**
parameter: t_p = 80 µs



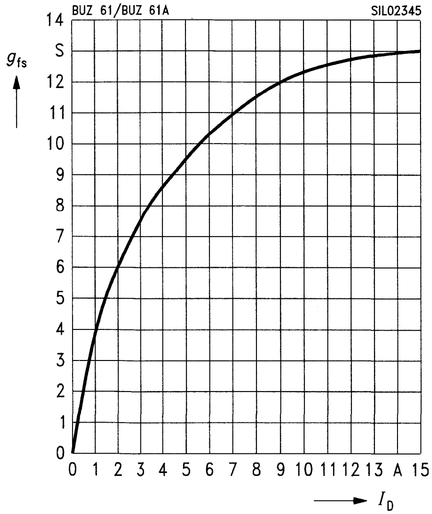
Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$ **BUZ 61**
parameter: V_{GS}

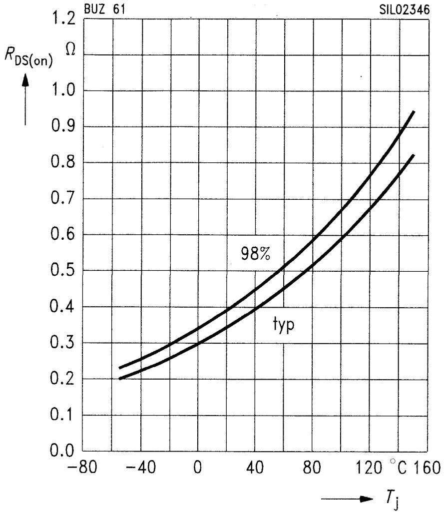


Typ. forward transconductance

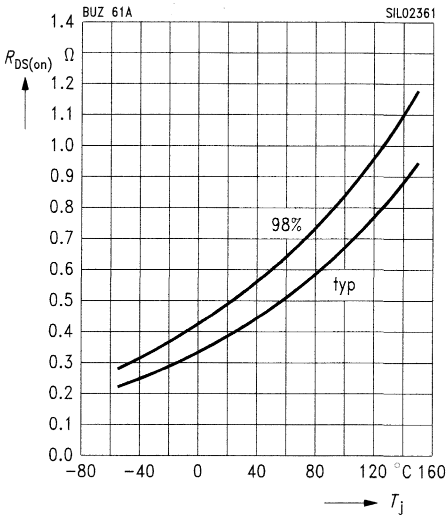
$g_{fs} = f(I_D)$
parameter: t_p = 80 µs



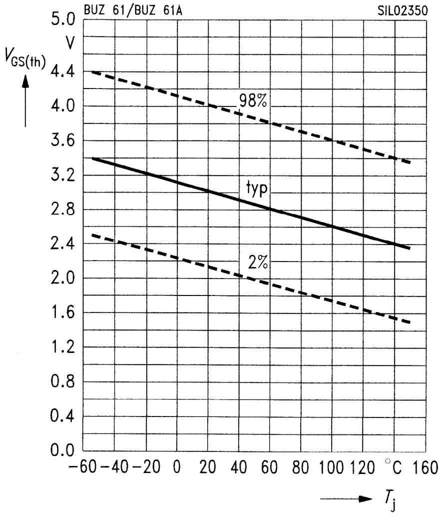
Drain-source on-resistance
$R_{DS\ (on)} = f\ (T_j)$ **BUZ 61**
parameter: I_D = 8 A, V_{GS} = 10 V, (spread)



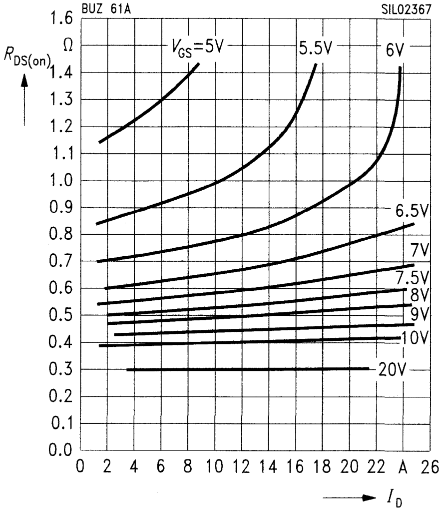
Drain-source on-resistance
$R_{DS\ (on)} = f\ (T_j)$ **BUZ 61 A**
parameter: I_D = 8 A, V_{GS} = 10 V, (spread)



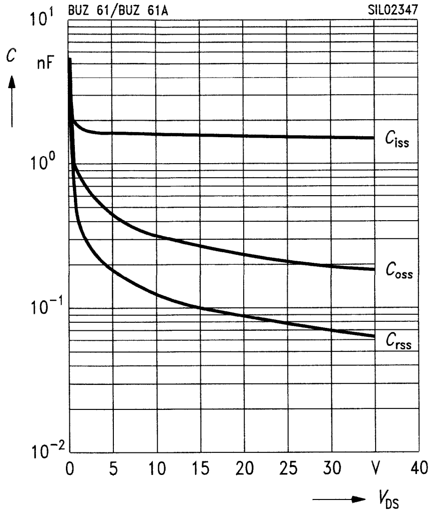
Gate threshold voltage
$V_{GS\ (th)} = f\ (T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



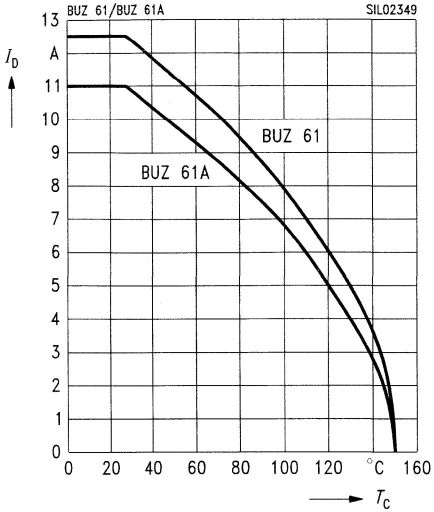
Typ. drain-source on-resistance
$R_{DS\ (on)} = f\ (I_D)$ **BUZ 61 A**
parameter: V_{GS}



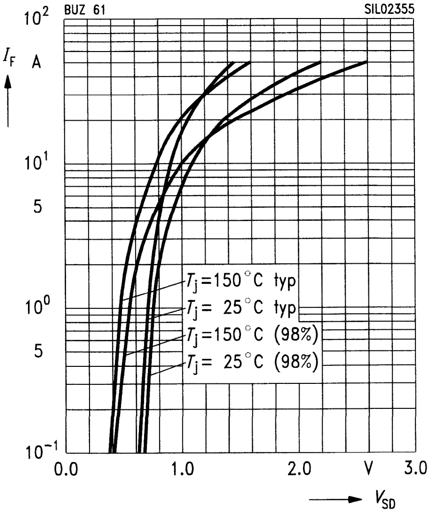
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



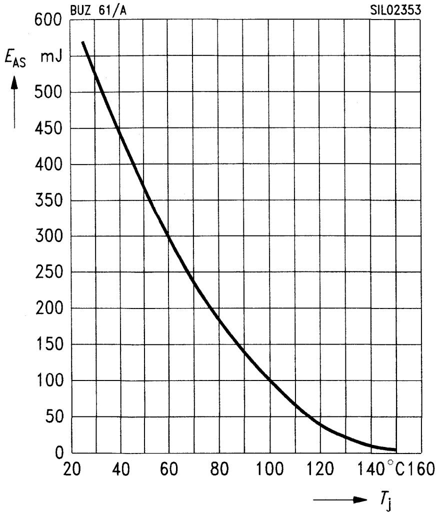
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$ **BUZ 61**
parameter: T_j, $t_p = 80$ µs, (spread)



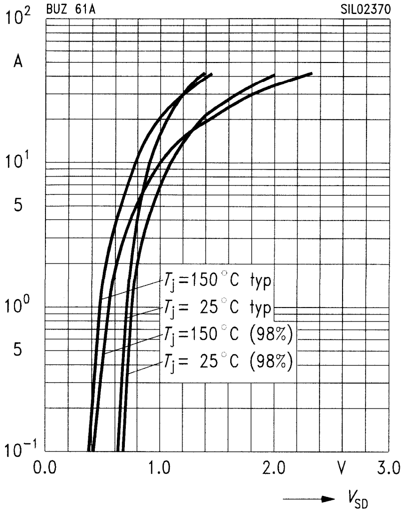
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 12.5$ A, $V_{DD} = 50$ V
$R_{GS} = 25\ \Omega$, $L = 6.38$ mH



Forward characteristics of reverse diode

$I_F = f(V_{SD})$ **BUZ 61 A**

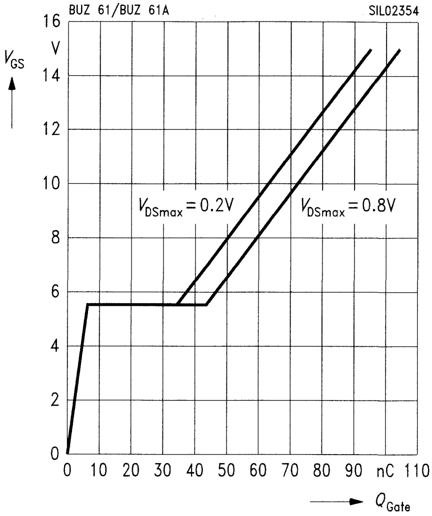
parameter: T_j, t_p = 80 µs, (spread)



Typ. gate charge

$V_{GS} = f(Q_{Gate})$

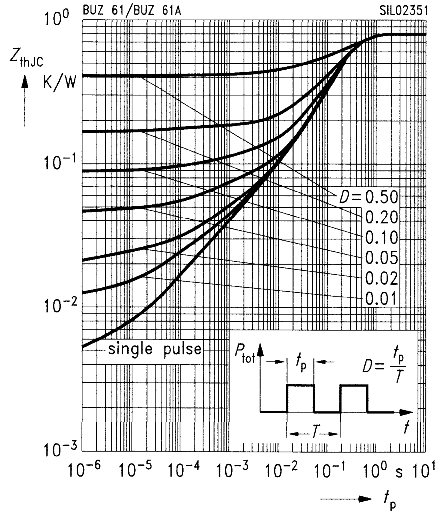
parameter: $I_{D\,puls}$ = 15.0 A



Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

parameter: $D = t_p / T$

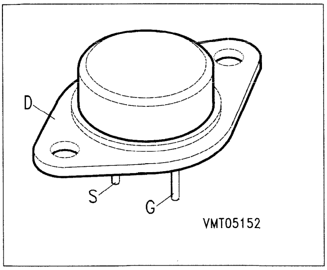


SIEMENS

SIPMOS® Power Transistor

BUZ 64

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 64	400 V	11.5 A	0.4 Ω	TO-204 AA	C67078-S1017-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, $T_C = 31$ °C	I_D	**11.5**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**46**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**11.5**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**13**	mJ
Avalanche energy, single pulse I_D =11.5 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 8.87 mH, T_j = 25 °C	E_{AS}	**670**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, $T_C = 25$ °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**C**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	400	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 400 V, V_{GS} = 0 V T_j = 25 °C T_j = 125 °C	I_{DSS}	 – –	 0.1 10	 1.0 100	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 7.5 A	$R_{DS(on)}$	–	0.35	0.40	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 7.5 A	g_{fs}	5.0	9.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1900	2500	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	260	400	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	110	170	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	30	45	ns
	t_r	–	90	135	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	350	465	
	t_f	–	100	135	

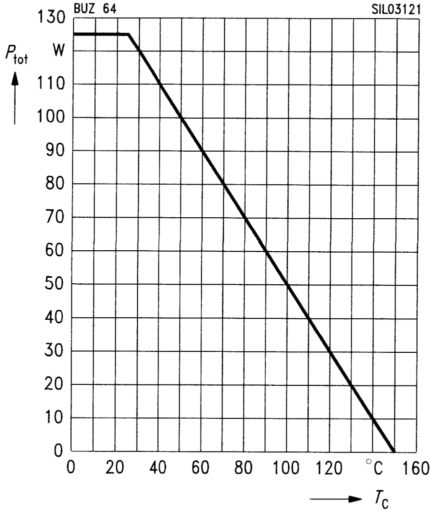
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	11.5	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	46	
Diode forward on-voltage I_S = 23 A, V_{GS} = 0 V	V_{SD}	–	1.1	1.4	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	180	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	1.2	–	µC

Characteristics at T_j = 25 ˚C, unless otherwise specified.

Total power dissipation

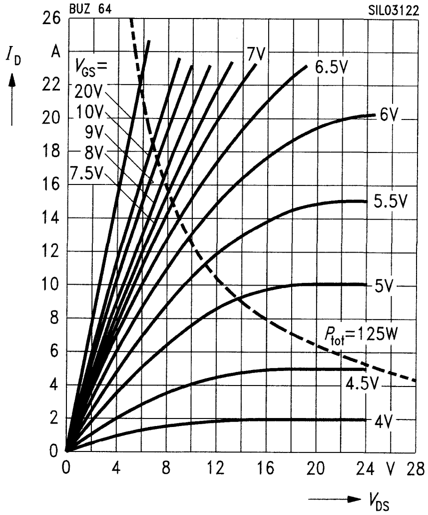
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

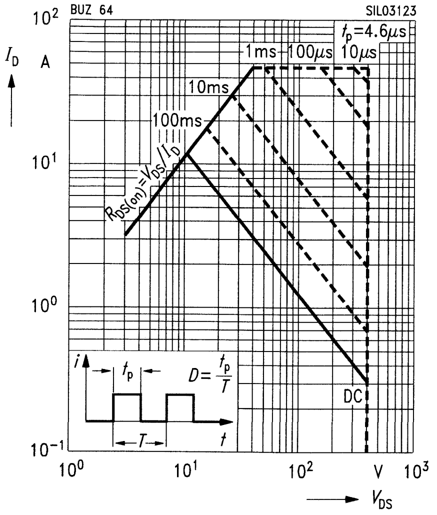
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

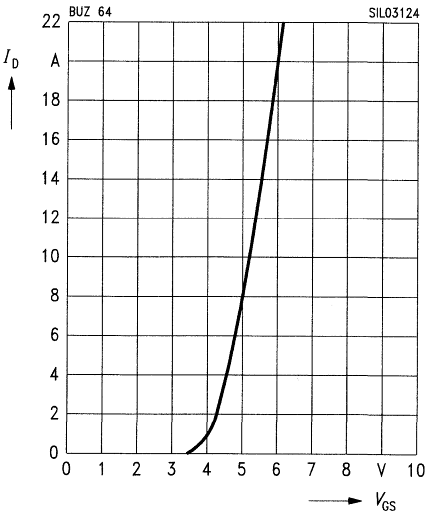
parameter: D = 0.01, T_C = 25 ˚C



Typ. transfer characteristics

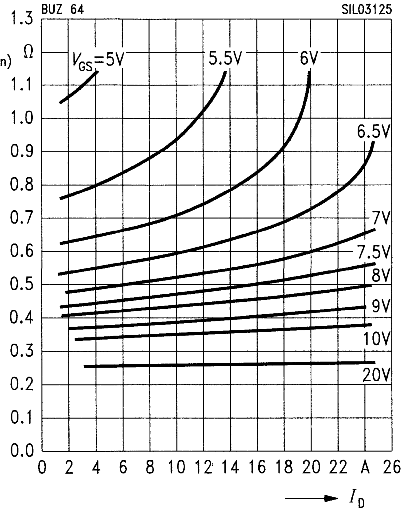
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



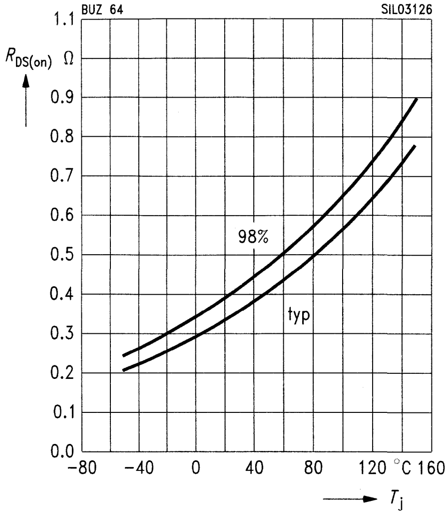
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



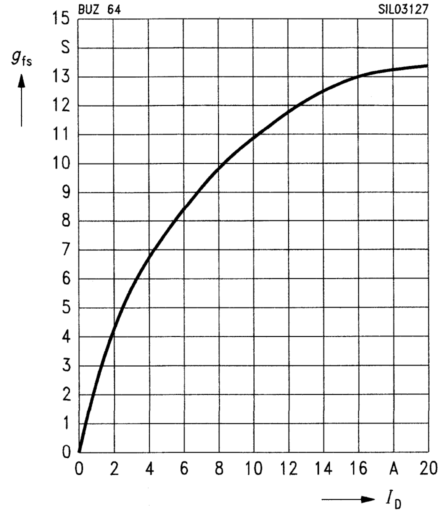
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 7.5 A, V_{GS} = 10 V, (spread)



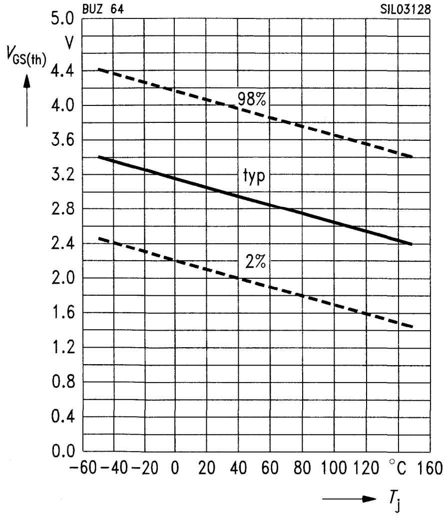
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs

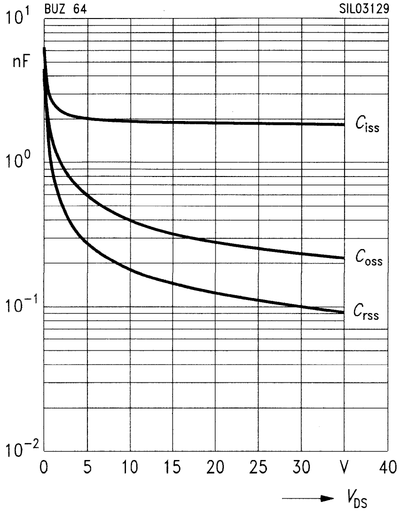


Gate threshold voltage

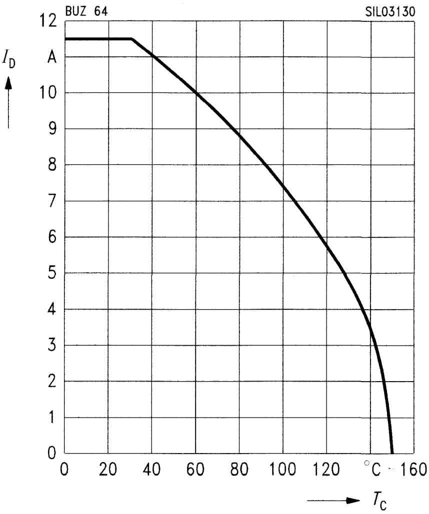
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



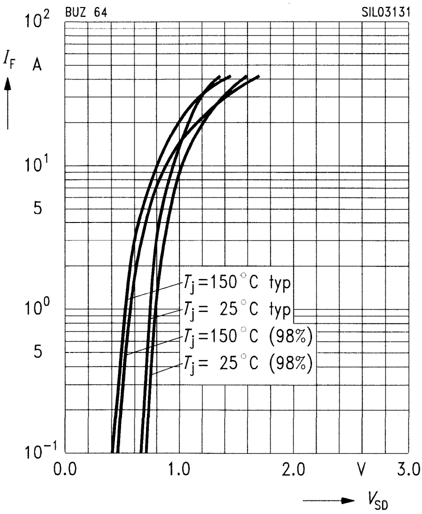
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



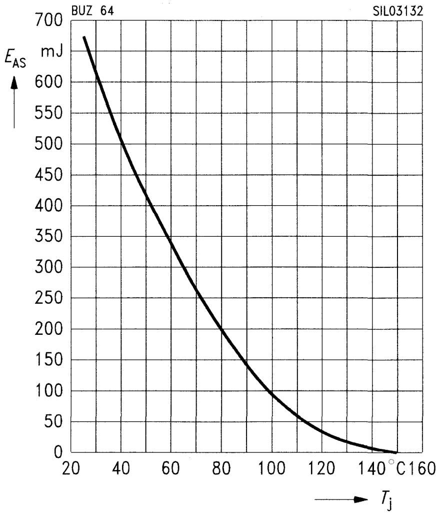
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs, (spread)



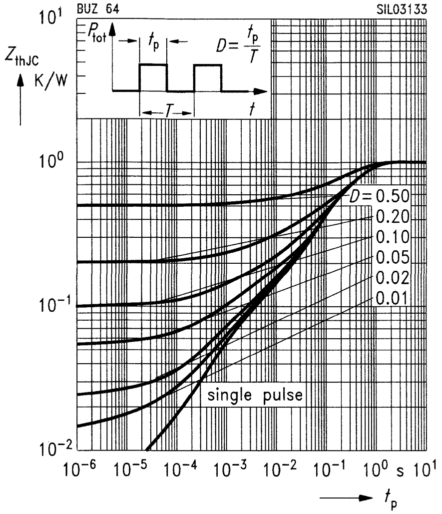
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 11.5$ A, $V_{DD} = 50$ V
$R_{GS} = 25\ \Omega$, $L = 8.87$ mH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

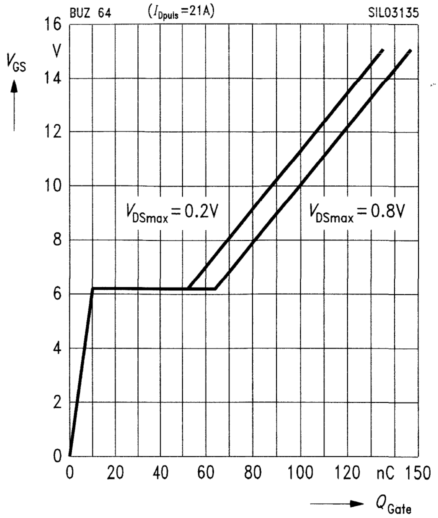
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{\text{Gate}})$

parameter: $I_{\text{D puls}} = 21$ A

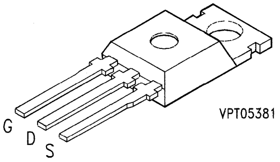


SIEMENS

SIPMOS® Power Transistor

BUZ 70

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 70	60 V	12 A	0.15 Ω	TO-220 AB	C67078-S1334-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, $T_C = 33$ °C	I_D	**12**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**48**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**12**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**1**	mJ
Avalanche energy, single pulse $I_D = 12$ A, $V_{DD} = 30$ V, $R_{GS} = 25$ Ω $L = 48.6$ µH, $T_j = 25$ °C	E_{AS}	**6**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, $T_C = 25$ °C	P_{tot}	**40**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	60	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 60 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 7.5 A	$R_{DS\,(on)}$	–	0.12	0.15	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 7.5 A	g_{fs}	2.0	5.7	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	360	480	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	160	250	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	50	90	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	15	25	ns
	t_r	–	30	45	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	40	55	
	t_f	–	55	75	

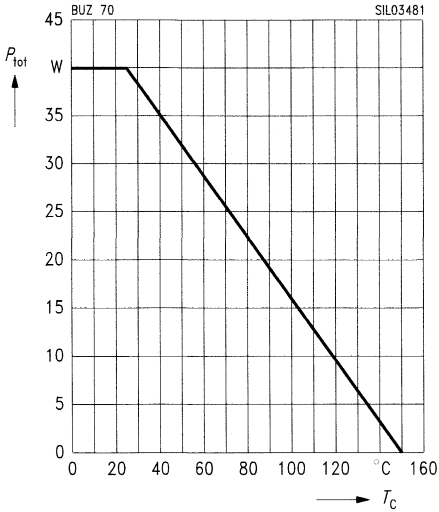
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	12	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	48	
Diode forward on-voltage I_S = 25 A, V_{GS} = 0 V	V_{SD}	–	1.5	1.8	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	60	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.10	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

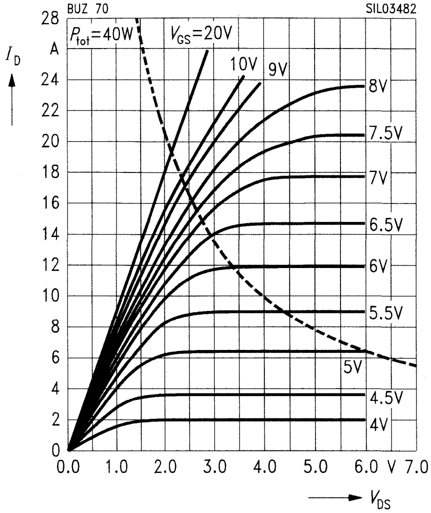
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

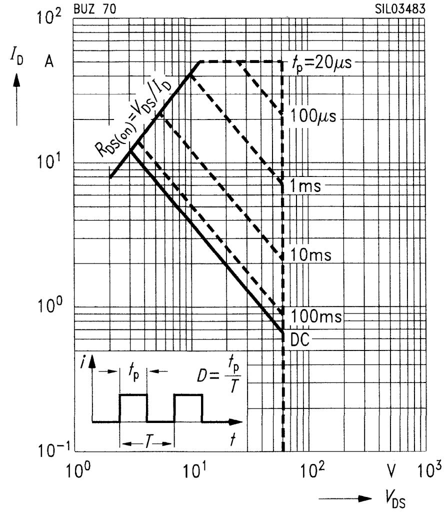
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

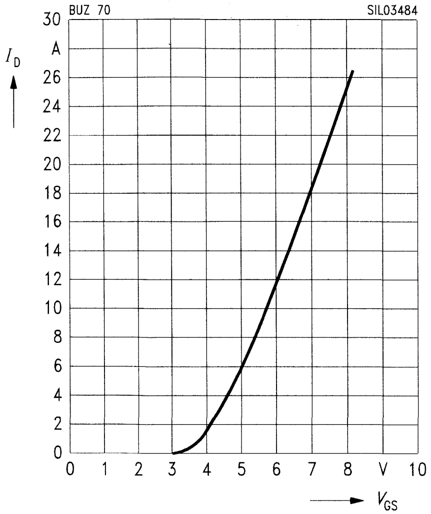
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

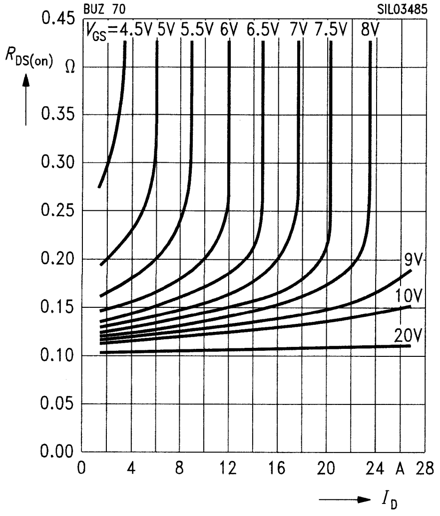
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



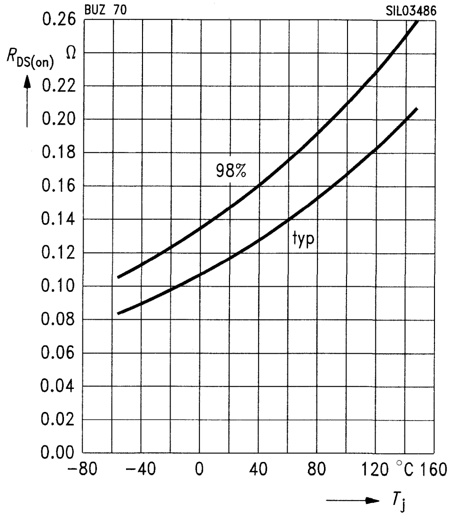
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



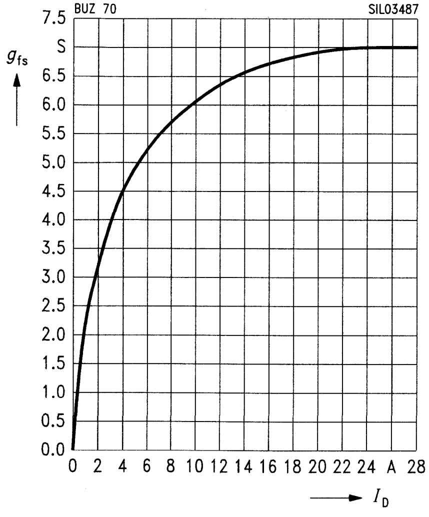
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 7.5 A, V_{GS} = 10 V, (spread)



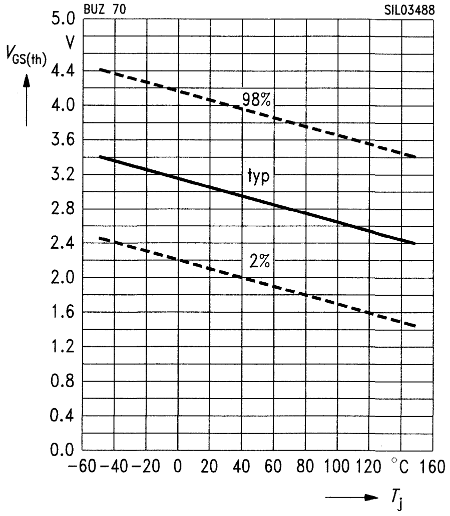
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

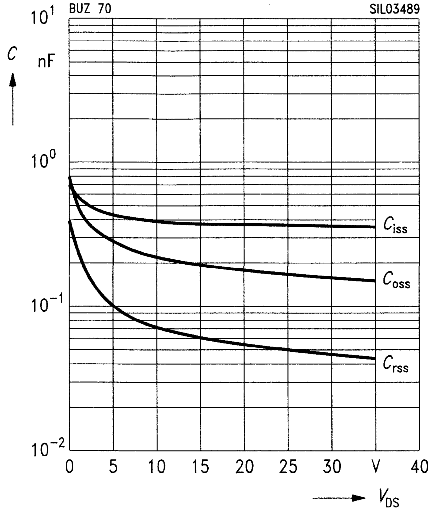
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

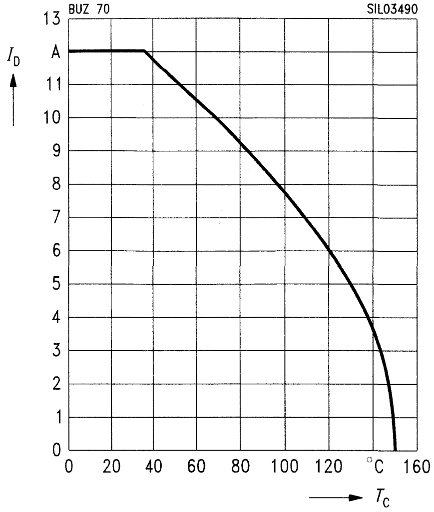
parameter: V_{GS} = 0 V, f = 1 MHz



Drain current

$I_D = f(T_C)$

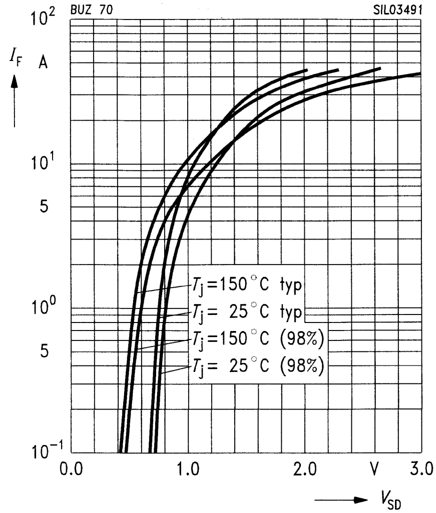
parameter: $V_{GS} \geq$ 10 V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

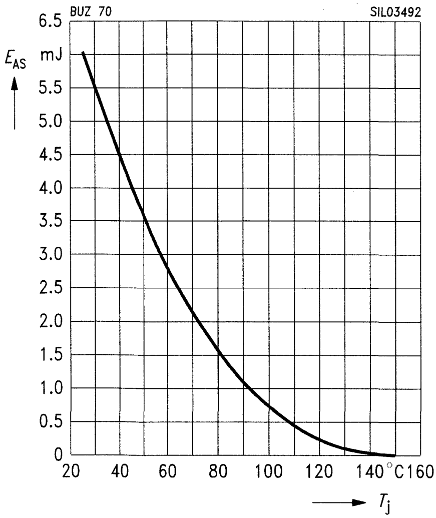
parameter: T_j , t_p = 80 µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

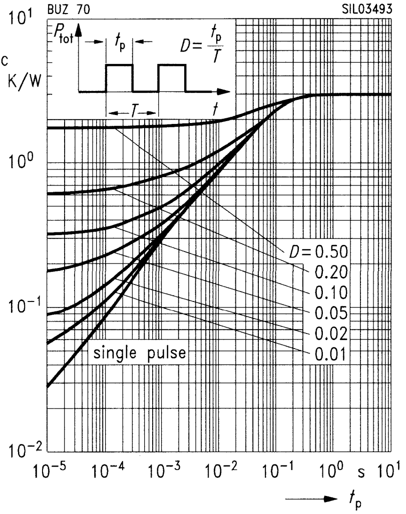
parameter: I_D = 12 A, V_{DD} = 25 V

R_{GS} = 25 Ω, L = 48.6 µH



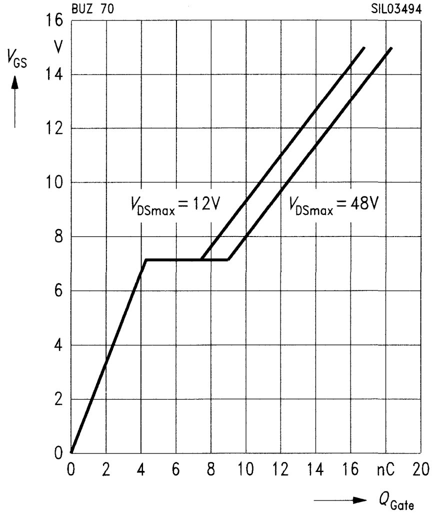
Transient thermal impedance

$Z_{\text{th JC}} = f\,(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

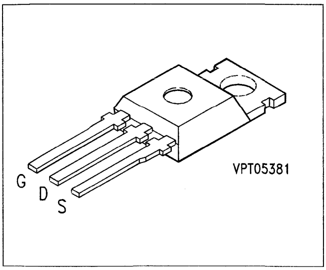
$V_{GS} = f\,(Q_{\text{Gate}})$
parameter: $I_{\text{D puls}} = 18$ A



SIEMENS

SIPMOS® Power Transistor **BUZ 70 L**

- N channel
- Enhancement mode
- Avalanche-rated
- Logic Level



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 70 L	60 V	12 A	0.15 Ω	TO-220 AB	C67078-S1325-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 33 °C	I_D	**12**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**48**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**12**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**1**	mJ
Avalanche energy, single pulse I_D = 12 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 48.6 µH, T_j = 25 °C	E_{AS}	**6**	
Gate-source voltage	V_{GS}	**± 10**	V
Gate-source peak voltage aperiodic	V_{gs}	**± 20**	
Power dissipation, T_C = 25 °C	P_{tot}	**40**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	60	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	1.5	2.0	2.5	
Zero gate voltage drain current V_{DS} = 60 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 5 V, I_D = 6.0 A	$R_{DS(on)}$	–	0.12	0.15	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 6.0 A	g_{fs}	2.0	7.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	420	560	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	160	250	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	60	110	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	15	25	ns
	t_r	–	55	80	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	45	60	
	t_f	–	40	55	

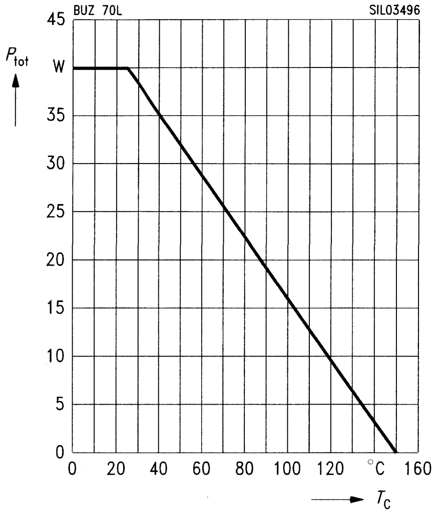
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	**typ.**	**max.**	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	12	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	48	
Diode forward on-voltage I_S = 24 A, V_{GS} = 0 V	V_{SD}	–	1.5	1.8	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	60	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.10	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

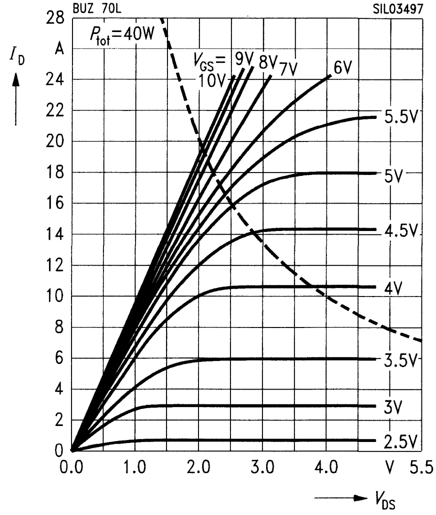
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

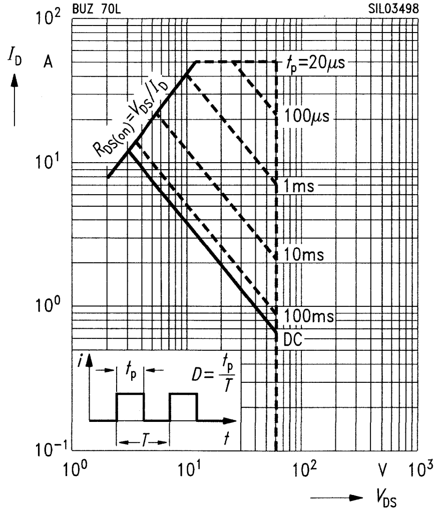
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

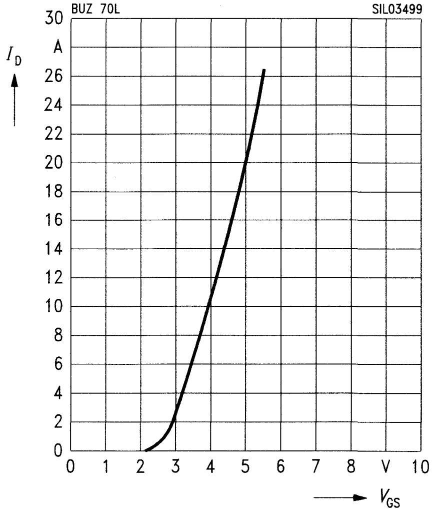
parameter: D = 0.01, T_C = 25 °C



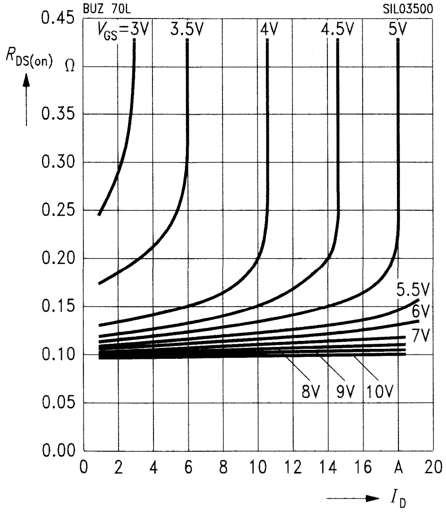
Typ. transfer characteristics

$I_D = f(V_{GS})$

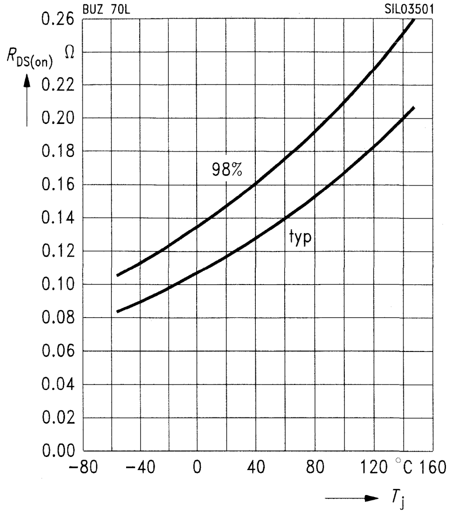
parameter: t_p = 80 µs, V_{DS} = 25 V



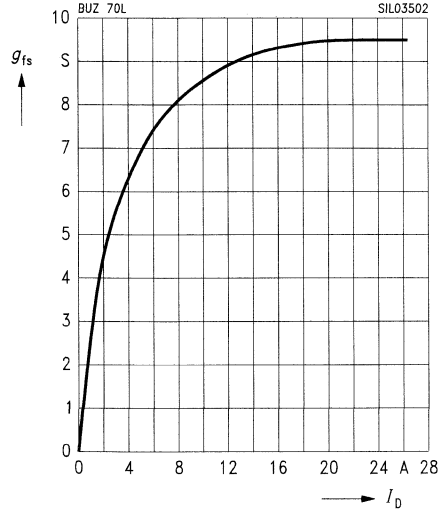
Typ. drain-source on-resistance
$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



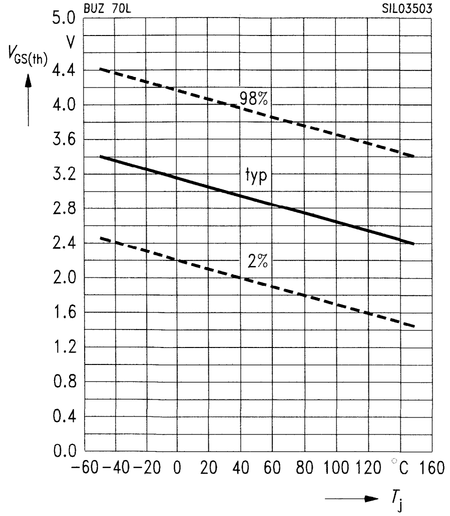
Drain-source on-resistance
$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 6.0 A, V_{GS} = 5 V, (spread)



Typ. forward transconductance
$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



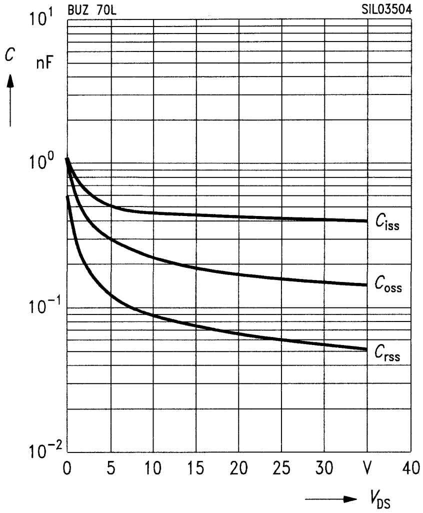
Gate threshold voltage
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

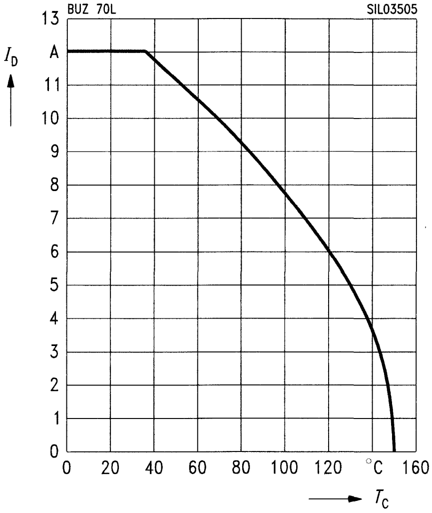
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

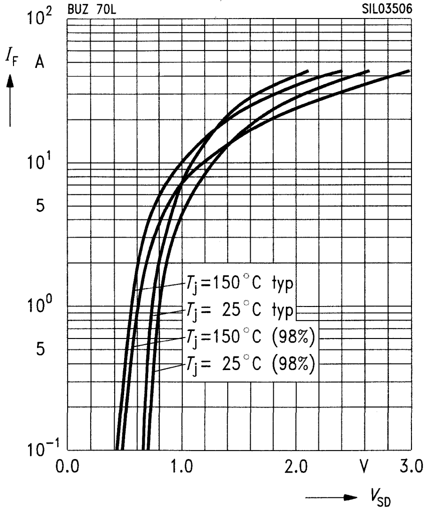
parameter: $V_{GS} \geq 5$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

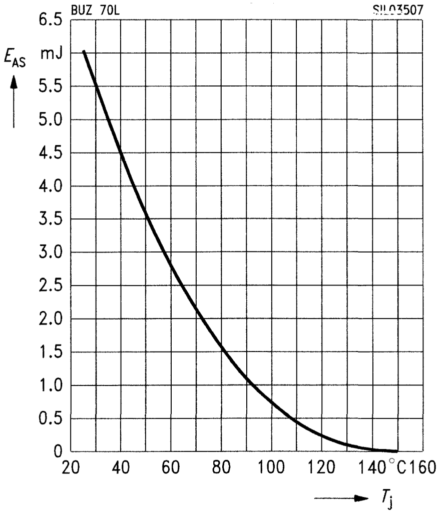
parameter: T_j , $t_p = 80$ µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

parameter: $I_D = 12$ A, $V_{DD} = 25$ V

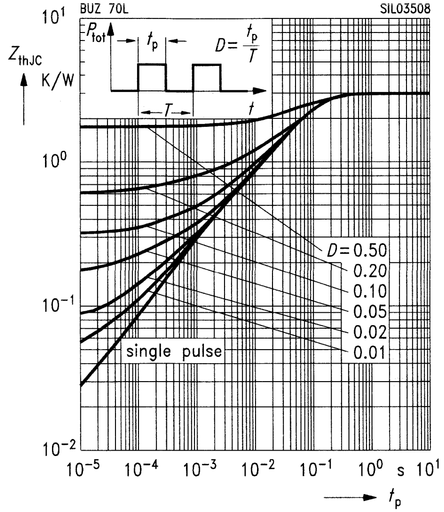
$R_{GS} = 25\ \Omega$, $L = 48.6$ µH



Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

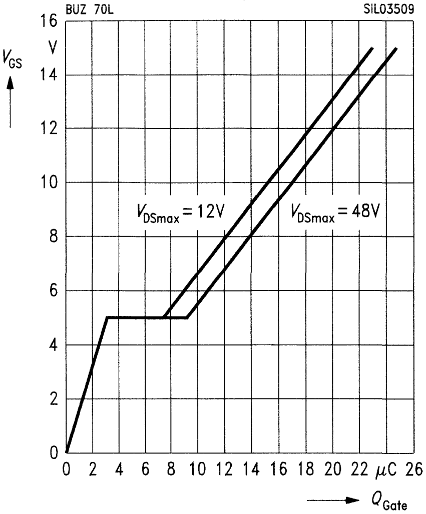
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{Gate})$

parameter: $I_{D\,puls}$ = 18 A

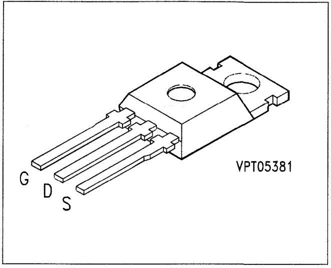


SIEMENS

SIPMOS® Power Transistors

BUZ 71
BUZ 71 A, BUZ 71 S2

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	T_C	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 71	50 V	14 A	28 °C	0.10 Ω	TO-220 AB	C67078-S1316-A2
BUZ 71 A	50 V	13 A	25 °C	0.12 Ω	TO-220 AB	C67078-S1316-A3
BUZ 71 S2	60 V	14 A	28 °C	0.10 Ω	TO-220 AB	C67078-S1316-A9

Maximum Ratings

Parameter	Symbol	BUZ			Unit
		71	71 A	71 S2	
Continuous drain current	I_D	**14**	**13**	**14**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**56**	**52**	**56**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**14**			
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**1**			mJ
Avalanche energy, single pulse V_{DD} = 25 V, R_{GS} = 25 Ω, T_j = 25 °C I_D = 14 A, L = 30.6 µH	E_{AS}	**6**			
Gate-source voltage	V_{GS}	**± 20**			V
Power dissipation, T_C = 25 °C	P_{tot}	**40**			W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**			°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	–

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	**typ.**	**max.**	
Static characteristics					
Drain-source breakdown voltage	$V_{(BR)\,DSS}$				V
V_{GS} = 0 V, I_D = 0.25 mA BUZ 71 / 71 A		50	–	–	
BUZ 71 S2		60	–	–	
Gate threshold voltage V_{GS} = V_{DS} , I_D = 0.25 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current	I_{DSS}				µA
V_{GS} = 0 V V_{DS} = 50 V BUZ 71 / 71 A					
V_{DS} = 60 V BUZ 71 S2					
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS(on)}$				Ω
V_{GS} = 10 V, I_D = 9 A BUZ 71 / 71 S2		–	0.08	0.10	
BUZ 71 A		–	0.10	0.12	

Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 9 A	g_{fs}	4.0	7.7	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	450	600	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	220	350	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	85	150	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\ ,(on)}$	–	20	30	ns
	t_r	–	40	60	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\ (off)}$	–	55	70	
	t_f	–	40	55	

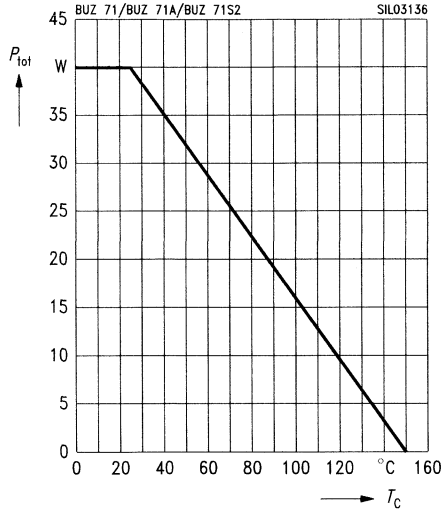
Reverse diode

Parameter	Symbol	min.	typ.	max.	Unit
Continuous reverse drain current	I_S				A
T_C = 25 °C BUZ 71/71 S2		–		14	
BUZ 71 A		–		13	
Pulsed reverse drain current	I_{SM}				A
T_C = 25 °C BUZ 71/71 S2		–		56	
BUZ 71		–		52	
Diode forward on-voltage I_S = 28, V_{GS} = 0 V	V_{SD}	–	1.5	1.8	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	60	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.10	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

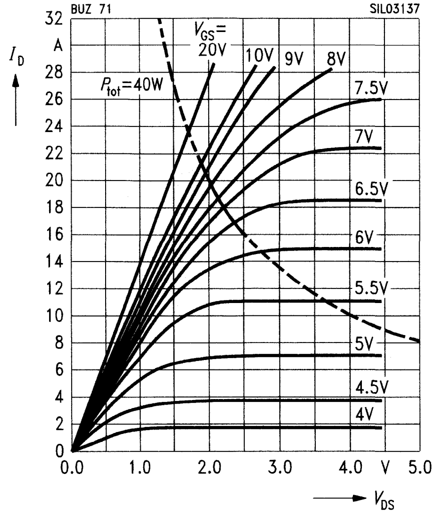
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 71 / BUZ 71 S2**

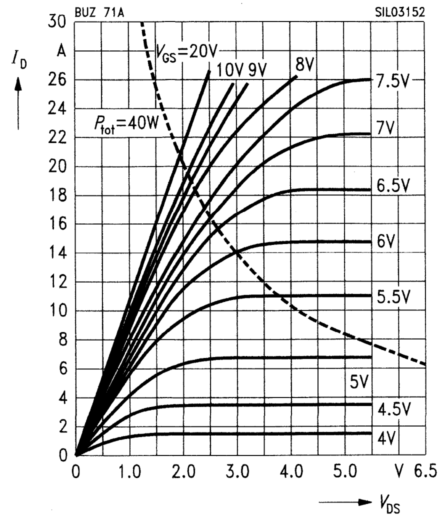
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 71 A**

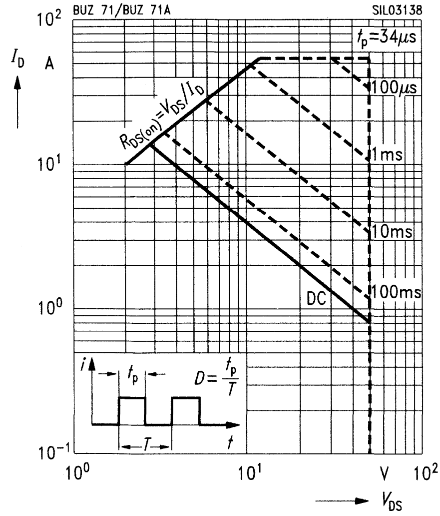
parameter: t_p = 80 µs



Safe operating area

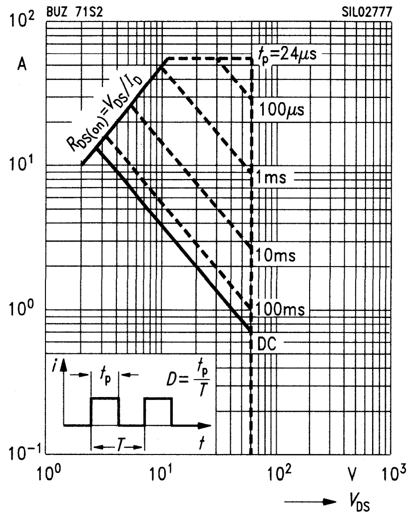
$I_D = f(V_{DS})$ **BUZ 71 / BUZ 71 A**

parameter: D = 0.01, T_C = 25 °C



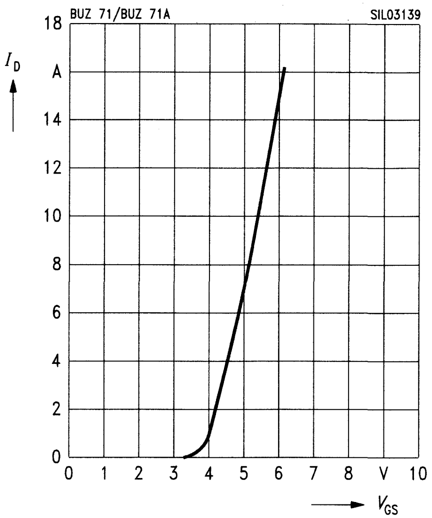
Safe operating area

$I_D = f(V_{DS})$ **BUZ 71 S2**
parameter: $D = 0.01$, $T_C = 25$ °C



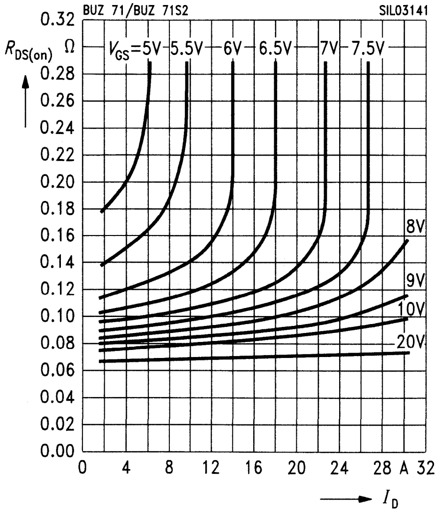
Typ. transfer characteristics

$I_D = f(V_{GS})$
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



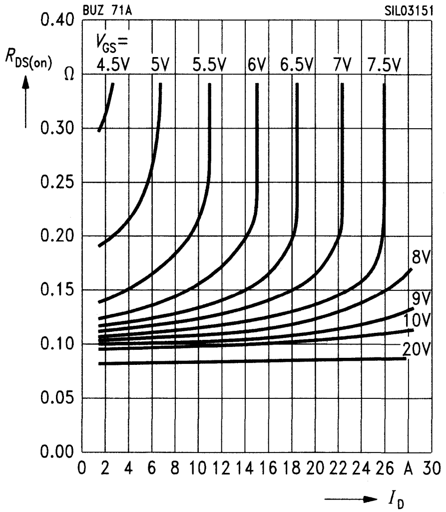
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 71 / BUZ 71 S2**
parameter: V_{GS}



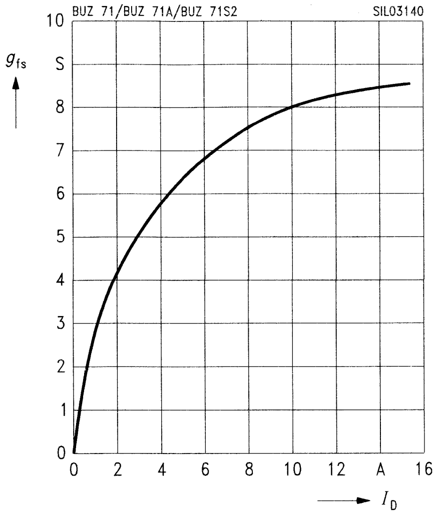
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 71 A**
parameter: V_{GS}



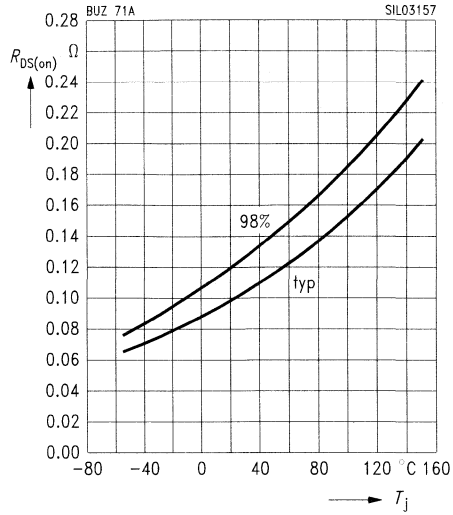
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: t_p = 80 µs



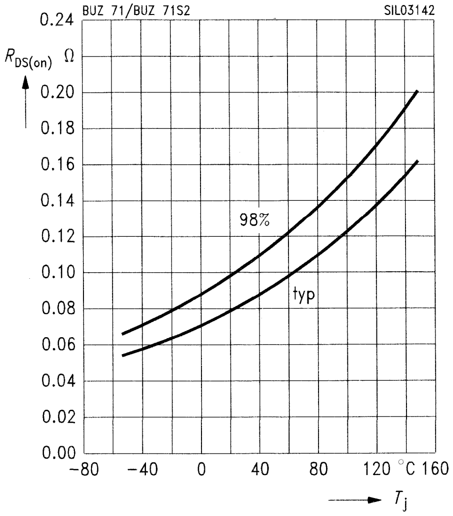
Drain-source on-resistance

$R_{DS\,(on)} = f(T_j)$ **BUZ 71 / BUZ 71 S2**
parameter: I_D = 9 A, V_{GS} = 10 V, (spread)



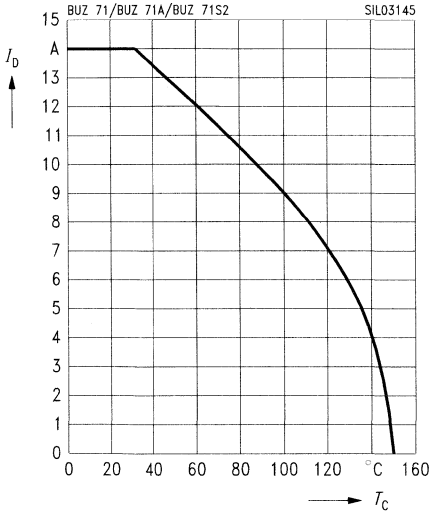
Drain-source on-resistance

$R_{DS\,(on)} = f\ (T_j)$ **BUZ 71 A**
parameter: I_D = 9 A, V_{GS} = 10 V, (spread)



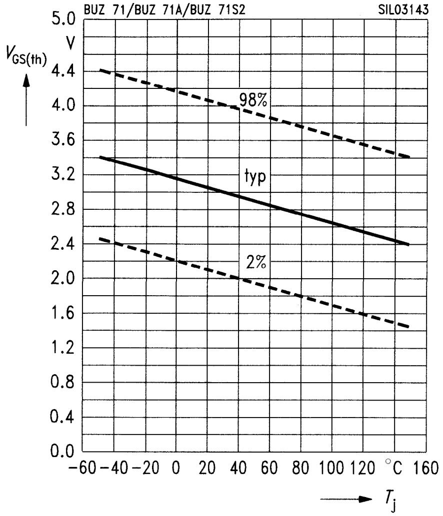
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



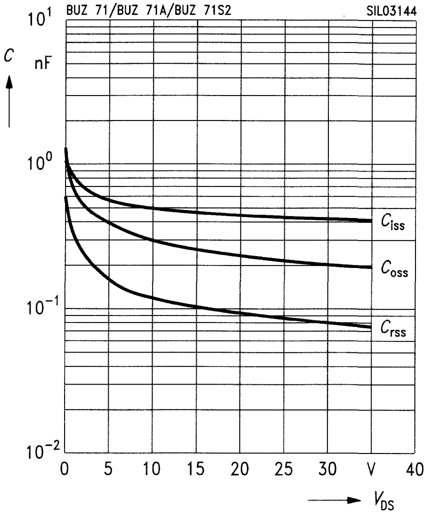
Gate threshold voltage

$V_{GS\,(th)} = f(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



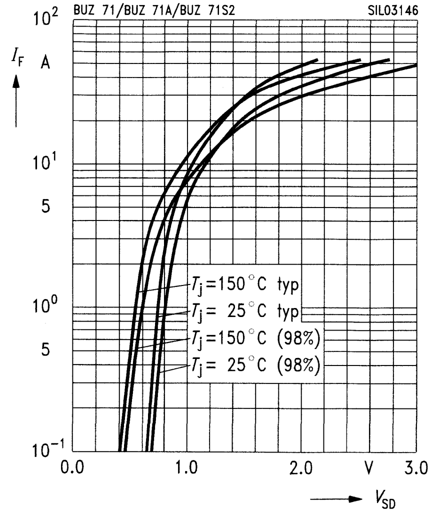
Typ. capacitances

$C = f(V_{DS})$
parameter: V_{GS} = 0 V, f = 1 MHz



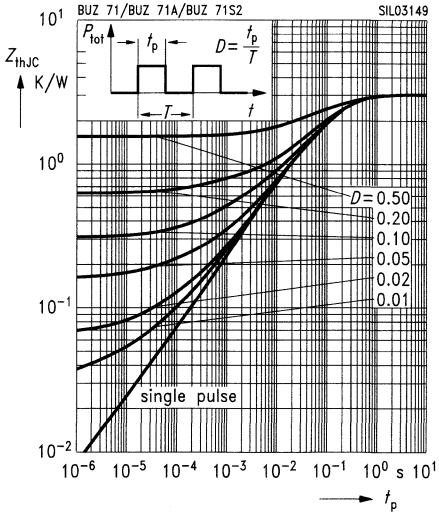
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: T_j, t_p = 80 µs, (spread)

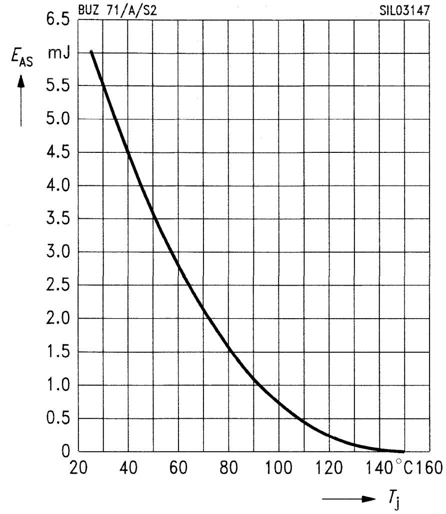


Transient thermal impedance

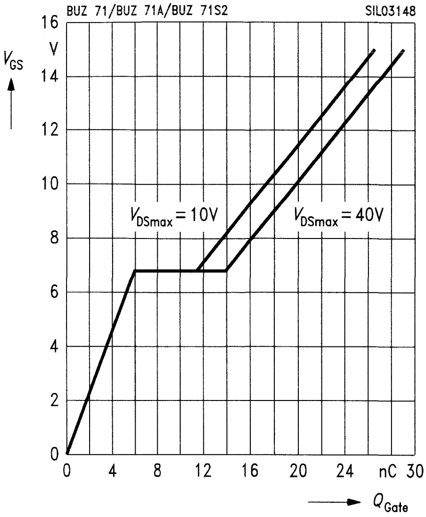
$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



Avalanche energy $E_{AS} = f(T_j)$
parameter: I_D = 14 A, V_{DD} = 25 V
R_{GS} = 25 Ω, L = 30.6 μH



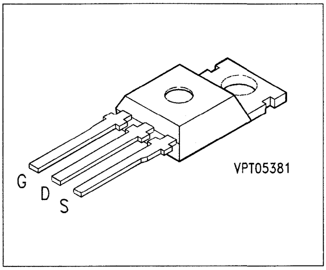
Typ. gate charge
$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls}$ = 22.5 A



SIPMOS® Power Transistors

BUZ 71 AL
BUZ 71 L

- N channel
- Enhancement mode
- Avalanche-rated
- Logic Level



Type	V_{DS}	I_D	T_C	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 71 AL	50 V	13 A	25 °C	0.12 Ω	TO-220 AB	C67078-S1326-A5
BUZ 71 L	50 V	14 A	28 °C	0.10 Ω	TO-220 AB	C67078-S1316-A2

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		71 L	**71 AL**	
Continuous drain current	I_D	**14**	**13**	A
Pulsed drain current	$I_{D\,puls}$	**56**	**52**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**14**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**1**		mJ
Avalanche energy, single pulse $I_D = 14$ A, $V_{DD} = 25$ V, $R_{GS} = 25\ \Omega$ $L = 30.6\ \mu$H, $T_j = 25$ °C	E_{AS}	**6**		
Gate-source voltage	V_{GS}	**± 10**		V
Gate-source peak voltage, aperiodic	V_{gs}	**± 20**		
Power dissipation, $T_C = 25$ °C	P_{tot}	**40**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	**typ.**	**max.**	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	50	–	–	V
Gate threshold voltage V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS\,(th)}$	1.5	2.0	2.5	
Zero gate voltage drain current V_{DS} = 50 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS\,(on)}$				Ω
V_{GS} = 5 V, I_D = 7.0 A BUZ 71 L		–	0.08	0.1	
BUZ 71 AL		–	0.09	0.12	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 7.0 A	g_{fs}	5.0	9.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	550	730	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	200	320	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	85	150	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	15	25	ns
	t_r	–	70	100	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	70	90	
	t_f	–	50	70	

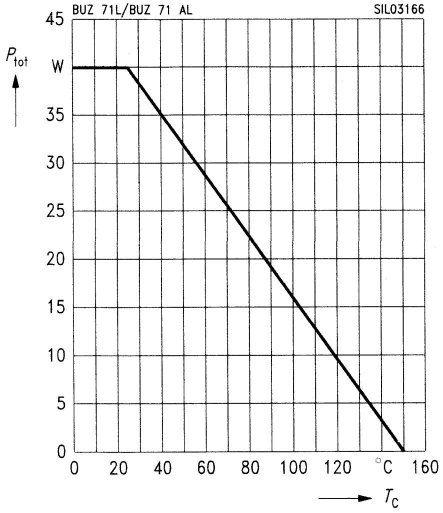
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter		**Symbol**	**Values**			**Unit**
			min.	**typ.**	**max.**	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 °C	BUZ 71 L		–		14	
	BUZ 71 AL		–		13	
Pulsed reverse drain current		I_{SM}				
T_C = 25 °C	BUZ 71 L		–		56	
	BUZ 71 AL		–		52	
Diode forward on-voltage I_S = 28 A, V_{GS} = 0 V		V_{SD}	–	1.3	1.8	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs		t_{rr}	–	120	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs		Q_{rr}	–	0.15	–	µC

Characteristics at $T_j = 25\ ^\circ C$, unless otherwise specified.

Total power dissipation

$P_{tot} = f(T_C)$

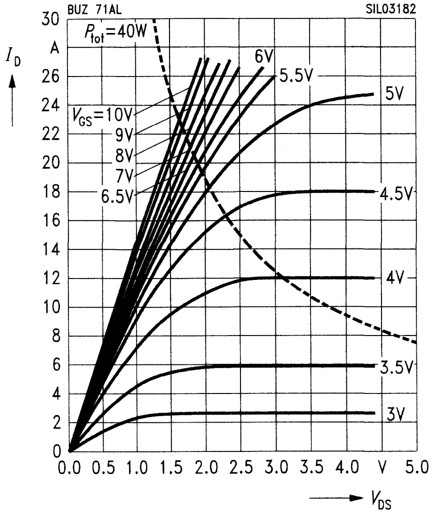


Typ. output characteristics

$I_D = f(V_{DS})$

BUZ 71 AL

parameter: $t_p = 80\ \mu s$

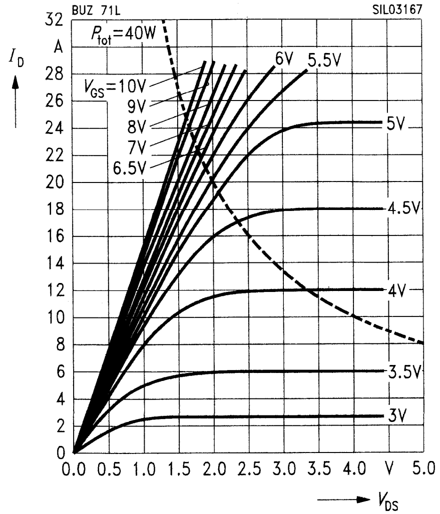


Typ. output characteristics

$I_D = f(V_{DS})$

BUZ 71 L

parameter: $t_p = 80\ \mu s$

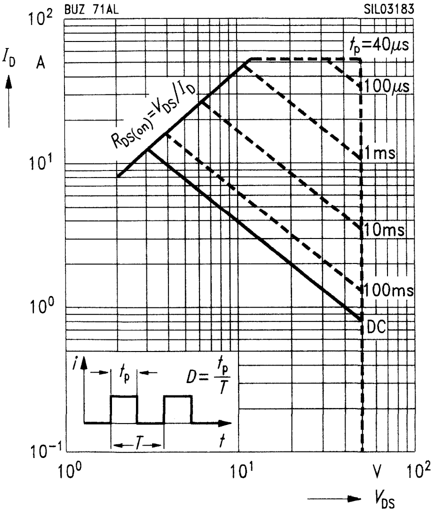


Safe operating area

$I_D = f(V_{DS})$

BUZ 71 AL

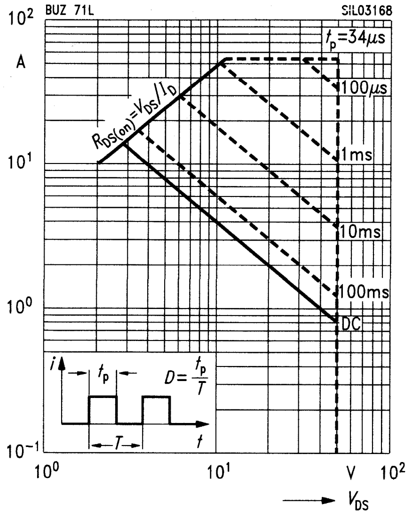
parameter: $D = 0.01$, $T_C = 25\ ^\circ C$



Safe operating area

$I_D = f(V_{DS})$ **BUZ 71 L**

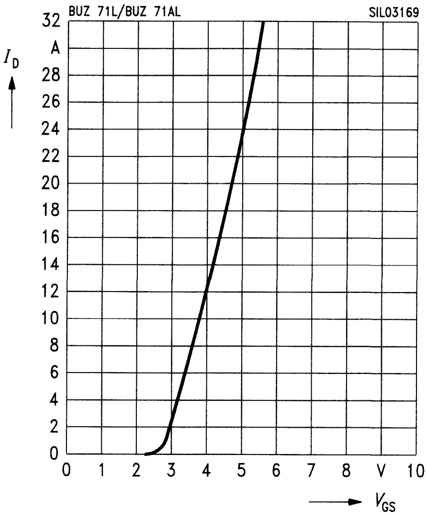
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

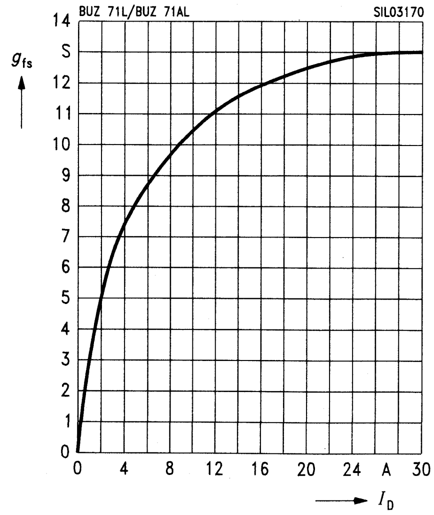
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. forward transconductance

$g_{fs} = f(I_D)$

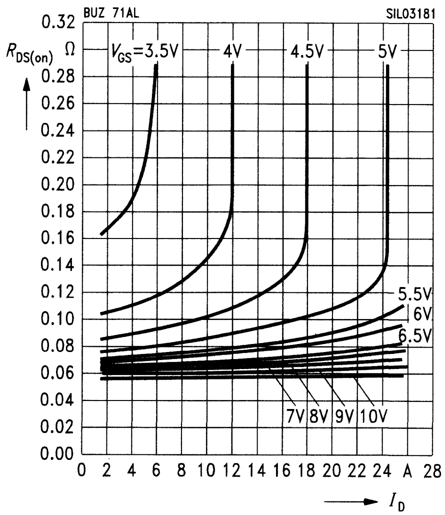
parameter: t_p = 80 µs



Typ. drain-source on-resistance

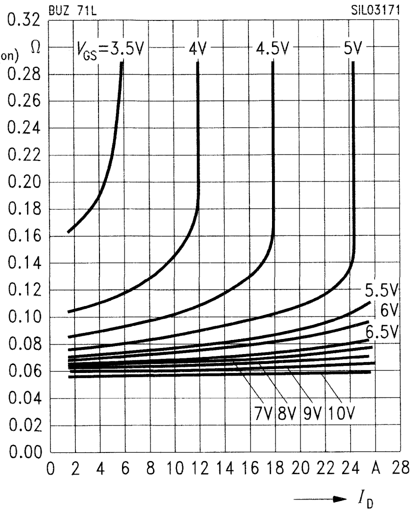
$R_{DS\,(on)} = f(I_D)$ **BUZ 71 AL**

parameter: V_{GS}



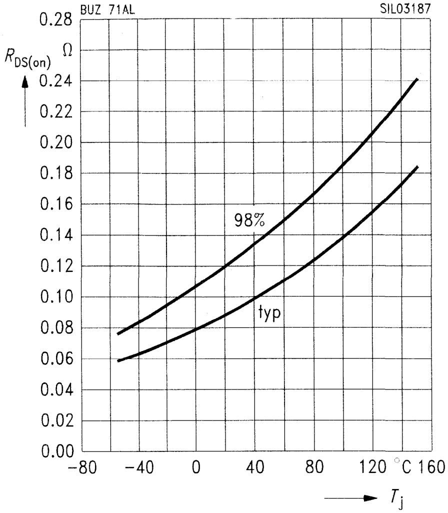
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 71 L**
parameter: V_{GS}



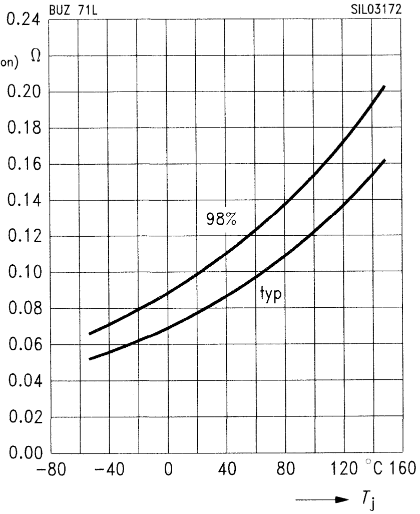
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 71 AL**
parameter: I_D = 7 A, V_{GS} = 5 V, (spread)



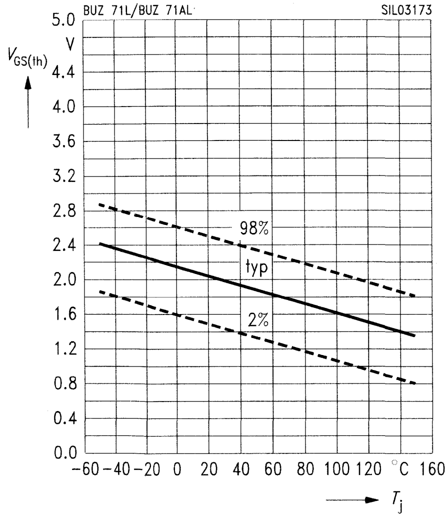
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 71 L**
parameter: I_D = 7 A, V_{GS} = 5 V, (spread)

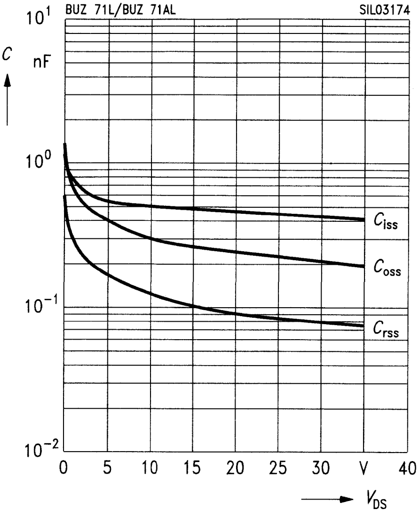


Gate threshold voltage

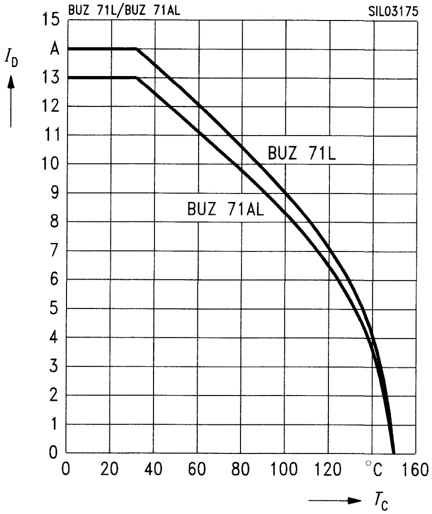
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



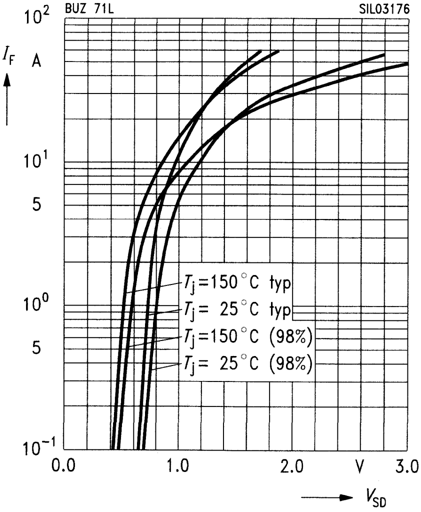
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



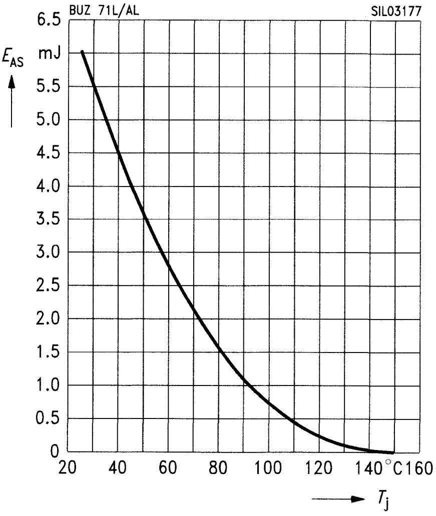
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 5$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs, (spread)

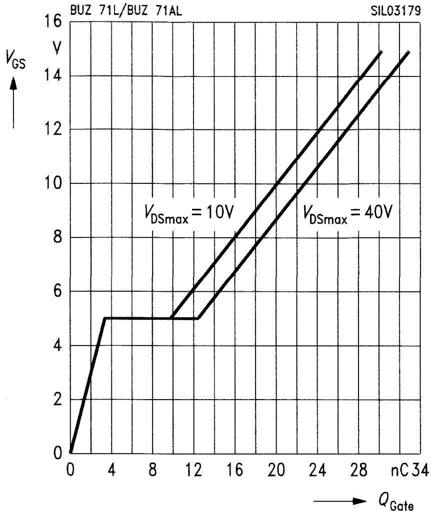


Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 14$ A, $V_{DD} = 25$ V
$R_{GS} = 25\ \Omega$, $L = 30.6$ µH



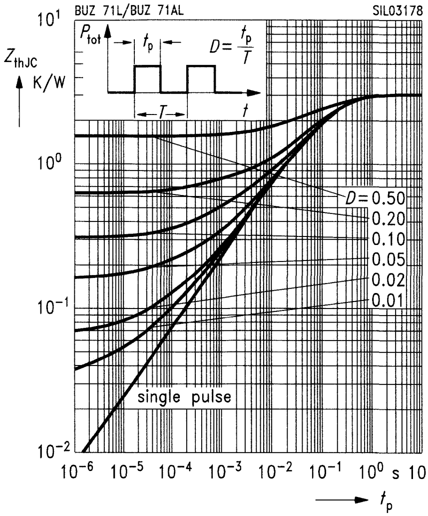
Typ. gate charge

$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 21$ A



Transient thermal impedance

$Z_{th\ JC} = f(t_p)$
parameter: $D = t_p / T$



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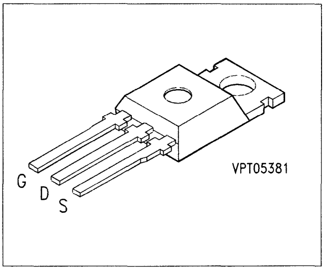
SIPMOS® Power Transistors

BUZ 72
BUZ 72 A

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 72	100 V	10 A	0.20 Ω	TO-220 AB	C67078-S1313-A2
BUZ 72 A	100 V	9.0 A	0.25 Ω	TO-220 AB	C67078-S1313-A3

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		72	72 A	
Continuous drain current, T_C = 25 °C	I_D	**10**	**9.0**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**40**	**36**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**10**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**7.9**		mJ
Avalanche energy, single pulse I_D = 10 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 885 µH, T_j = 25 °C	E_{AS}	**59**		
Gate-source voltage	V_{GS}	**± 20**		V
Power dissipation, T_C = 25 °C	P_{tot}	**40**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	100	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 100 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS\,(on)}$				Ω
V_{GS} = 10 V, I_D = 6 A BUZ 72		–	0.15	0.2	
BUZ 72 A		–	0.2	0.25	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 6 A	g_{fs}	3.0	4.3	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	400	530	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	120	180	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	70	105	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	10	15	ns
	t_r	–	45	70	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	55	75	
	t_f	–	40	55	

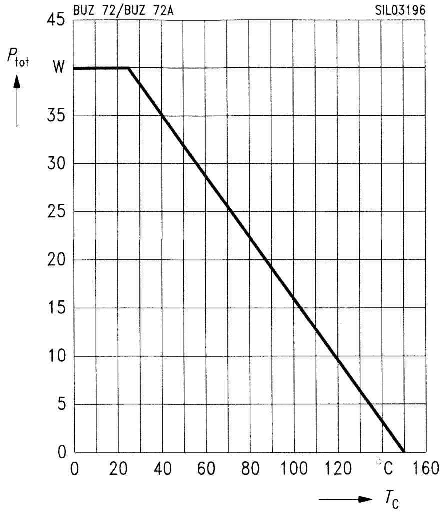
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter		Symbol	Values			Unit
			min.	typ.	max.	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 ˚C	BUZ 72		–	–	10	
	BUZ 72 A		–	–	9.0	
Pulsed reverse drain current		I_{SM}				
T_C = 25 ˚C	BUZ 72		–	–	40	
	BUZ 72 A		–	–	36	
Diode forward on-voltage I_S = 20 A, V_{GS} = 0 V		V_{SD}	–	1.4	1.6	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs		t_{rr}	–	170	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs		Q_{rr}	–	0.30	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Total power dissipation

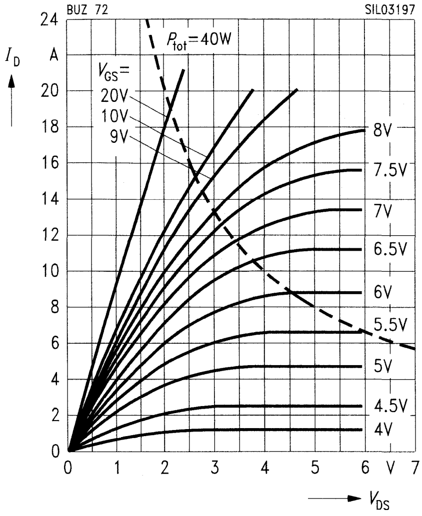
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 72**

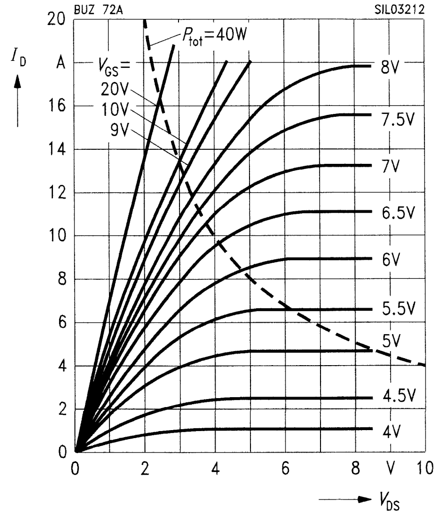
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 72 A**

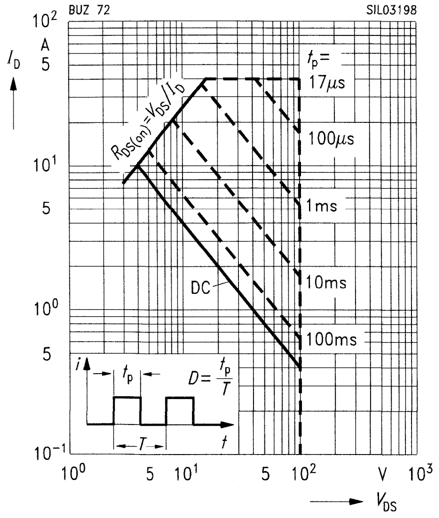
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$ **BUZ 72**

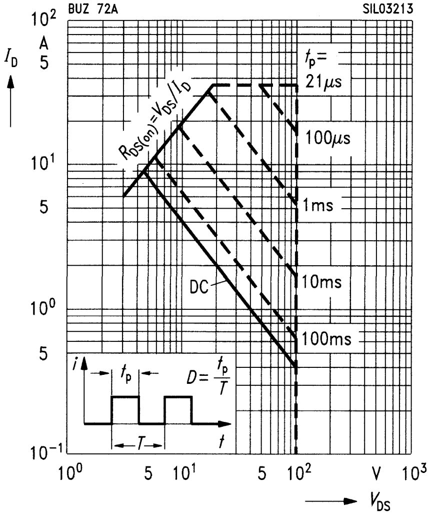
parameter: D = 0.01, T_C = 25 °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 72 A**

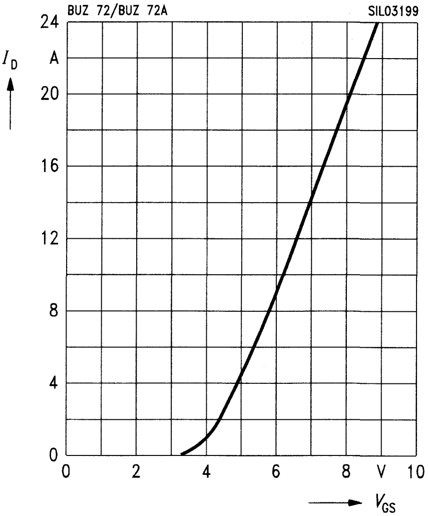
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

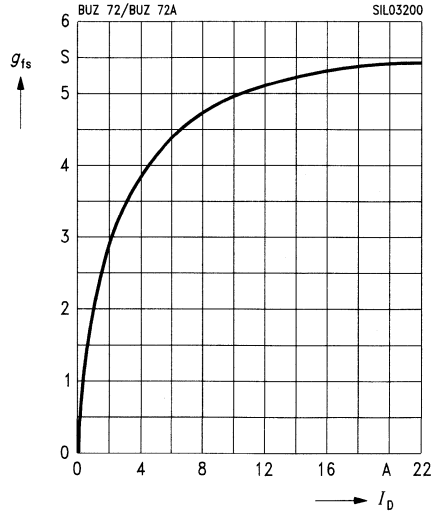
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



Typ.forward transconductance

$g_{fs} = f(I_D)$

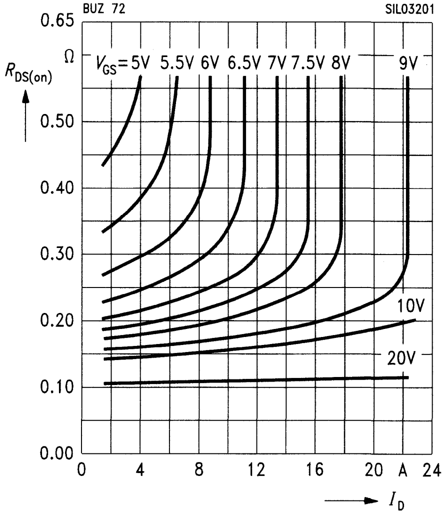
parameter: $t_p = 80$ µs



Typ. drain-source on-resistance

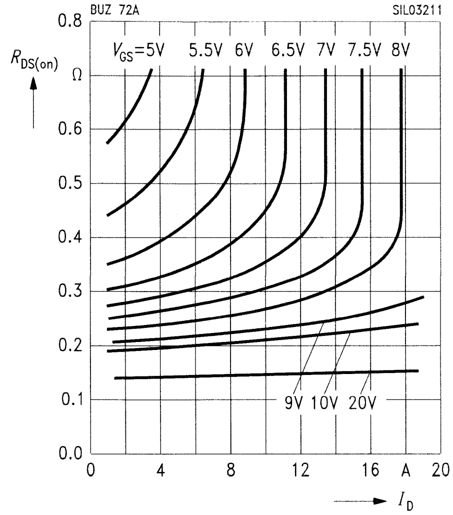
$R_{DS(on)} = f(I_D)$ **BUZ 72**

parameter: V_{GS}



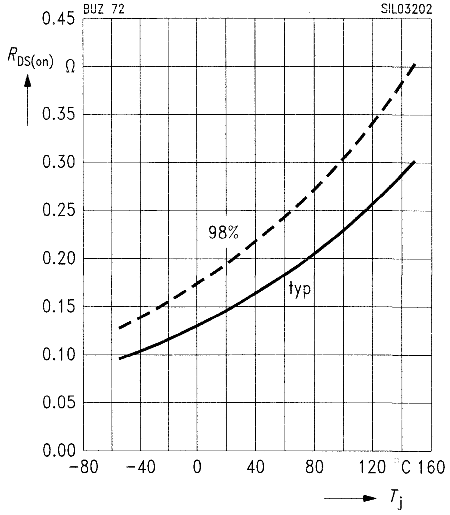
Typ. drain-source on-resistance

$R_{\mathrm{DS\,(on)}} = f\,(I_{\mathrm{D}})$ **BUZ 72 A**
parameter: V_{GS}



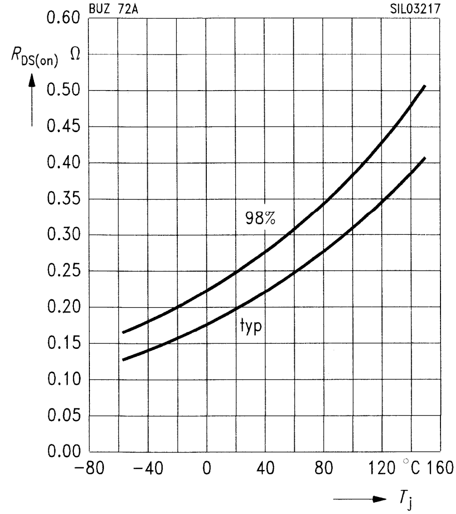
Drain-source on-resistance

$R_{\mathrm{DS\,(on)}} = f\,(T_{\mathrm{j}})$ **BUZ 72**
parameter: I_{D} = 6 A, V_{GS} = 10 V, (spread)



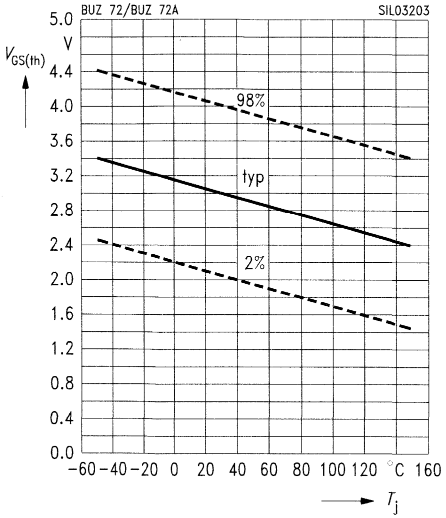
Drain-source on-resistance

$R_{\mathrm{DS\,(on)}} = f\,(T_{\mathrm{j}})$ **BUZ 72 A**
parameter: I_{D} = 6 A, V_{GS} = 10 V, (spread)



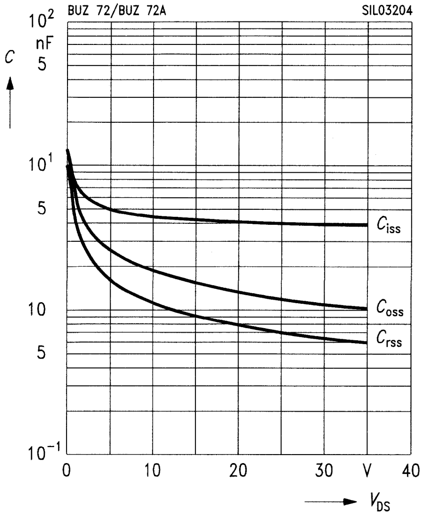
Gate threshold voltage

$V_{\mathrm{GS\,(th)}} = f\,(T_{\mathrm{j}})$
parameter: $V_{\mathrm{GS}} = V_{\mathrm{DS}}$, I_{D} = 1 mA, (spread)



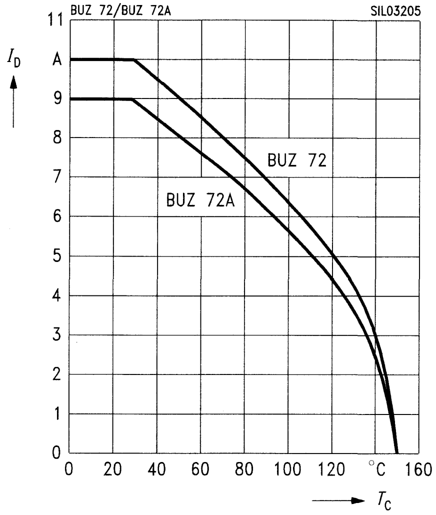
Typ. capacitances

$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



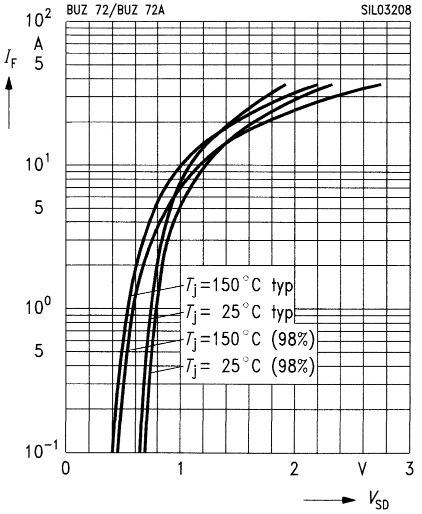
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



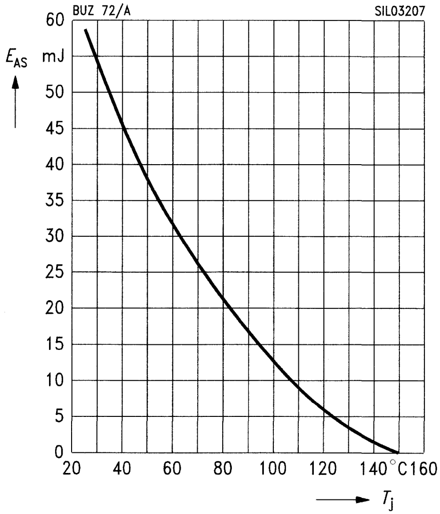
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs, (spread)

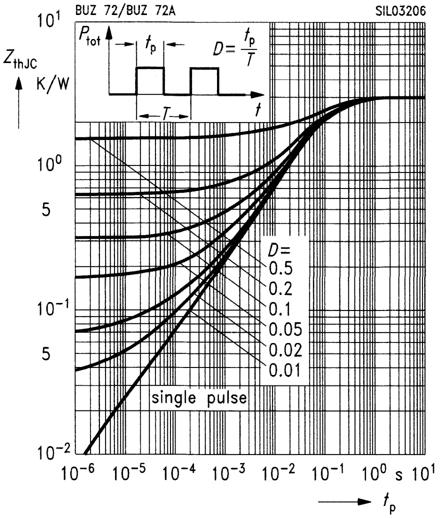


Avalanche energy $E_{AS} = f(T_j)$

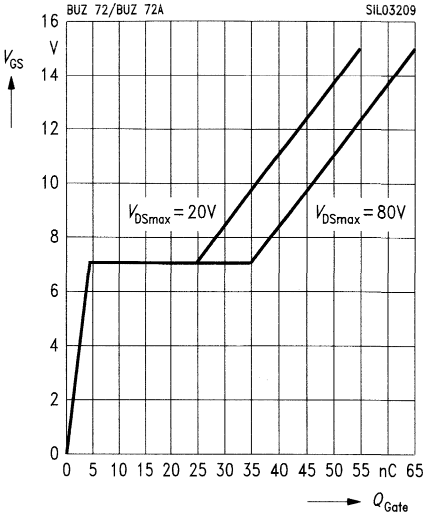
parameter: $I_D = 10$ A, $V_{DD} = 25$ V
$R_{GS} = 25$ Ω, $L = 885$ µH



Transient thermal impedance
$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge
$V_{GS} = f(Q_{\text{Gate}})$
parameter: $I_{\text{D puls}} = 21$ A

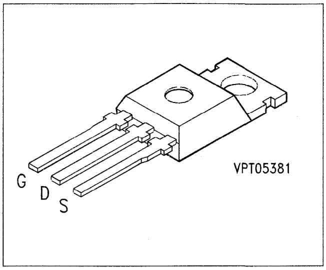


SIEMENS

SIPMOS® Power Transistors

BUZ 72 AL
BUZ 72 L

- N channel
- Enhancement mode
- Avalanche-rated
- Logic Level



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1)]	Ordering Code
BUZ 72 AL	100 V	9.0 A	0.025 Ω	TO-220 AB	C67078-S1327-A3
BUZ 72 L	100 V	10 A	0.020 Ω	TO-220 AB	C67078-S1327-A2

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		72 L	72 AL	
Continuous drain current, T_C = 25 ˚C	I_D	**10**	**9.0**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**40**	**36**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**10**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**7.9**		mJ
Avalanche energy, single pulse I_D = 10 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 885 µH, T_j = 25 ˚C	E_{AS}	**59**		
Gate-source voltage	V_{GS}	**± 10**		V
Gate-source peak voltage, aperiodic	V_{gs}	**± 20**		
Power dissipation, T_C = 25 ˚C	P_{tot}	**40**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	100	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	1.5	2.0	2.5	
Zero gate voltage drain current V_{DS} = 100 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS\,(on)}$				Ω
V_{GS} = 5 V, I_D = 5 A BUZ 72 AL		–	0.15	0.25	
BUZ 72 L		–	0.12	0.2	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 5 A	g_{fs}	5.0	7.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	680	900	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	180	250	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	90	150	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	20	30	ns
	t_r	–	85	130	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	100	130	
	t_f	–	55	70	

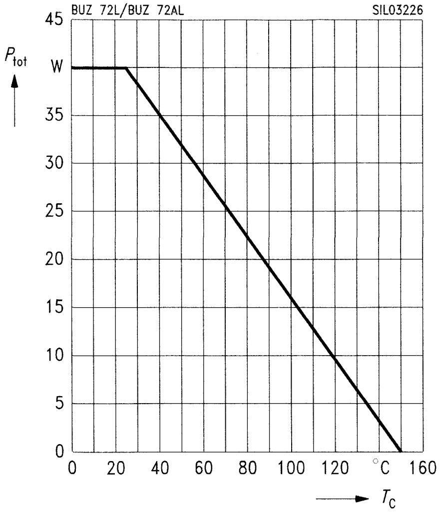
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter		Symbol	Values			Unit
			min.	typ.	max.	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 °C	BUZ 72 AL		–		9.0	
	BUZ 72 L		–		10	
Pulsed reverse drain current		I_{SM}				
T_C = 25 °C	BUZ 72 AL		–		36	
	BUZ 72 L		–		40	
Diode forward on-voltage I_F = 20 A, V_{GS} = 0 V		V_{SD}	–	1.2	1.5	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs		t_{rr}	–	180	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs		Q_{rr}	–	460	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

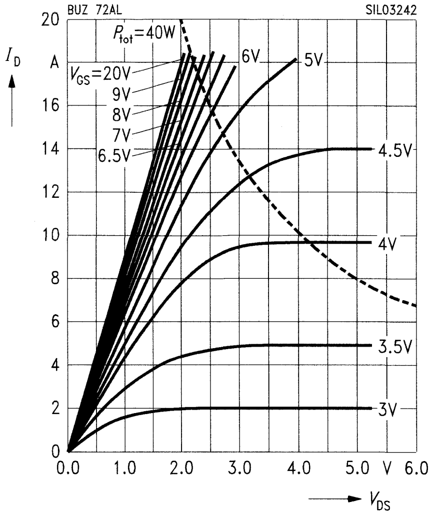
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 72 AL**

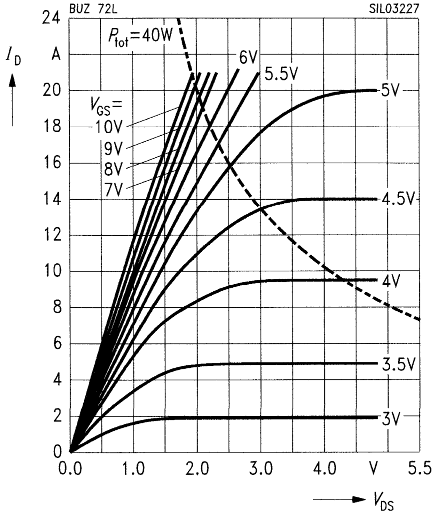
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 72 L**

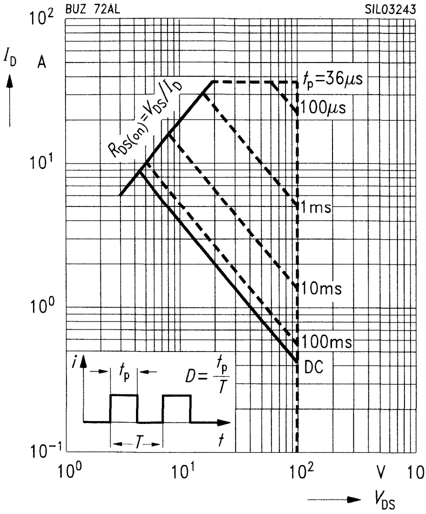
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$ **BUZ 72 AL**

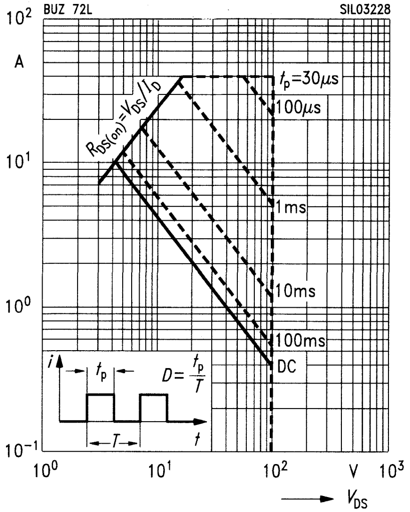
parameter: D = 0.01, T_C = 25 °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 72 L**

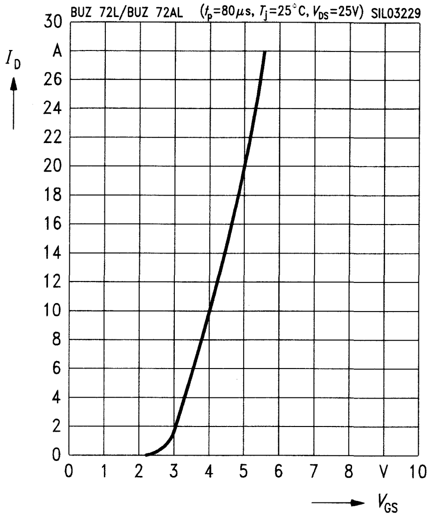
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

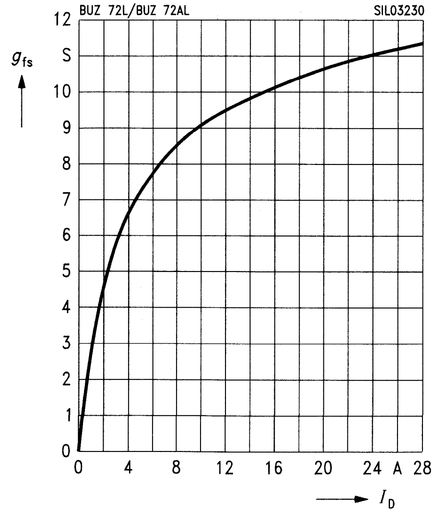
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ.forward transconductance

$g_{fs} = f(I_D)$

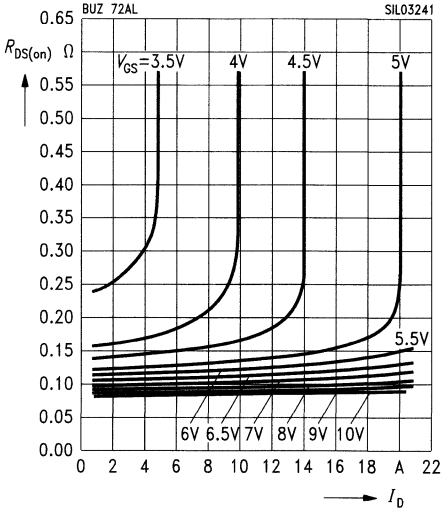
parameter: t_p = 80 µs



Typ. drain-source on-resistance

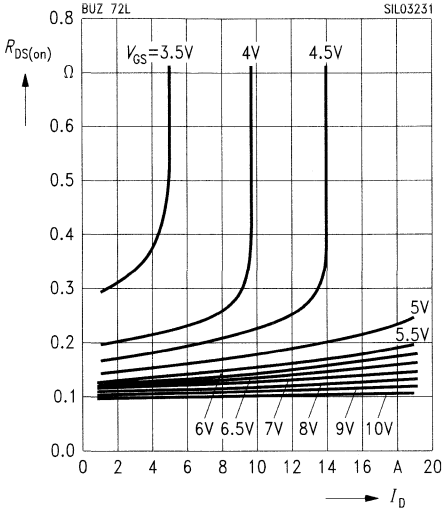
$R_{DS\,(on)} = f(I_D)$ **BUZ 72 AL**

parameter: V_{GS}



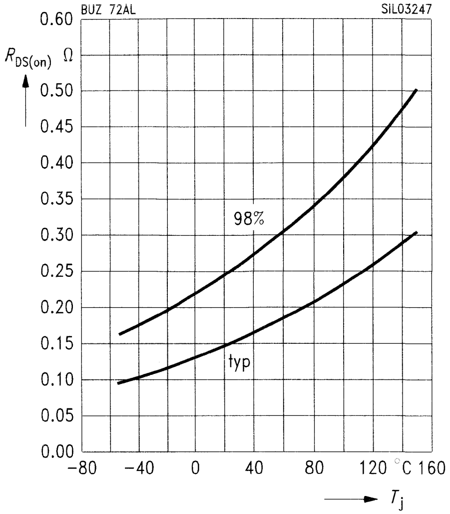
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 72 L**
parameter: V_{GS}



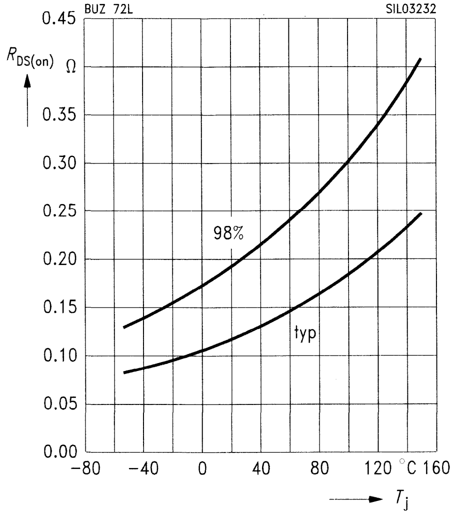
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 72 AL**
parameter: I_D = 5 A, V_{GS} = 5 V, (spread)



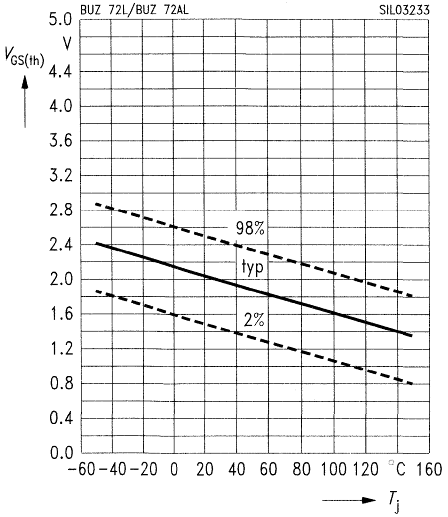
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 72 L**
parameter: I_D = 6 A, V_{GS} = 5 V, (spread)

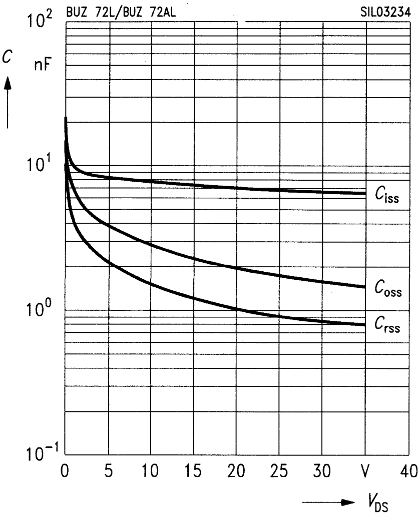


Gate threshold voltage

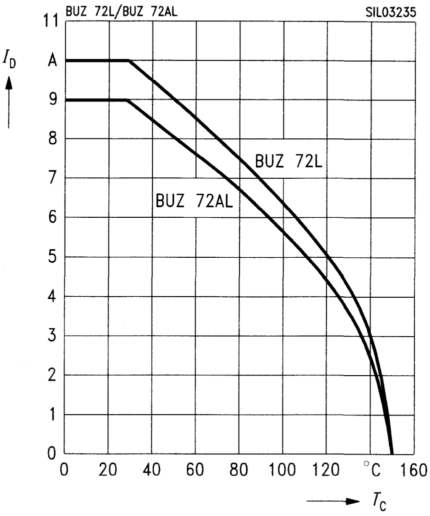
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



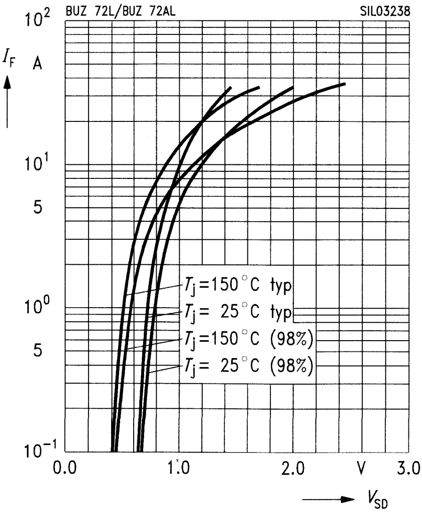
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



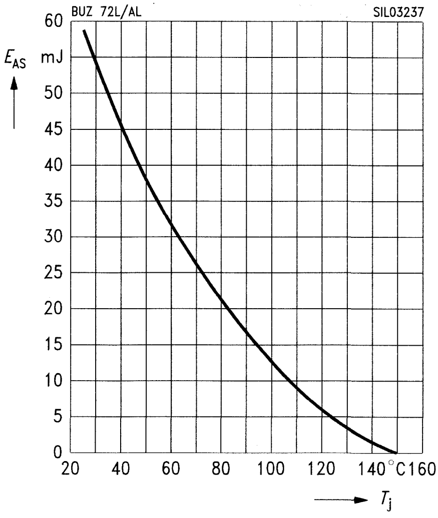
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 5$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs, (spread)



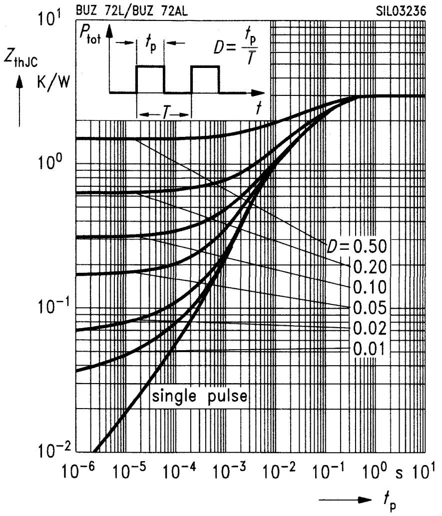
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 10$ A, $V_{DD} = 25$ V
$R_{GS} = 25\ \Omega$, $L = 885$ µH



Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

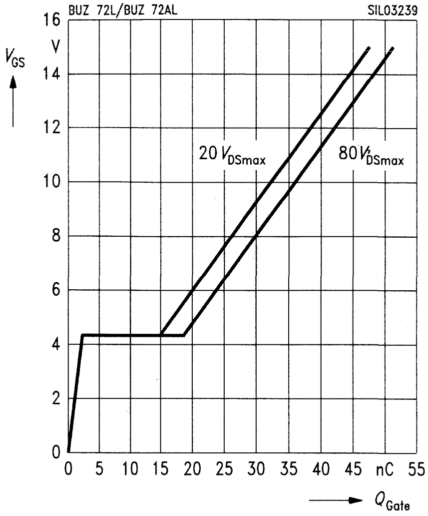
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{Gate})$

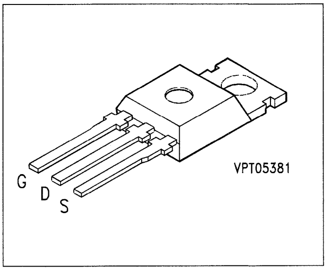
parameter: $I_{D\,puls} = 15$ A



SIPMOS® Power Transistors

BUZ 73
BUZ 73 A

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	T_C	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 73	200 V	7.0 A	28 °C	0.4 Ω	TO-220 AB	C67078-S1317-A2
BUZ 73 A	200 V	5.5 A	37 °C	0.6 Ω	TO-220 AB	C67078-S1317-A3

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		73	73 A	
Continuous drain current	I_D	**7.0**	**5.5**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**28**	**22**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**7.0**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**6.5**		mJ
Avalanche energy, single pulse $I_D = 7$ A, $V_{DD} = 50$ V, $R_{GS} = 25$ Ω $L = 3.67$ mH, $T_j = 25$ °C	E_{AS}	**120**		
Gate-source voltage	V_{GS}	**± 20**		V
Power dissipation, $T_C = 25$ °C	P_{tot}	**40**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values min.	Values typ.	Values max.	Unit
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	200	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 200 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS\,(on)}$				Ω
V_{GS} = 10 V, I_D = 4.5 A BUZ 73		–	0.3	0.4	
BUZ 73 A		–	0.5	0.6	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 4.5 A	g_{fs}	3.0	4.2	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	400	530	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	85	130	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	45	70	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	10	15	ns
	t_r	–	40	60	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	55	75	
	t_f	–	30	40	

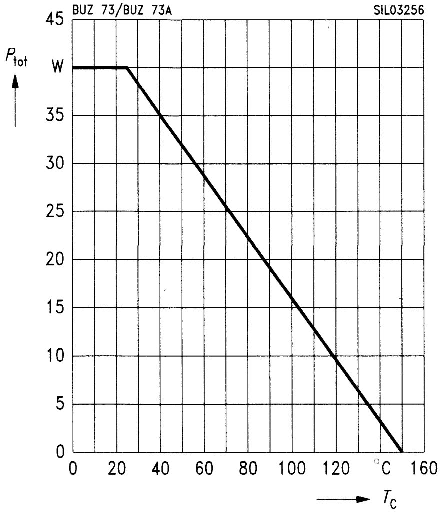
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter		Symbol	Values			Unit
			min.	typ.	max.	
Reverse diode						
Continuous reverse drain current T_C = 25 ˚C	 BUZ 73 BUZ 73 A	I_S	 – –	 – –	 7.0 5.5	A
Pulsed reverse drain current T_C = 25 ˚C	 BUZ 73 BUZ 73 A	I_{SM}	 – –	 – –	 28 22	
Diode forward on-voltage I_S = 14 A, V_{GS} = 0 V		V_{SD}	–	1.3	1.7	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		t_{rr}	–	200	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		Q_{rr}	–	0.60	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

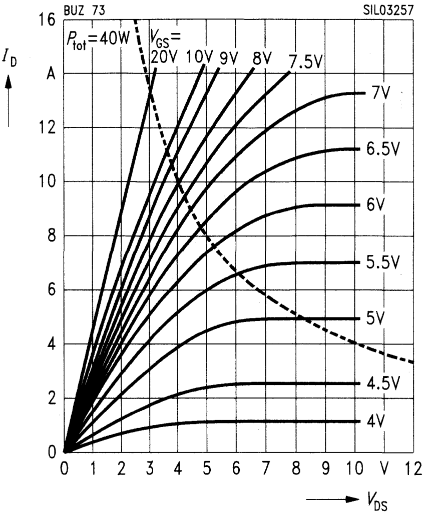
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 73**

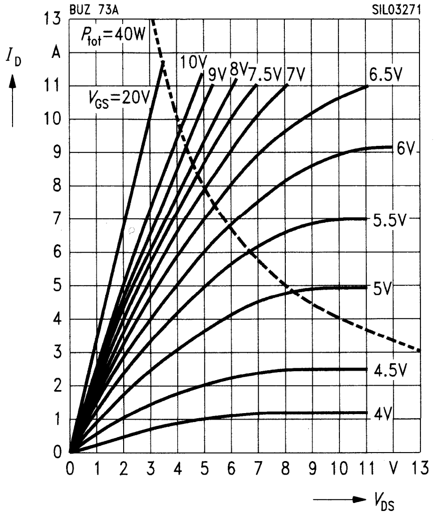
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 73 A**

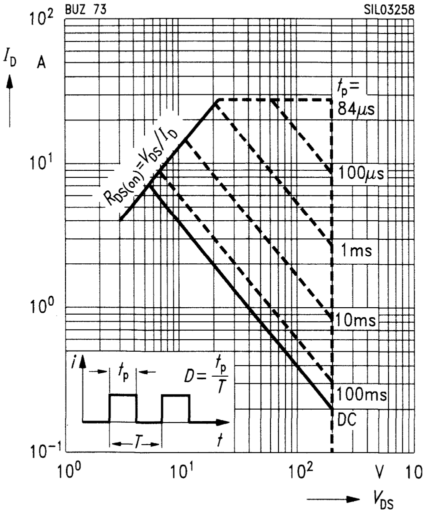
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$ **BUZ 73**

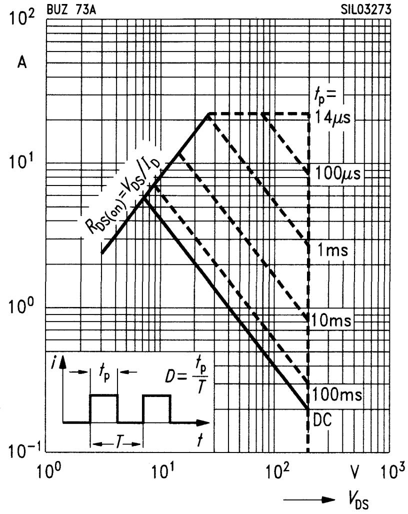
parameter: D = 0.01, T_C = 25 °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 73 A**

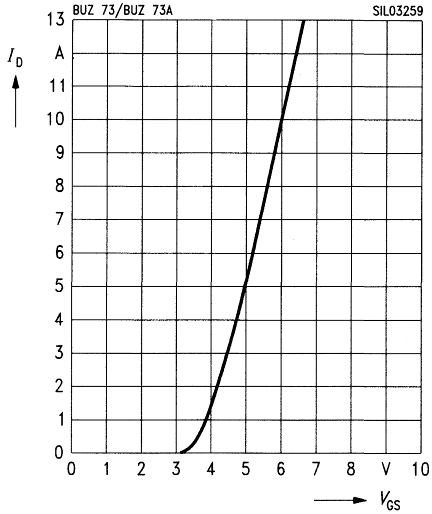
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

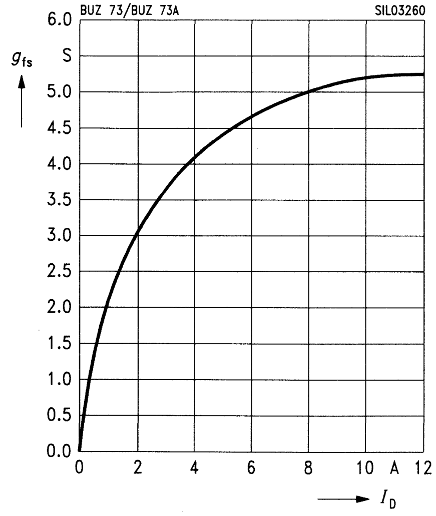
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



Typ.forward transconductance

$g_{fs} = f(I_D)$

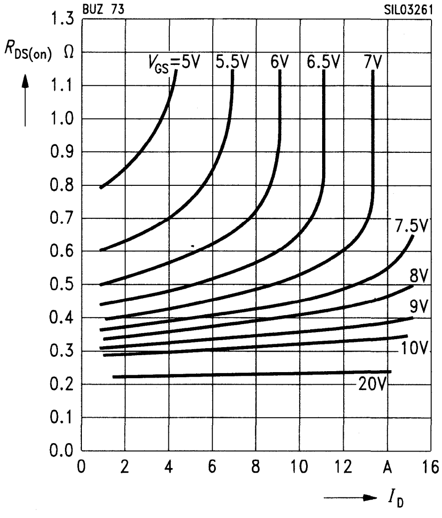
parameter: $t_p = 80$ µs



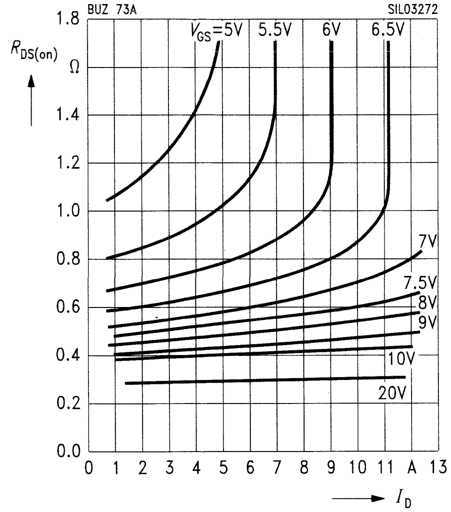
Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$ **BUZ 73**

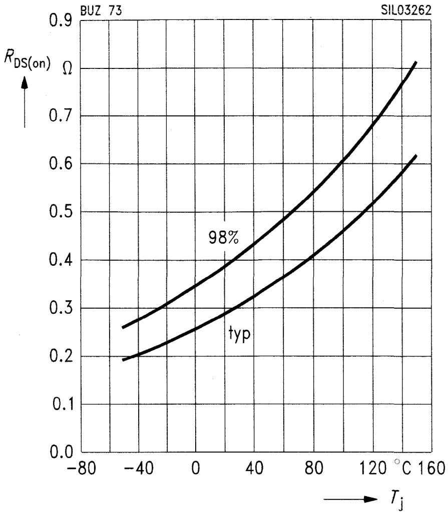
parameter: V_{GS}



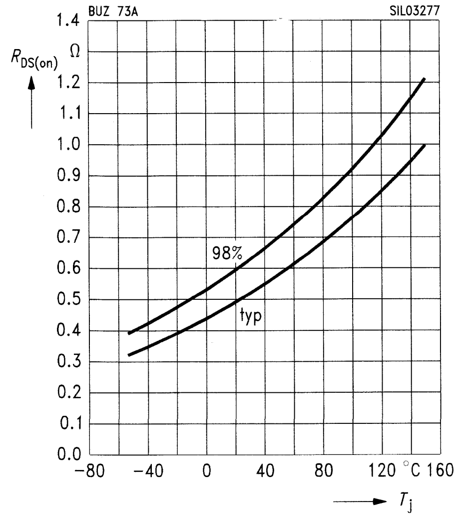
Typ. drain-source on-resistance
$R_{DS\,(on)} = f\,(I_D)$ **BUZ 73 A**
parameter: V_{GS}



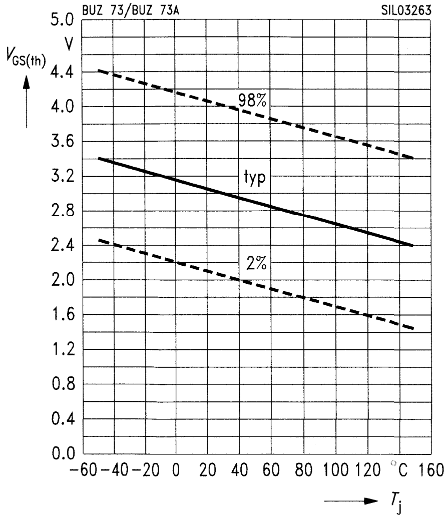
Drain-source on-resistance
$R_{DS\,(on)} = f\,(T_j)$ **BUZ 73**
parameter: I_D = 4.5 A, V_{GS} = 10 V, (spread)



Drain-source on-resistance
$R_{DS\,(on)} = f\,(T_j)$ **BUZ 73 A**
parameter: I_D = 4.5 A, V_{GS} = 10 V, (spread)



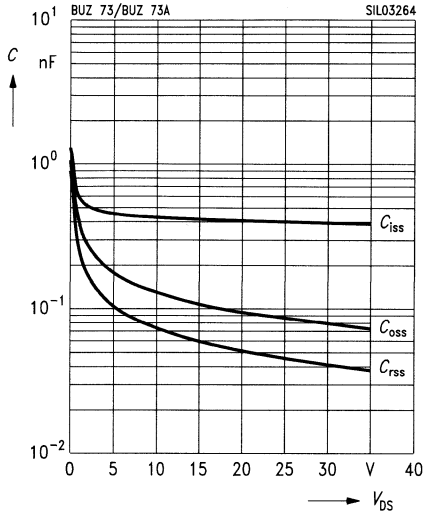
Gate threshold voltage
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

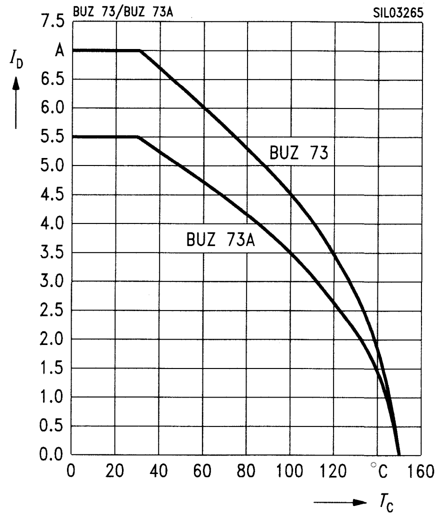
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

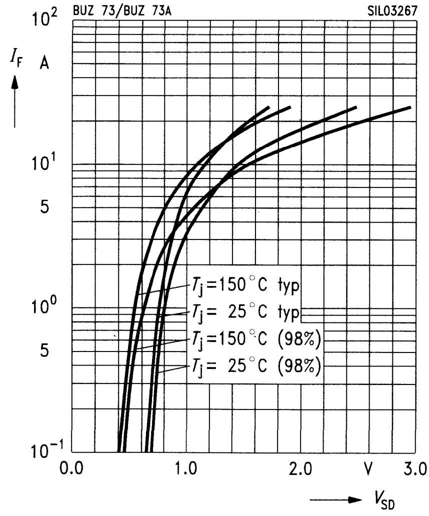
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

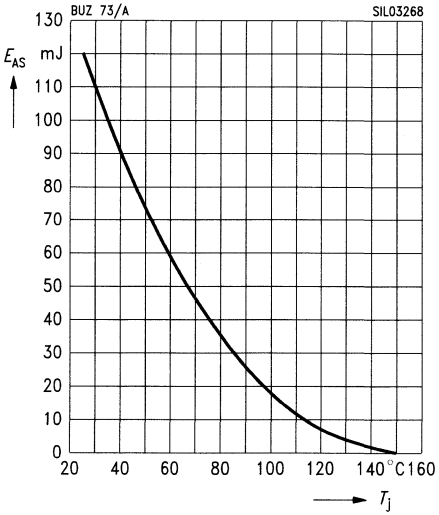
parameter: T_j, $t_p = 80$ µs



Avalanche energy $E_{AS} = f(T_j)$

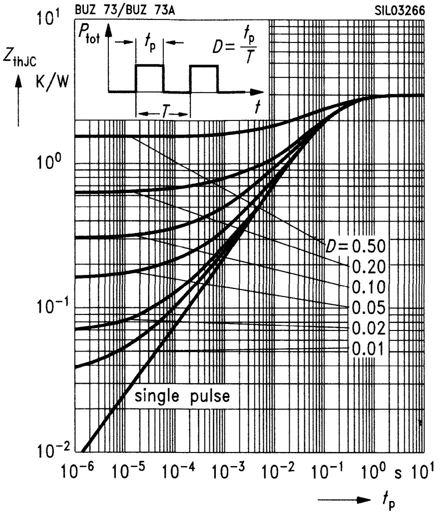
parameter: $I_D = 7$ A, $V_{DD} = 50$ V

$R_{GS} = 25\ \Omega$, $L = 3.67$ mH



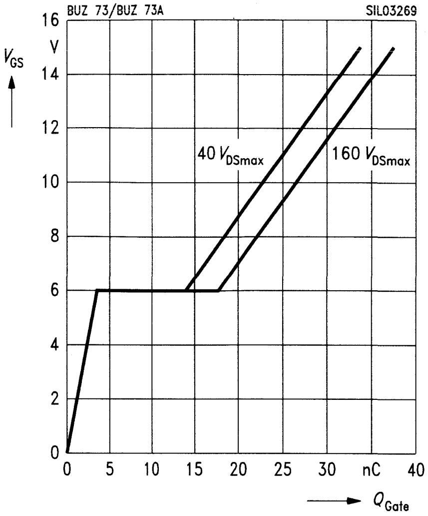
Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{\text{Gate}})$
parameter: $I_{\text{D puls}} = 13.5$ A

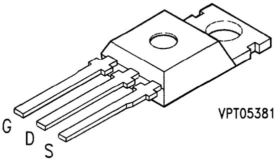


SIEMENS

SIPMOS® Power Transistors

BUZ 73 AL
BUZ 73 L

- N channel
- Enhancement mode
- Avalanche-rated
- Logic Level



Type	V_{DS}	I_D	T_C	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 73 AL	200 V	5.5 A	37 °C	0.4 Ω	TO-220 AB	C67078-S1328-A3
BUZ 73 L	200 V	7.0 A	28 °C	0.6 Ω	TO-220 AB	C67078-S1328-A2

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		73 AL	73 L	
Continuous drain current	I_D	**5.5**	**7.0**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**22**	**28**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**7**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**6.5**		mJ
Avalanche energy, single pulse $I_D = 7$ A, $V_{DD} = 50$ V, $R_{GS} = 25\ \Omega$ $L = 3.67$ mH, $T_j = 25$ °C	E_{AS}	**120**		
Gate-source voltage	V_{GS}	**± 10**		V
Gate-source peak voltage, aperiodic	V_{gs}	**± 20**		
Power dissipation, $T_C = 25$ °C	P_{tot}	**40**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	**typ.**	**max.**	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	200	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	1.5	2.0	2.5	
Zero gate voltage drain current V_{DS} = 200 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS\,(on)}$				Ω
V_{GS} = 5 V, I_D = 3.5 A BUZ 73 AL		–	0.5	0.6	
BUZ 73 L		–	0.3	0.4	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 3.5 A	g_{fs}	5.0	6.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	650	850	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	120	200	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	55	95	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	15	20	ns
	t_r	–	60	90	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 5 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	100	130	
	t_f	–	40	50	

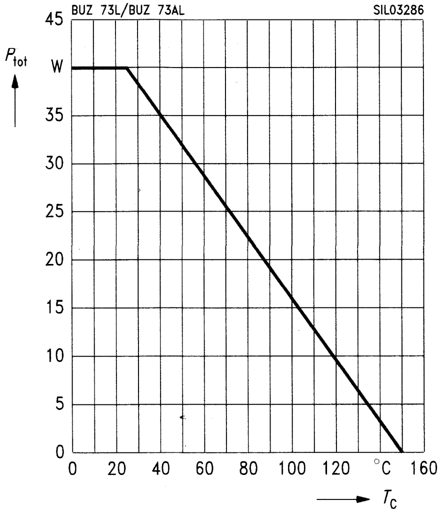
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter		Symbol	Values			Unit
			min.	typ.	max.	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 ˚C	BUZ 73 AL		–	–	5.5	
	BUZ 73 L		–	–	7.0	
Pulsed reverse drain current		I_{SM}				
T_C = 25 ˚C	BUZ 73 AL		–	–	22	
	BUZ 73 L		–	–	28	
Diode forward on-voltage I_S = 14 A, V_{GS} = 0 V		V_{SD}	–	1.1	1.7	V
Reverse recovery time V_R = 100 V, I_F = I_S , di_F / dt = 100 A/µs		t_{rr}	–	140	–	ns
Reverse recovery charge V_R = 100 V, I_F = I_S , di_F / dt = 100 A/µs		Q_{rr}	–	0.70	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

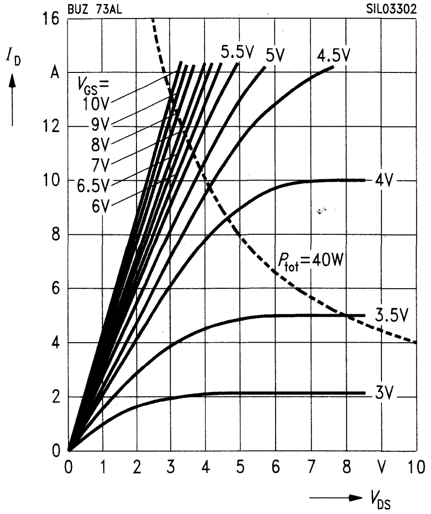
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 73 AL**

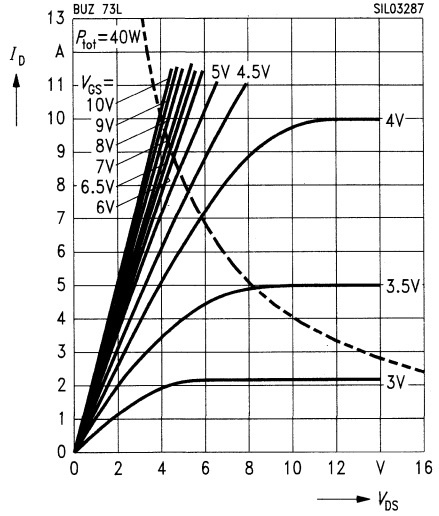
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 73 L**

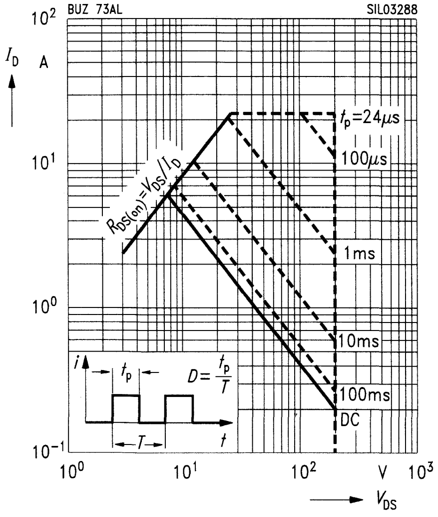
parameter: t_p = 80 µs



Safe operating area

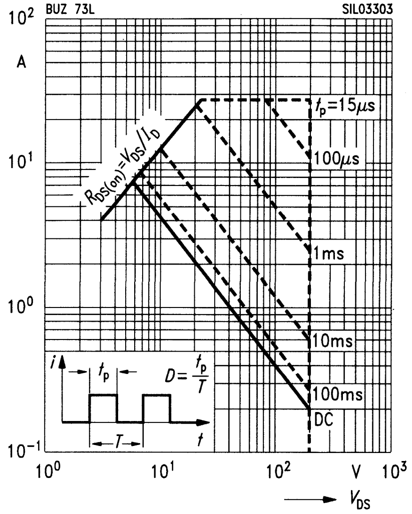
$I_D = f(V_{DS})$ **BUZ 73 AL**

parameter: D = 0.01, T_C = 25 °C



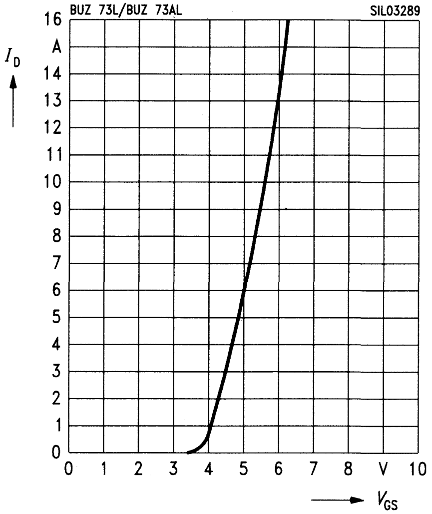
Safe operating area

$I_D = f(V_{DS})$ **BUZ 73 L**
parameter: $D = 0.01$, $T_C = 25$ °C



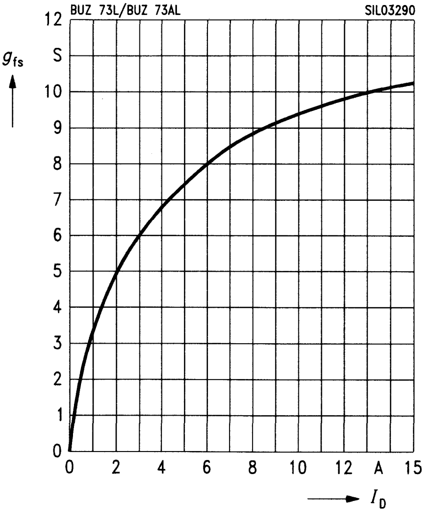
Typ. transfer characteristics

$I_D = f(V_{GS})$
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



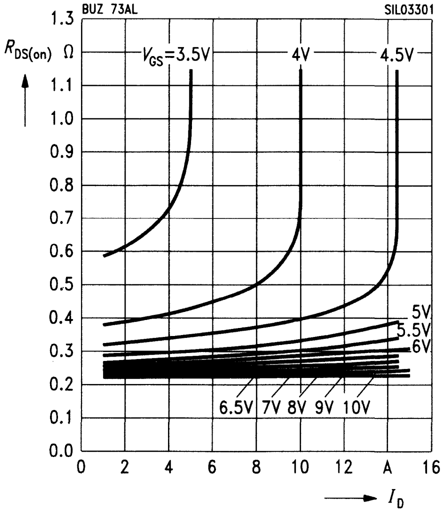
Typ.forward transconductance

$g_{fs} = f(I_D)$
parameter: $t_p = 80$ µs



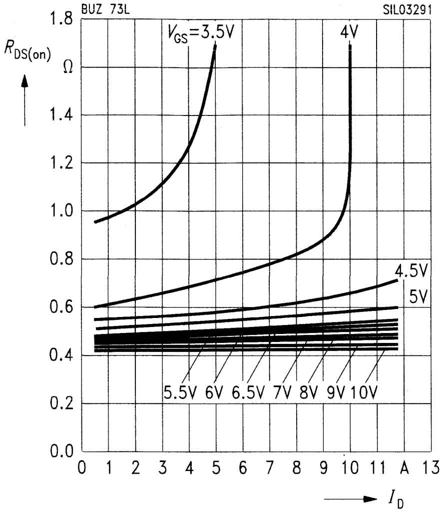
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 73 AL**
parameter: V_{GS}



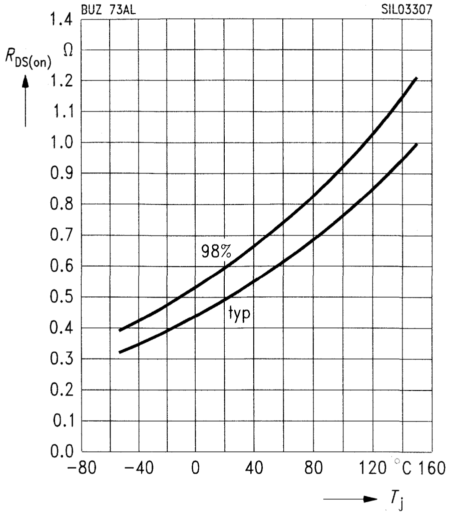
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 73 L**
parameter: V_{GS}



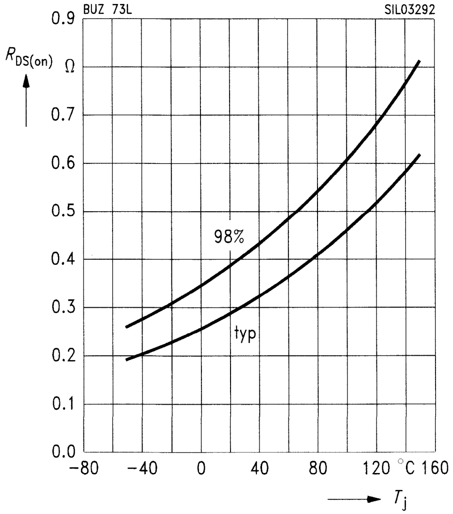
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 73 AL**
parameter: I_D = 4.5 A, V_{GS} = 5 V, (spread)



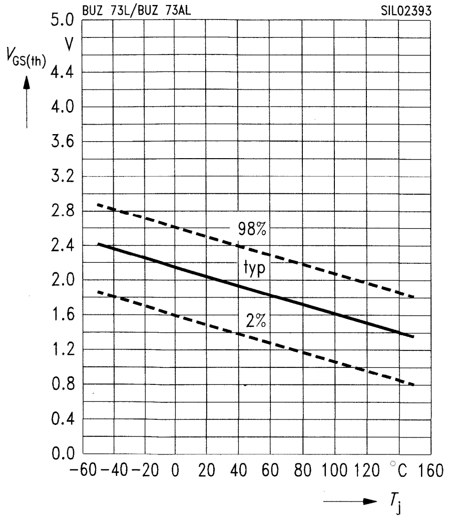
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 73 L**
parameter: I_D = 4.5 A, V_{GS} = 5 V, (spread)



Gate threshold voltage

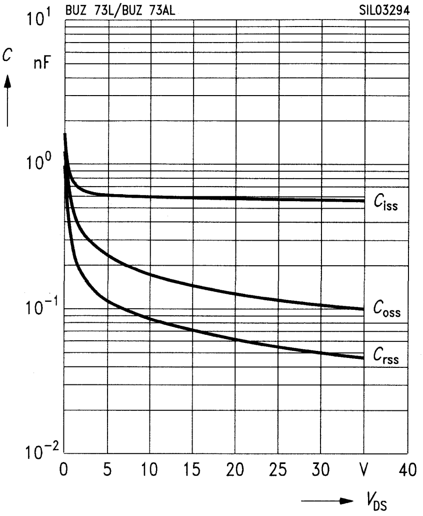
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

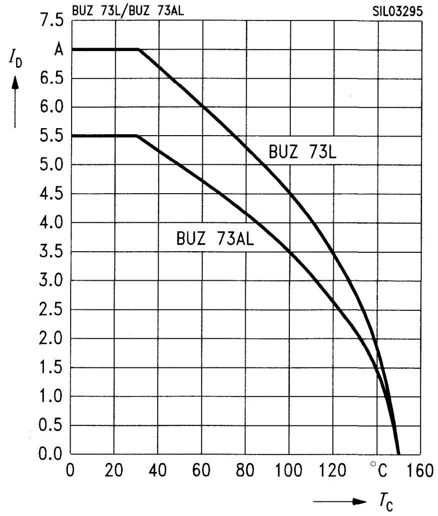
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

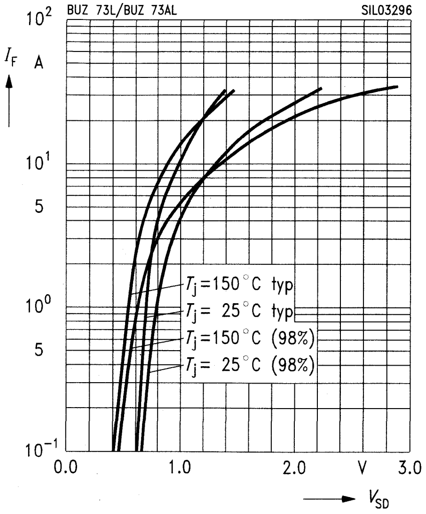
parameter: $V_{GS} \geq 5$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

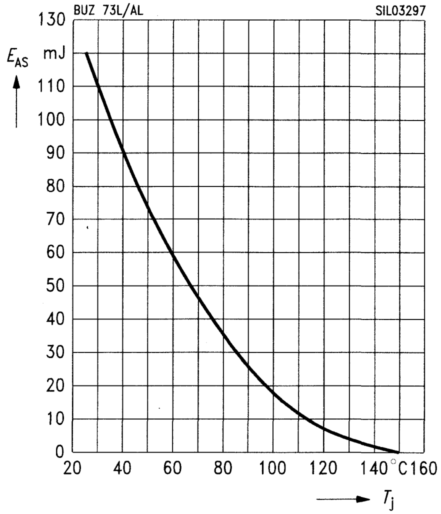
parameter: T_j , $t_p = 80$ µs



Avalanche energy $E_{AS} = f(T_j)$

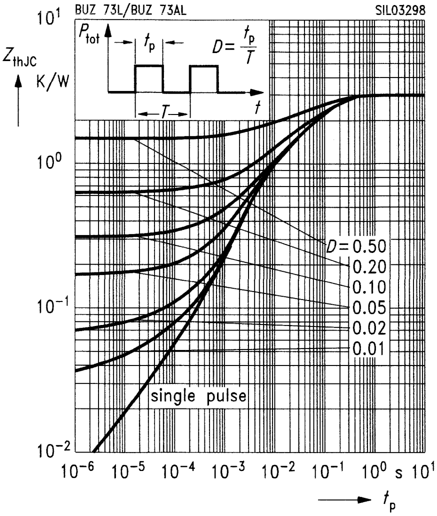
parameter: $I_D = 7$ A, $V_{DD} = 50$ V

$R_{GS} = 25\ \Omega$, $L = 3.67$ mH



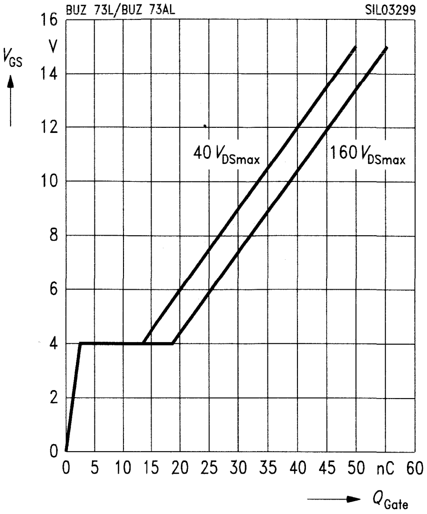
Transient thermal impedance

$Z_{\mathrm{th\,JC}} = f\,(t_\mathrm{p})$
parameter: $D = t_\mathrm{p} / T$



Typ. gate charge

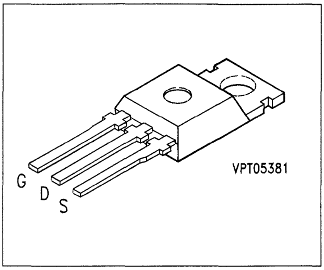
$V_{\mathrm{GS}} = f\,(Q_{\mathrm{Gate}})$
parameter: $I_{\mathrm{D\,puls}} = 10.5$ A



SIPMOS® Power Transistors

BUZ 74
BUZ 74 A

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	T_C	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 74	500 V	2.4 A	30 ˚C	3.0 Ω	TO-220 AB	C67078-S1314-A2
BUZ 74 A	500 V	2.1 A	27 ˚C	4.0 Ω	TO-220 AB	C67078-S1314-A3

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		74	74 A	
Continuous drain current	I_D	**2.4**	**2.1**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**9.5**	**8.5**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**2.4**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**5**		mJ
Avalanche energy, single pulse I_D = 2.4 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 56.3 mH, T_j = 25 ˚C	E_{AS}	**180**		
Gate-source voltage	V_{GS}	**± 20**		V
Power dissipation, T_C = 25 ˚C	P_{tot}	**40**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		˚C

Parameter	Symbol	BUZ	Unit
Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	500	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 500 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS\,(on)}$				Ω
V_{GS} = 10 V, I_D = 1.5 A BUZ 74		–	2.5	3.0	
BUZ 74 A		–	3.5	4.0	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 1.5 A	g_{fs}	1.8	2.1	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	450	675	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	50	75	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	20	30	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.1 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	8	12	ns
	t_r	–	40	60	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.1 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	50	65	
	t_f	–	30	40	

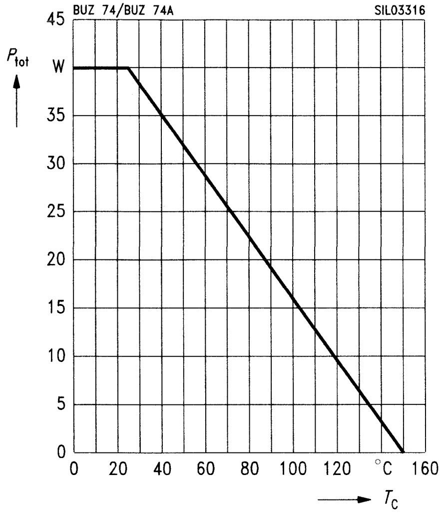
Electrical Characteristics (cont'd)

at T_j = 25 °C, unless otherwise specified.

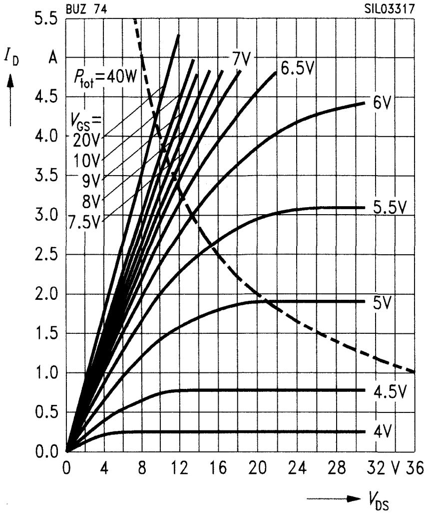
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C BUZ 74 BUZ 74 A	I_S	 – –	 – –	 2.4 2.1	A
Pulsed reverse drain current T_C = 25 °C BUZ 74 BUZ 74 A	I_{SM}	 – –	 – –	 9.5 8.5	
Diode forward on-voltage I_S = 4.8 A, V_{GS} = 0 V	V_{SD}	–	1.0	1.3	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	300	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	2.5	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

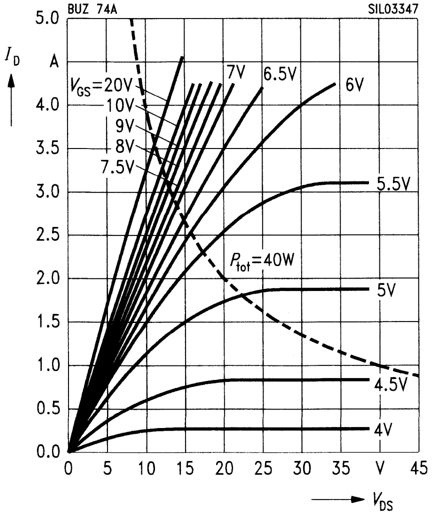
Total power dissipation
$P_{tot} = f(T_C)$



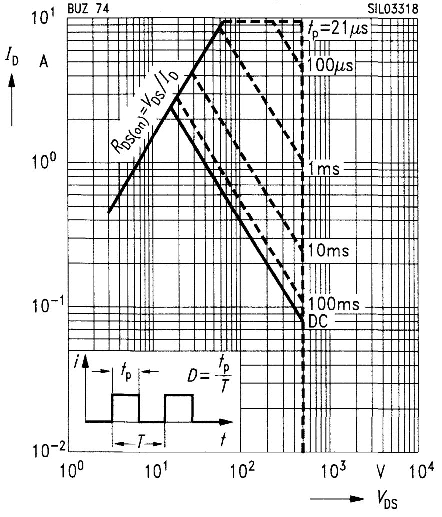
Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 74**
parameter: t_p = 80 µs



Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 74 A**
parameter: t_p = 80 µs



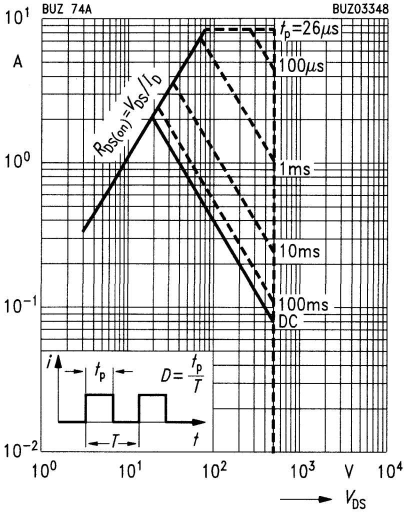
Safe operating area
$I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 74 A**

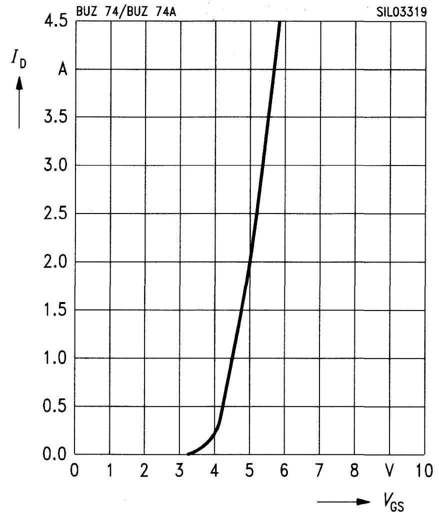
parameter: $D = 0.01$, $T_C = 25\ ^\circ C$



Typ. transfer characteristics

$I_D = f(V_{GS})$

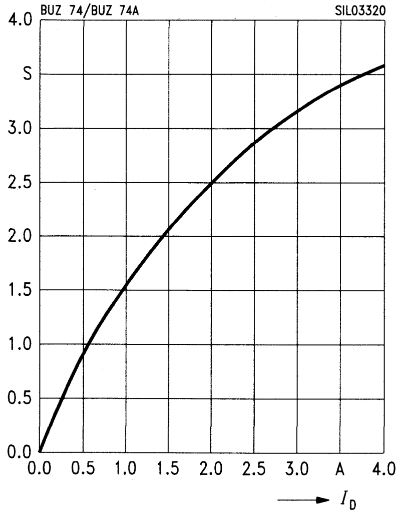
parameter: $t_p = 80\ \mu s$, $V_{DS} = 25$ V



Typ.forward transconductance

$g_{fs} = f(I_D)$

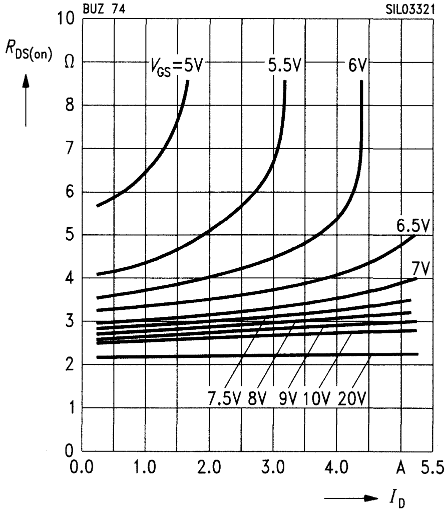
parameter: $t_p = 80\ \mu s$



Typ. drain-source on-resistance

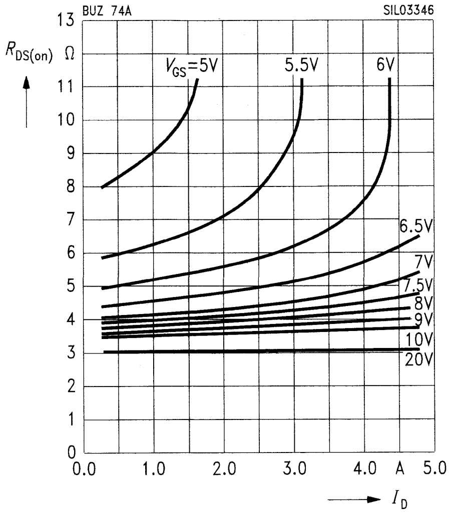
$R_{DS\,(on)} = f(I_D)$ **BUZ 74**

parameter: V_{GS}



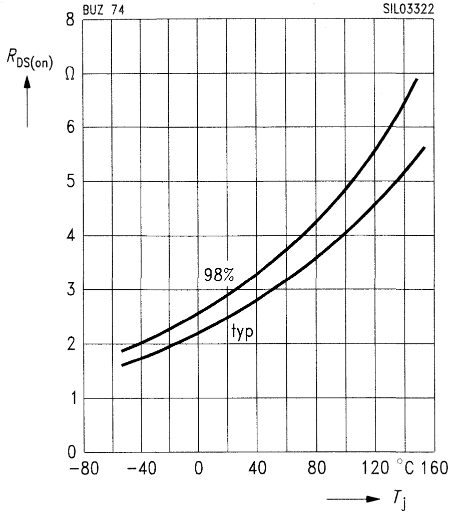
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 74 A**
parameter: V_{GS}



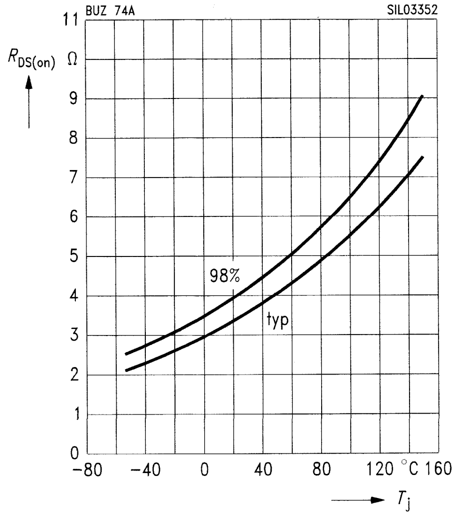
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 74**
parameter: I_D = 1.5 A, V_{GS} = 10 V, (spread)



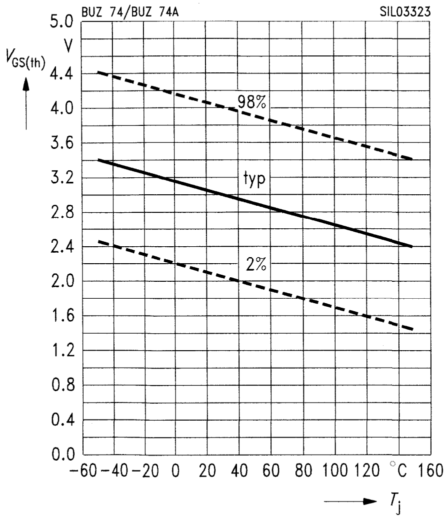
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 74 A**
parameter: I_D = 1.5 A, V_{GS} = 10 V, (spread)

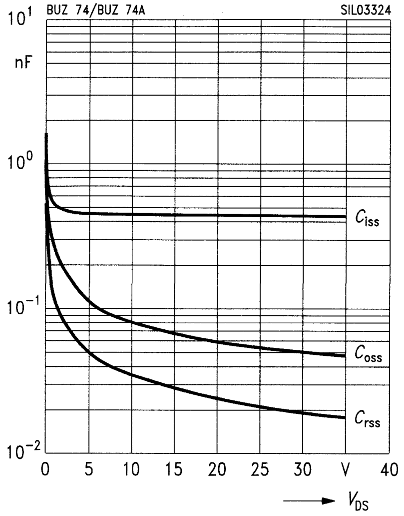


Gate threshold voltage

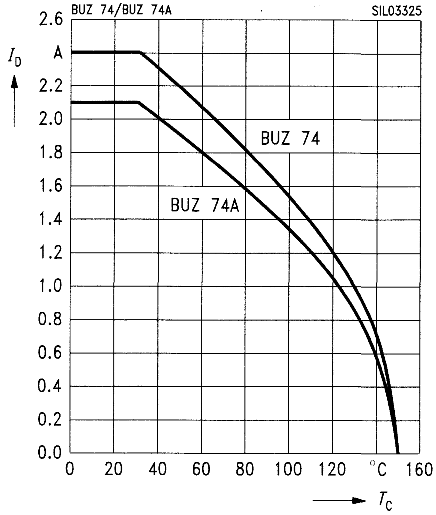
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



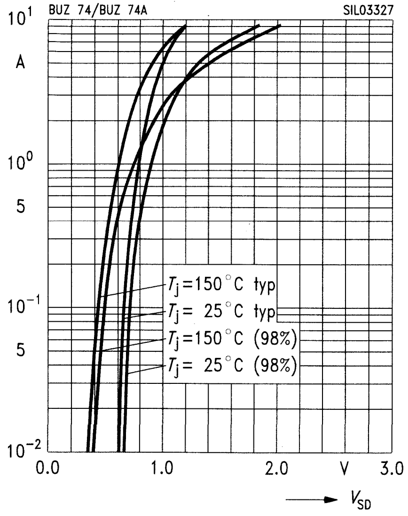
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



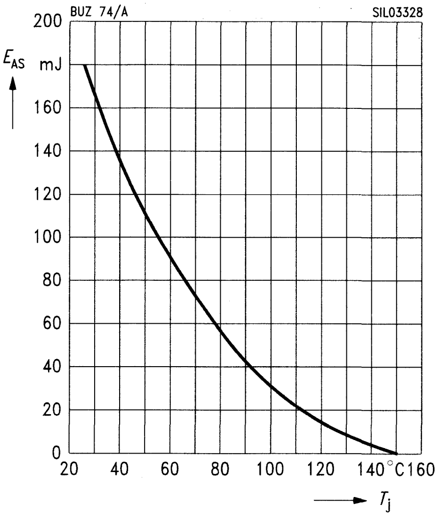
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs



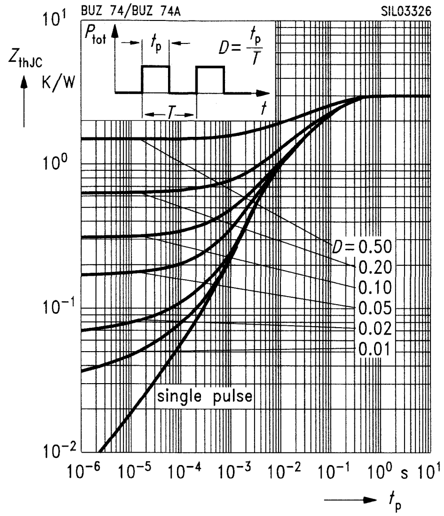
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 2.4$ A, $V_{DD} = 50$ V
$R_{GS} = 25\ \Omega$, $L = 56.3$ mH



Transient thermal impedance

$Z_{\mathrm{th\,JC}} = f(t_p)$

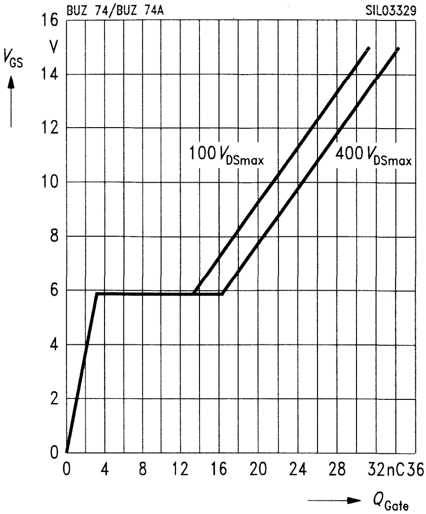
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{\mathrm{Gate}})$

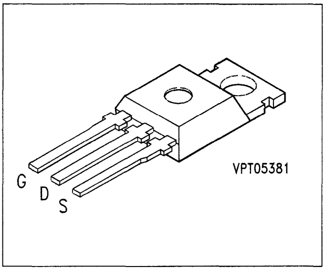
parameter: $I_{\mathrm{D\,puls}} = 4.8$ A



SIPMOS® Power Transistors

BUZ 76
BUZ 76 A

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	T_C	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 76	400 V	3.0 A	37 ˚C	1.8 Ω	TO-220 AB	C67078-S1315-A2
BUZ 76 A	400 V	2.7 A	23 ˚C	2.5 Ω	TO-220 AB	C67078-S1315-A3

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		76	76 A	
Continuous drain current	I_D	**3.0**	**2.7**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**12**	**11**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**3**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**5**		mJ
Avalanche energy, single pulse I_D = 3 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 35 mH, T_j = 25 ˚C	E_{AS}	**180**		
Gate-source voltage	V_{GS}	**± 20**		V
Power dissipation, T_C = 25 ˚C	P_{tot}	**40**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	400	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 400 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS(on)}$				Ω
V_{GS} = 10 V, I_D = 2.0 A BUZ 76		–	1.4	1.8	
BUZ 76 A		–	2.0	2.5	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 2.0 A	g_{fs}	2.1	3.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	430	650	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	65	100	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	25	40	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	8	12	ns
	t_r	–	30	45	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	55	75	
	t_f	–	30	40	

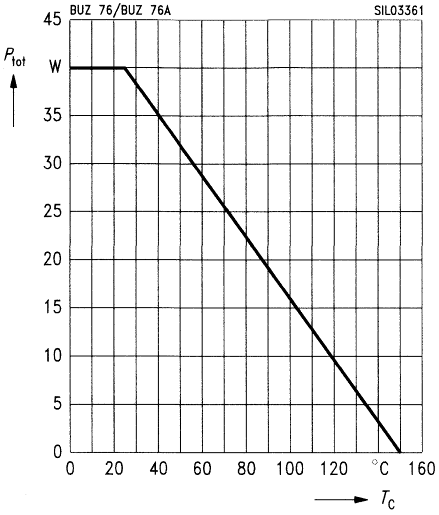
Electrical Characteristics (cont'd)

at T_j = 25 °C, unless otherwise specified.

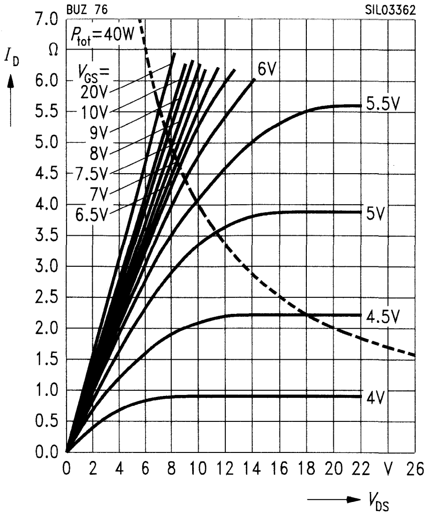
Parameter		**Symbol**	**Values**			**Unit**
			min.	**typ.**	**max.**	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 °C	BUZ 76		–	–	3.0	
	BUZ 76 A		–	–	2.7	
Pulsed reverse drain current		I_{SM}				
T_C = 25 °C	BUZ 76		–	–	12	
	BUZ 76 A		–	–	11	
Diode forward on-voltage I_S = 6.0 A, V_{GS} = 0 V		V_{SD}	–	1.0	1.4	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		t_{rr}	–	300	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		Q_{rr}	–	2.5	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

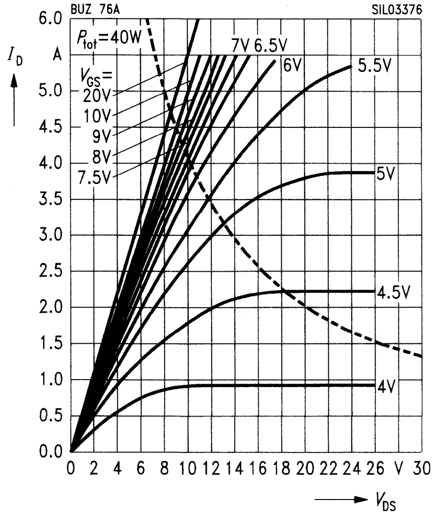
Total power dissipation
$P_{tot} = f(T_C)$



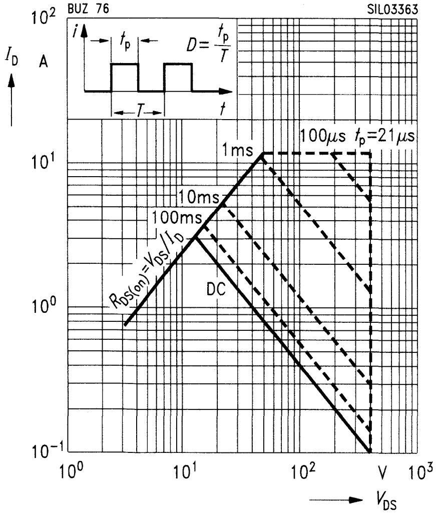
Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 76**
parameter: $t_p = 80$ µs



Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 76 A**
parameter: $t_p = 80$ µs



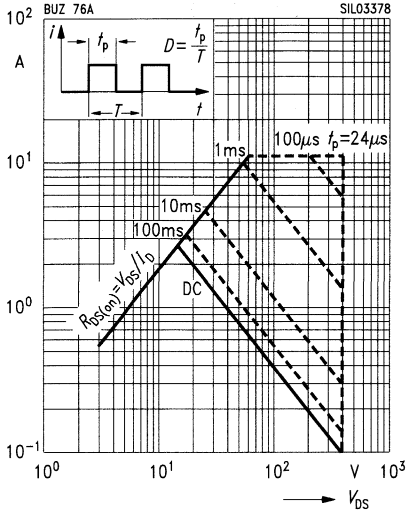
Safe operating area
$I_D = f(V_{DS})$ **BUZ 76**
parameter: $D = 0.01$, $T_C = 25$ °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 76 A**

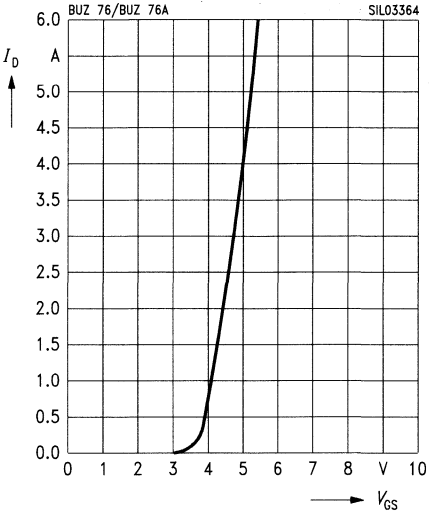
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

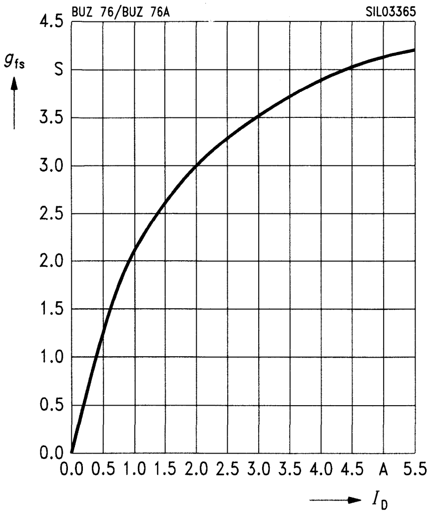
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



Typ.forward transconductance

$g_{fs} = f(I_D)$

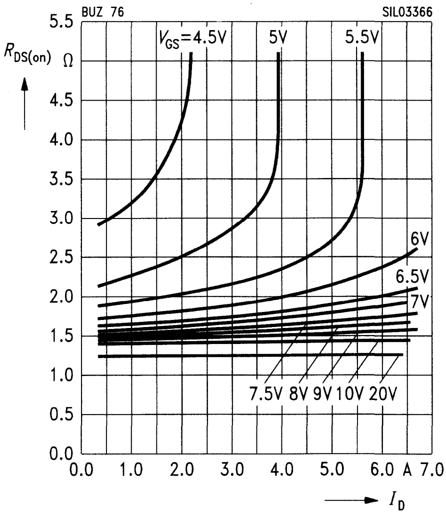
parameter: $t_p = 80$ µs



Typ. drain-source on-resistance

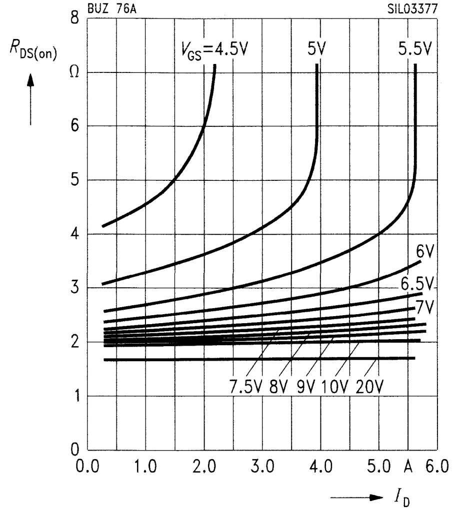
$R_{DS\,(on)} = f(I_D)$ **BUZ 76**

parameter: V_{GS}



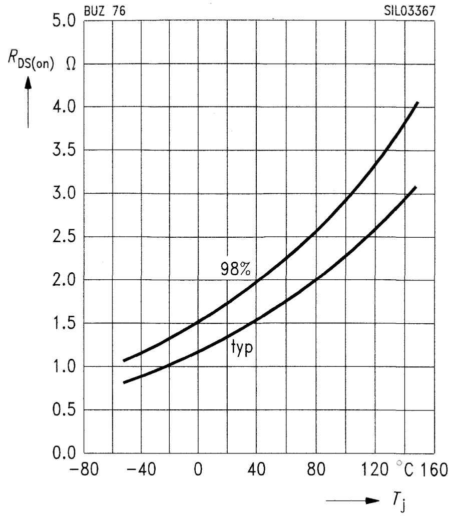
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 76 A**
parameter: V_{GS}



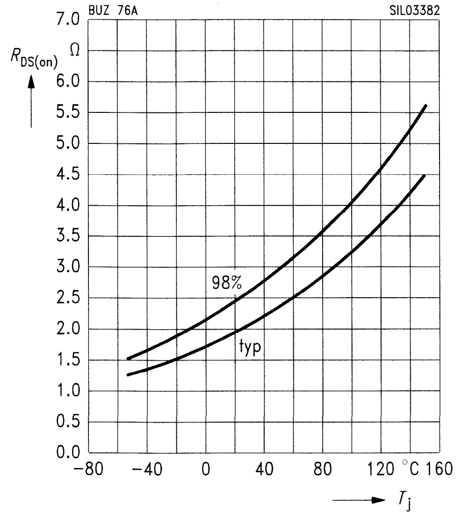
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 76**
parameter: I_D = 2 A, V_{GS} = 10 V, (spread)



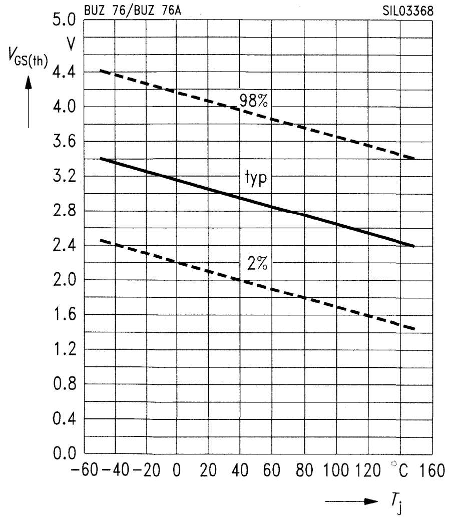
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 76 A**
parameter: I_D = 2 A, V_{GS} = 10 V, (spread)



Gate threshold voltage

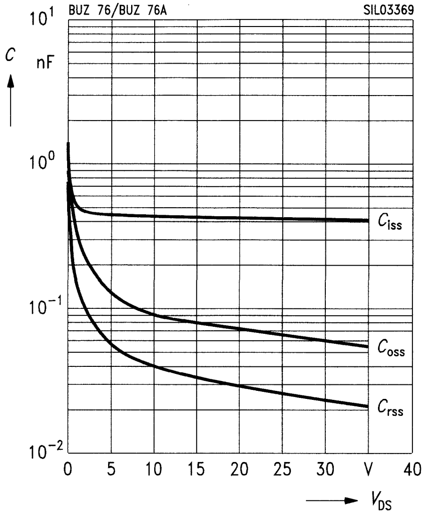
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

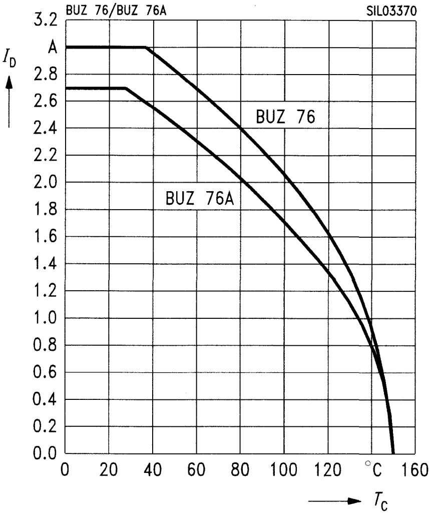
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

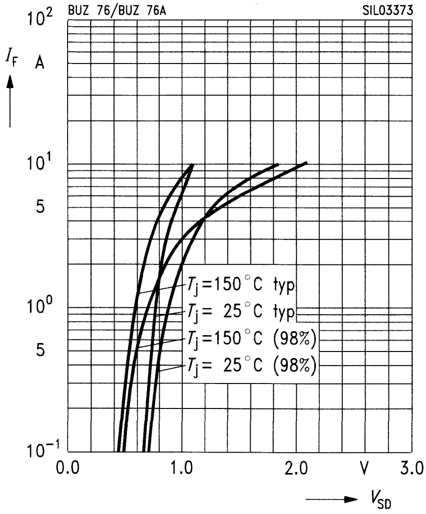
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

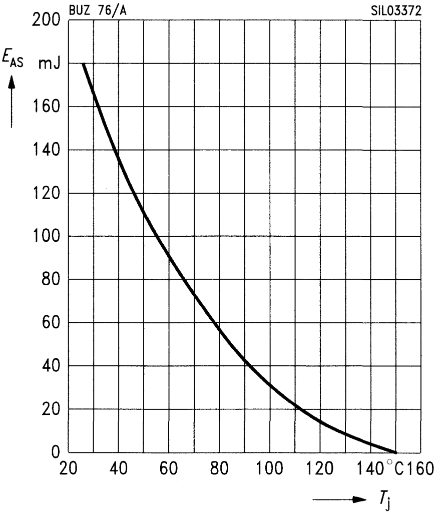
parameter: T_j, $t_p = 80$ µs



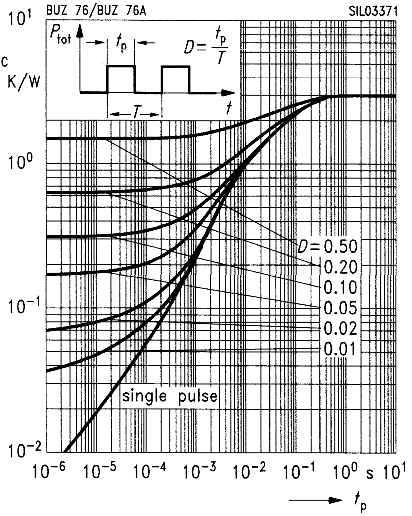
Avalanche energy $E_{AS} = f(T_j)$

parameter: $I_D = 3$ A, $V_{DD} = 50$ V

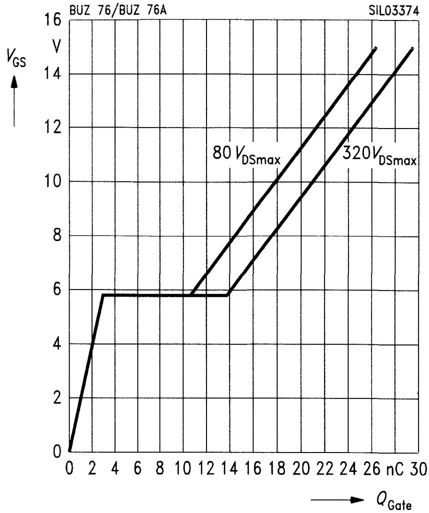
$R_{GS} = 25\ \Omega$, $L = 35$ mH



Transient thermal impedance
$Z_{th\,JC} = f\,(t_p)$
parameter: $D = t_p / T$



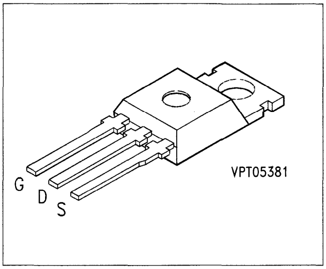
Typ. gate charge
$V_{GS} = f\,(Q_{Gate})$
parameter: $I_{D\,puls}$ = 6 A



SIPMOS® Power Transistors

BUZ 77 A
BUZ 77 B

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	T_C	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 77 A	600 V	2.7 A	31 °C	4.0 Ω	TO-220 AB	C67078-S1320-A3
BUZ 77 B	600 V	2.9 A	29 °C	3.5 Ω	TO-220 AB	C67078-S1320-A5

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		77 A	**77 B**	
Continuous drain current	I_D	**2.7**	**2.9**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**11**	**11.5**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**2.7**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**5.0**		mJ
Avalanche energy, single pulse I_D = 2.7 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 45.3 mH, T_j = 25 °C	E_{AS}	**180**		
Gate-source voltage	V_{GS}	**± 20**		V
Power dissipation, T_C = 25 °C	P_{tot}	**75**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	**typ.**	**max.**	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	600	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 600 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 1.7 A	$R_{DS(on)}$				Ω
BUZ 77 A		–	3.5	4.0	
BUZ 77 B		–	3.0	3.5	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 1.7 A	g_{fs}	1.5	3.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	460	690	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	55	85	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	20	30	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	8	12	ns
	t_r	–	30	40	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	50	65	
	t_f	–	30	40	

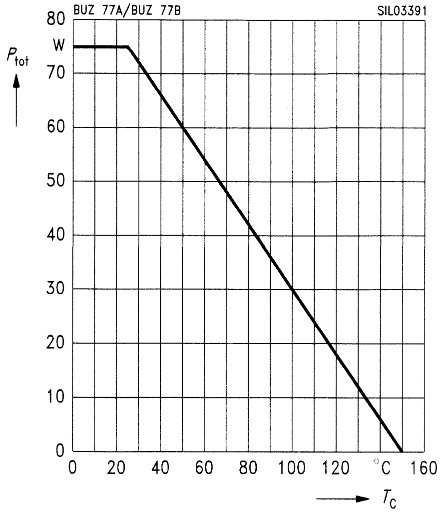
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	2.7	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	11.0	
Diode forward on-voltage I_S = 5.4 A, V_{GS} = 0 V	V_{SD}	–	0.95	1.3	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	350	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	3.5	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Total power dissipation

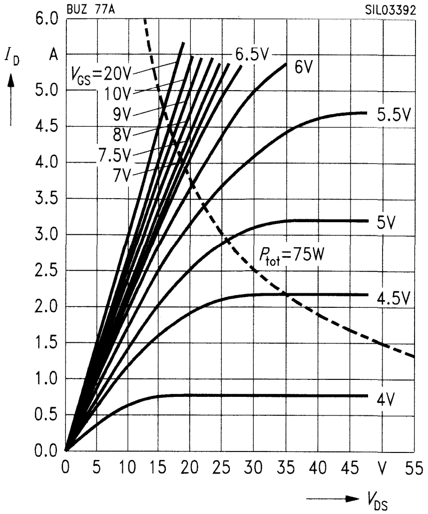
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 77 A**

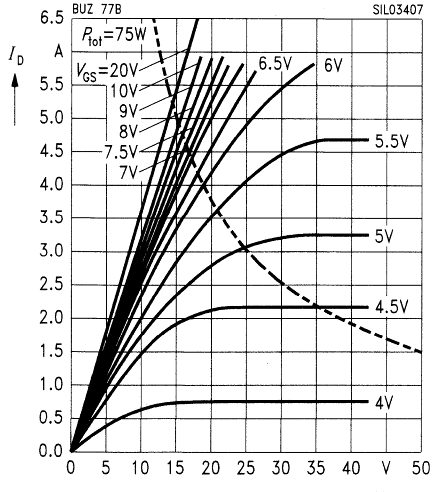
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 77 B**

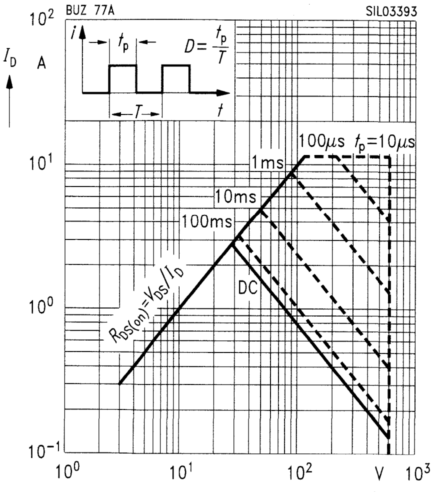
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$ **BUZ 77 A**

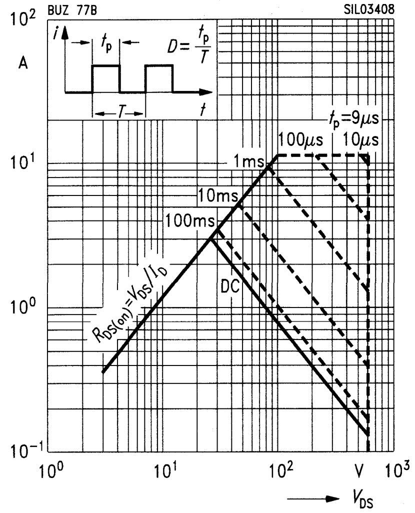
parameter: D = 0.01, T_C = 25 °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 77 B**

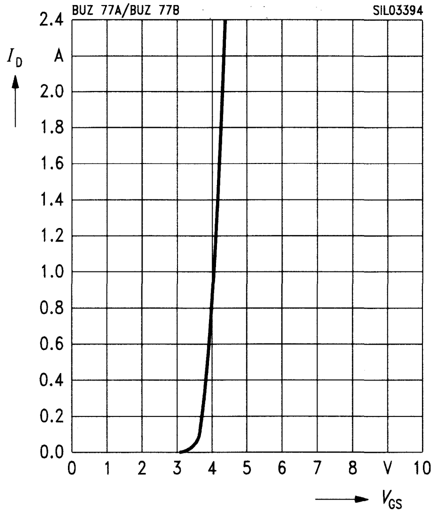
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

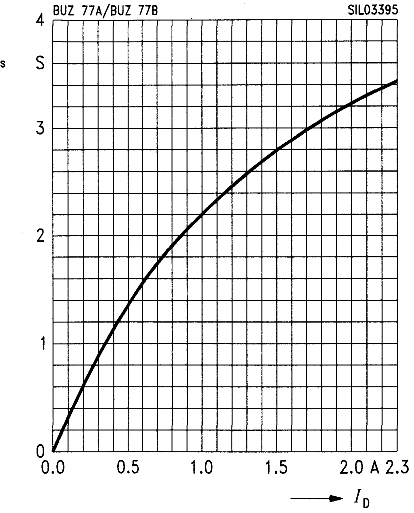
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



Typ.forward transconductance

$g_{fs} = f(I_D)$

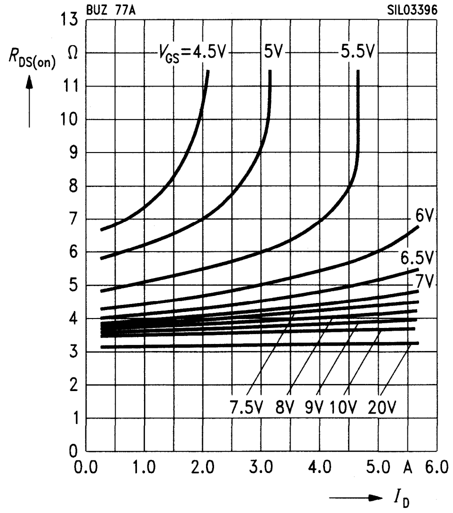
parameter: $t_p = 80$ µs



Typ. drain-source on-resistance

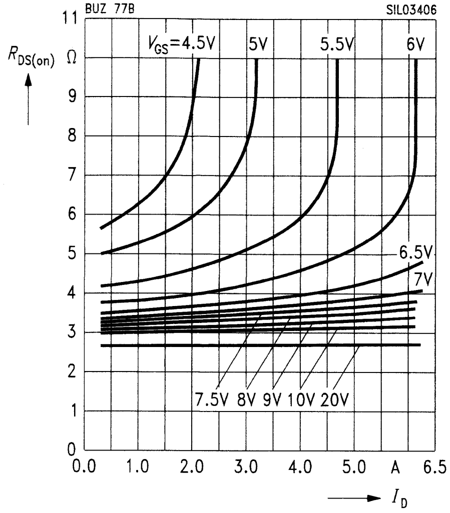
$R_{DS\,(on)} = f(I_D)$ **BUZ 77 A**

parameter: V_{GS}



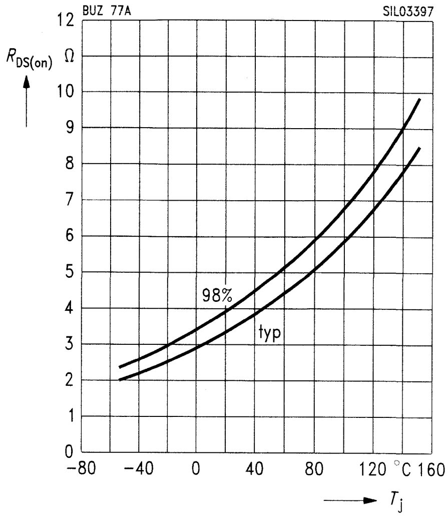
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 77 B**
parameter: V_{GS}



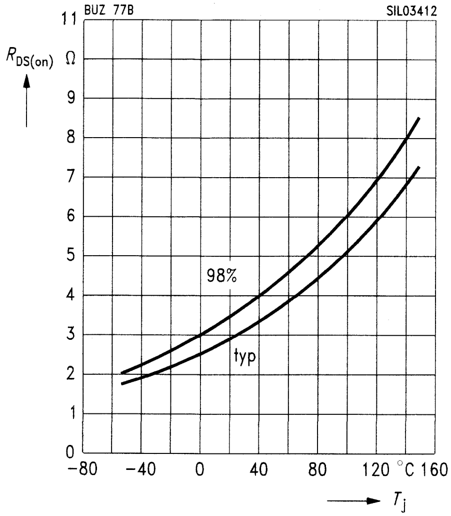
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 77 A**
parameter: I_D = 1.7 A, V_{GS} = 10 V, (spread)



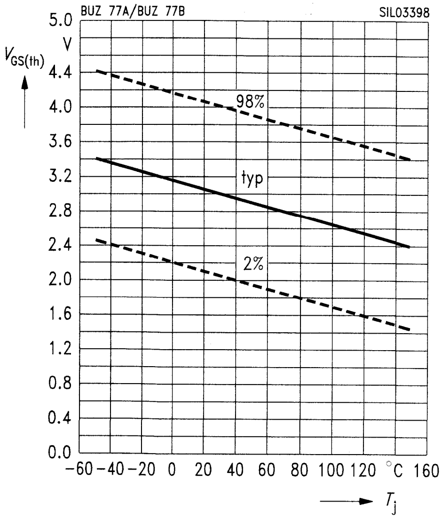
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 77 B**
parameter: I_D = 1.7 A, V_{GS} = 10 V, (spread)



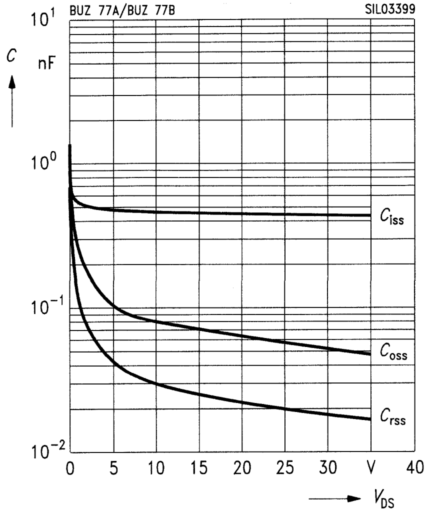
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



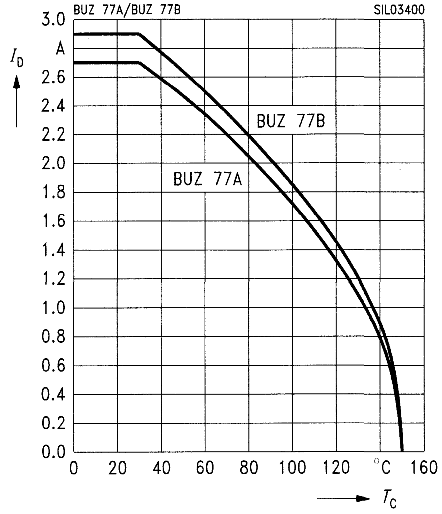
Typ. capacitances

$C = f\,(V_{DS})$
parameter: V_{GS} = 0 V, f = 1 MHz



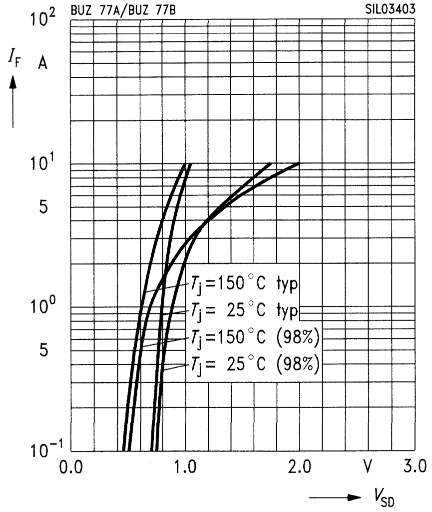
Drain current

$I_D = f\,(T_C)$
parameter: $V_{GS} \geq$ 10 V



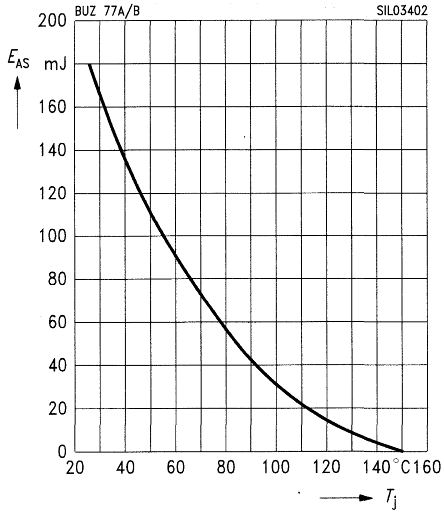
Forward characteristics of reverse diode

$I_F = f\,(V_{SD})$
parameter: t_p = 80 µs, T_j

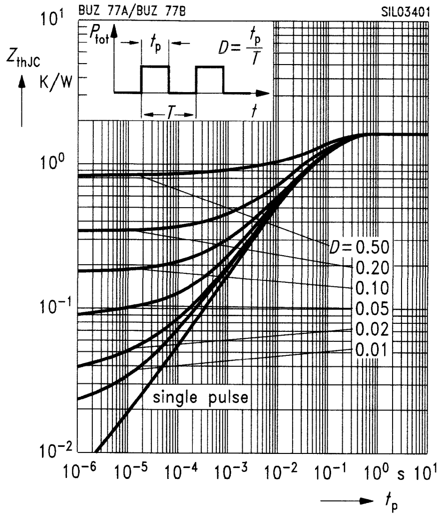


Avalanche energy $E_{AS} = f\,(T_j)$

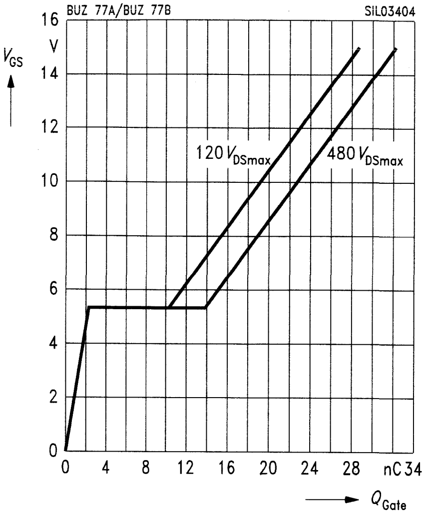
parameter: I_D = 2.7 A, V_{DD} = 50 V
R_{GS} = 25 Ω, L = 45.3 mH



Transient thermal impedance
$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$



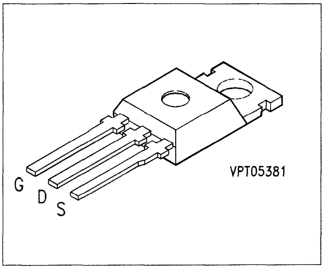
Typ. gate charge
$V_{\text{GS}} = f(Q_{\text{Gate}})$
parameter: $I_{\text{D puls}} = 4.4$ A



SIEMENS

SIPMOS® Power Transistor **BUZ 78**

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 78	800 V	1.5 A	8.0 Ω	TO-220 AB	C67078-S1318-A2

Maximum Ratings

Parameter	Symbol	Value	Unit
Continuous drain current, T_C = 25 ˚C	I_D	**1.5**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**6.0**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**1.5**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**5.0**	mJ
Avalanche energy, single pulse I_D = 1.5 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 142 mH, T_j = 25 ˚C	E_{AS}	**170**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 ˚C	P_{tot}	**40**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	800	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 800 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 1.0 A	$R_{DS\,(on)}$	–	6.5	8.0	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 1.0 A	g_{fs}	1.0	1.35	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	320	430	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	40	60	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	20	30	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 1.7 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	8	12	ns
	t_r	–	40	60	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 1.7 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	45	60	
	t_f	–	25	35	

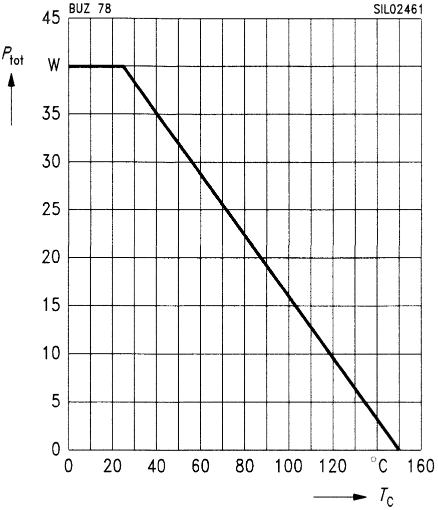
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	1.5	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	6.0	
Diode forward on-voltage I_S = 3.0 A, V_{GS} = 0 V	V_{SD}	–	0.95	1.45	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	370	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	2.10	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Total power dissipation

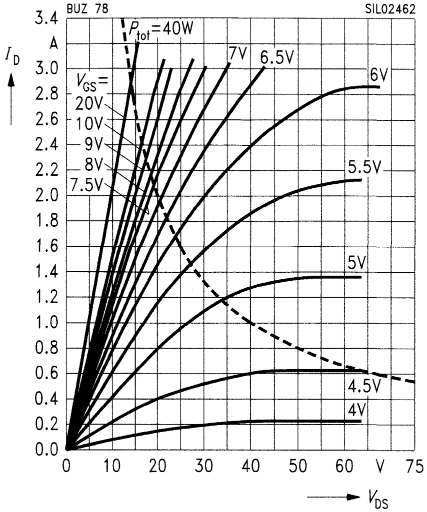
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

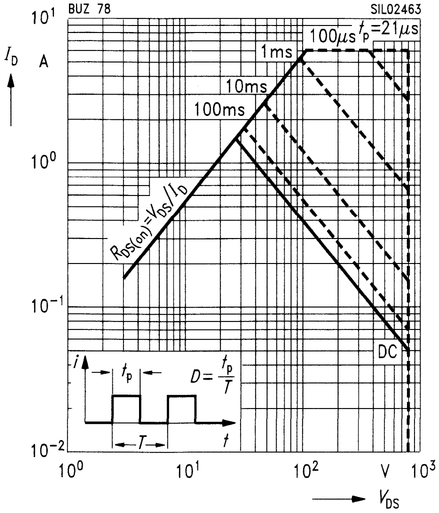
parameter: $t_p = 80$ µs



Safe operating area

$I_D = f(V_{DS})$

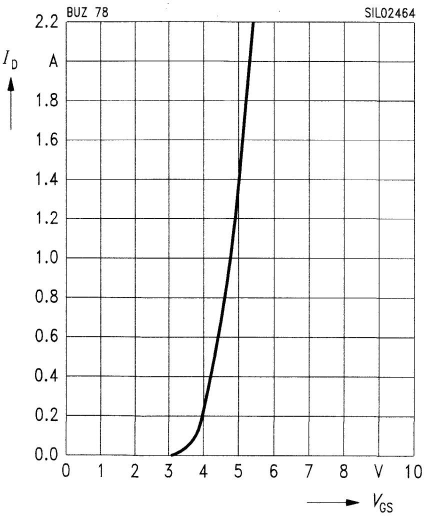
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

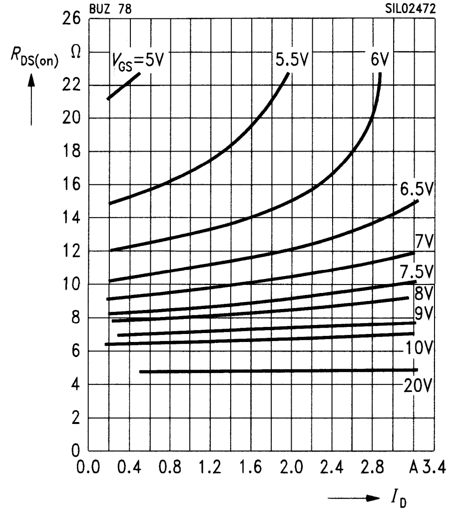
$I_D = f(V_{GS})$

parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



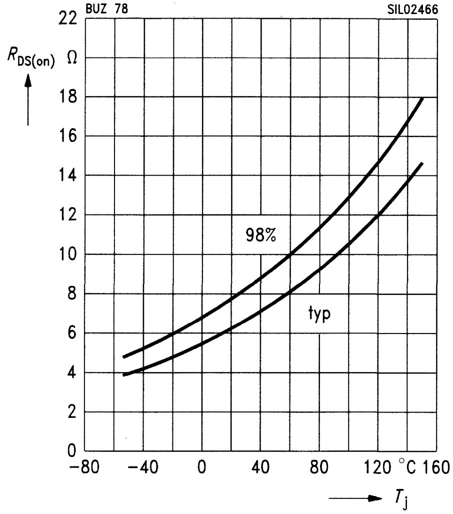
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



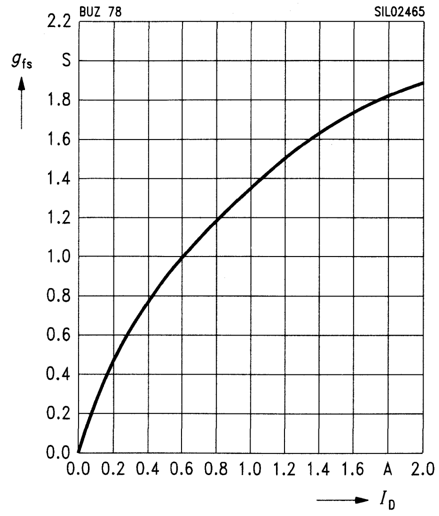
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 1.0 A, V_{GS} = 10 V, (spread)



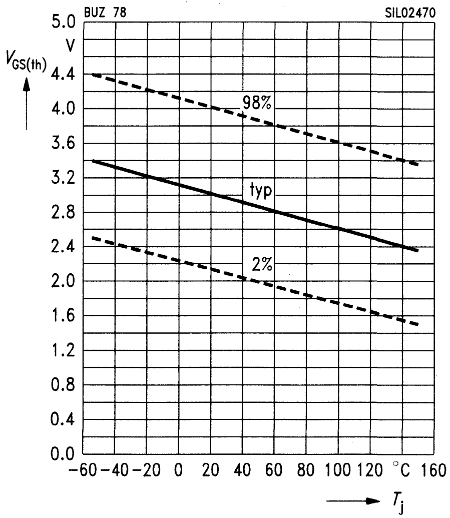
Typ.forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

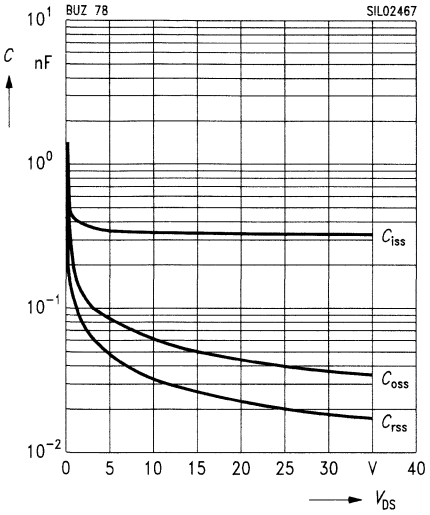
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

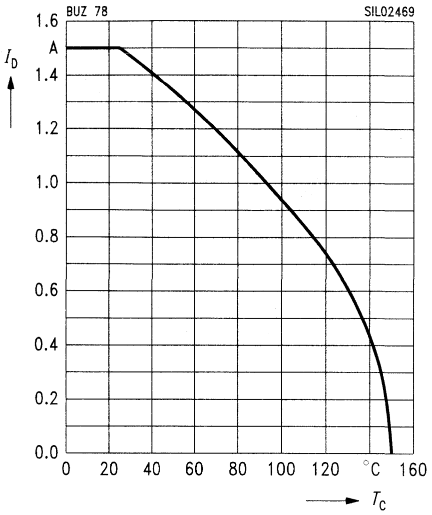
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

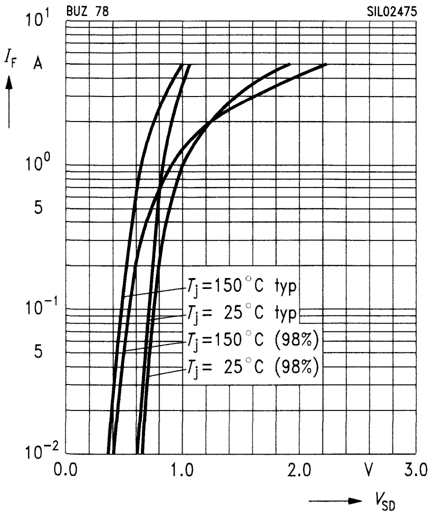
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

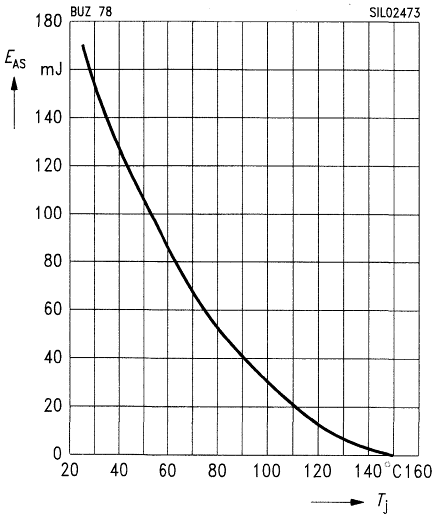
parameter: T_j, $t_p = 80$ µs



Avalanche energy $E_{AS} = f(T_j)$

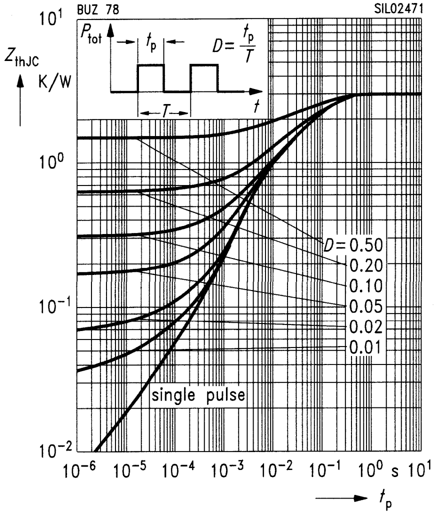
parameter: $I_D = 1.5$ A, $V_{DD} = 50$ V

$R_{GS} = 25\ \Omega$, $L = 142$ mH



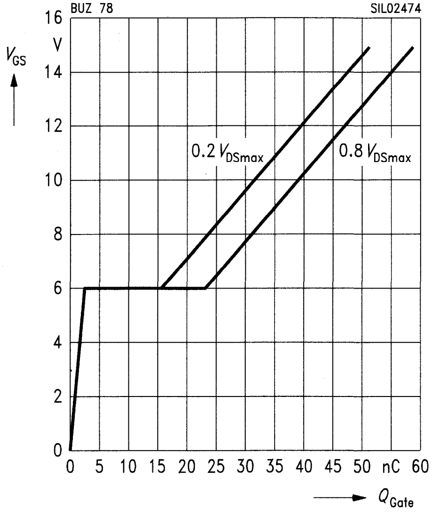
Transient thermal impedance

$Z_{th\,JC} = f\,(t_p)$
parameter: $D = t_p\,/\,T$



Typ. gate charge

$V_{GS} = f\,(Q_{Gate})$
parameter: $I_{D\,puls}$ = 2.85 A

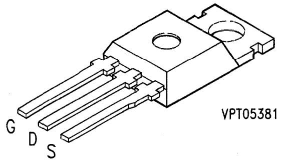


SIEMENS

SIPMOS® Power Transistors

BUZ 80
BUZ 80 A

- N channel
- Enhancement mode



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 80	800 V	2.6 A	4.0 Ω	TO-220 AB	C67078-A1309-A2
BUZ 80 A	800 V	3.0 A	3.0 Ω	TO-220 AB	C67078-A1309-A3

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		80	80 A	
Continuous drain current, T_C = 50 °C	I_D	**2.6**	**3.0**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**10**	**12**	
Drain-source voltage	V_{DS}	**800**		V
Drain-gate voltage, R_{GS} = 20 kΩ	V_{DGR}	**800**		
Gate-source voltage	V_{GS}	**± 20**		
Power dissipation, T_C = 25 °C	P_{tot}	**75**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Static characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	800	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 800 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	20	250	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS\,(on)}$				Ω
V_{GS} = 10 V, I_D = 1.5 A BUZ 80		–	3.5	4.0	
BUZ 80 A		–	2.7	3.0	

Dynamic characteristics

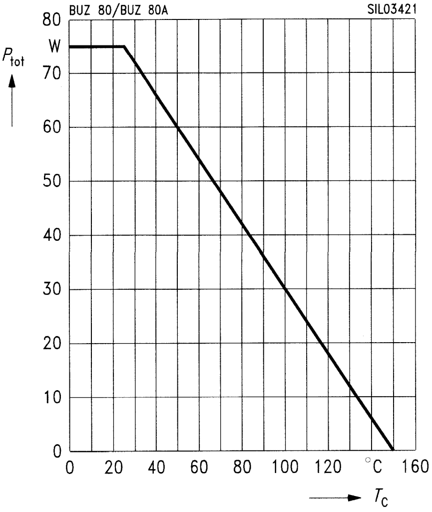
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$ I_D = 1.5 A	g_{fs}	1.0	1.8	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1600	2100	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	90	150	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	30	55	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	30	45	ns
	t_r	–	40	60	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	110	140	
	t_f	–	60	80	

Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

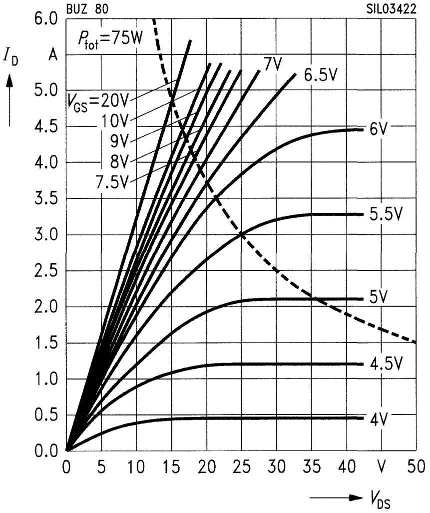
Parameter		Symbol	Values			Unit
			min.	typ.	max.	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 °C	BUZ 80		–	–	2.6	
	BUZ 80 A		–	–	3.0	
Pulsed reverse drain current		I_{SM}				
T_C = 25 °C	BUZ 80		–	–	10	
	BUZ80 A		–	–	12	
Diode forward on-voltage I_S = 6.0 A, V_{GS} = 0 V		V_{SD}	–	1.05	1.3	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		t_{rr}	–	1.8	–	µs
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		Q_{rr}	–	12	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

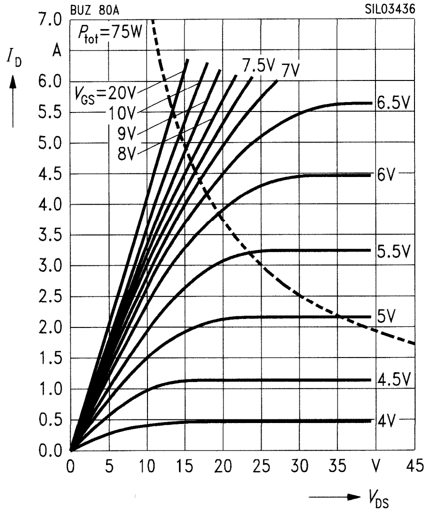
Total power dissipation
$P_{tot} = f(T_C)$



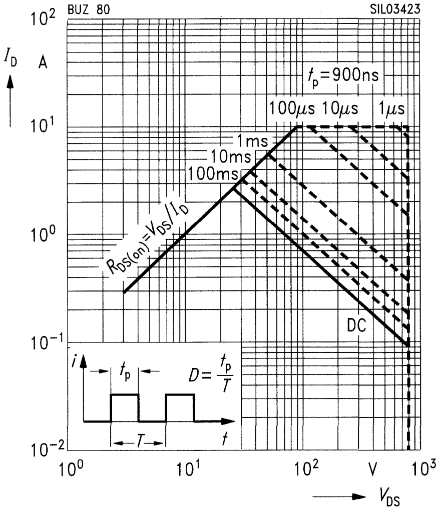
Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 80**
parameter: t_p = 80 µs



Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 80 A**
parameter: t_p = 80 µs

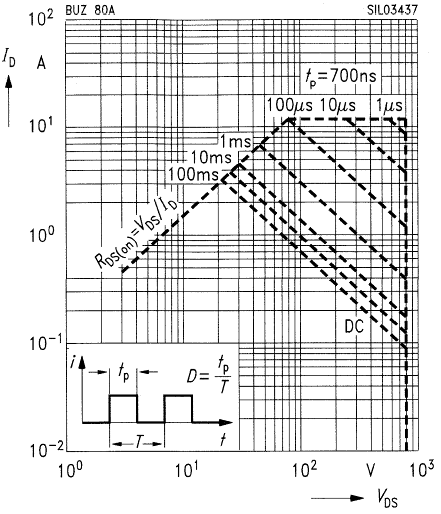


Safe operating area
$I_D = f(V_{DS})$ **BUZ 80**
parameter: D = 0.01, T_C = 25 °C



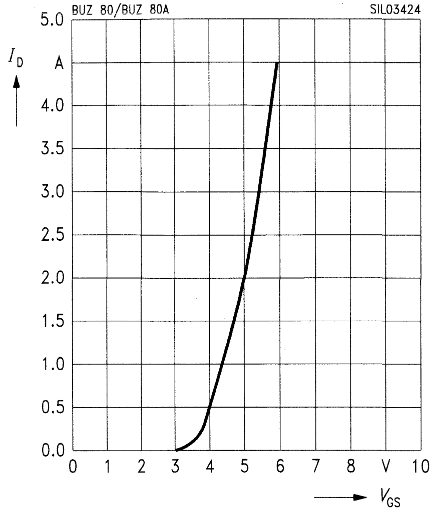
Safe operating area

$I_D = f(V_{DS})$ **BUZ 80 A**
parameter: $D = 0.01$, $T_C = 25\ ^\circ C$



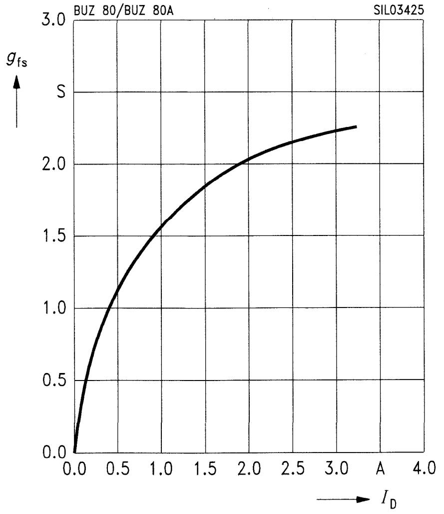
Typ. transfer characteristics

$I_D = f(V_{GS})$
parameter: $t_p = 80\ \mu s$, $V_{DS} = 25$ V



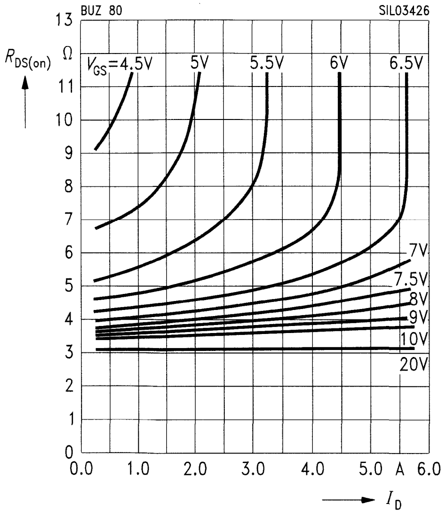
Typ.forward transconductance

$g_{fs} = f(I_D)$
parameter: $t_p = 80\ \mu s$



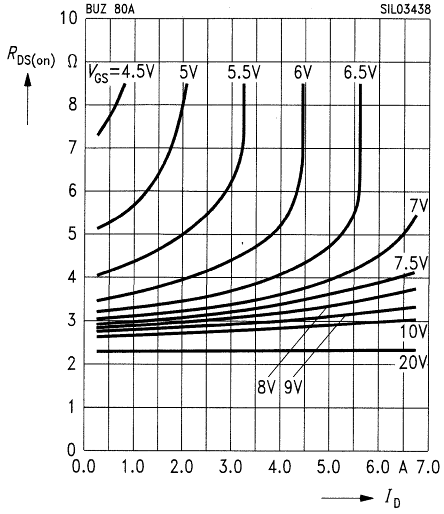
Typ. drain-source on-resistance

$R_{DS\ (on)} = f(I_D)$ **BUZ 80**
parameter: V_{GS}



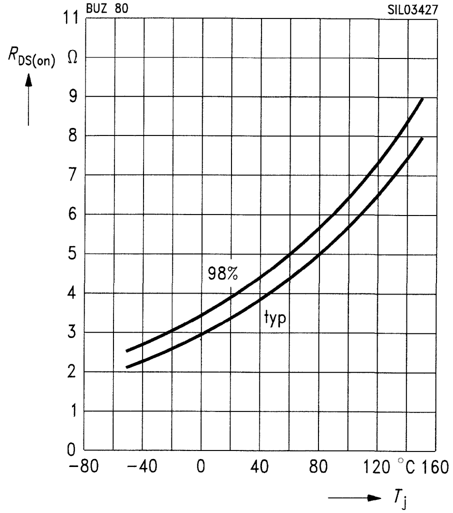
Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$ **BUZ 80 A**
parameter: V_{GS}



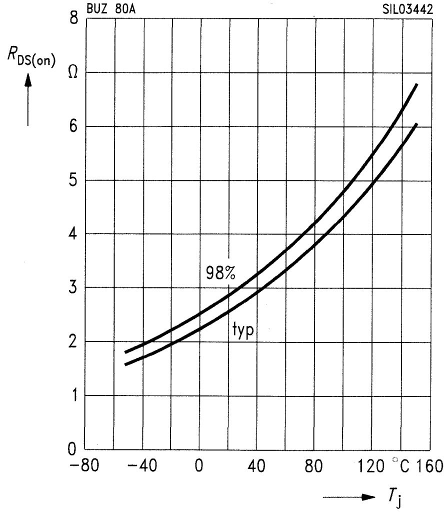
Drain-source on-resistance

$R_{DS\,(on)} = f(T_j)$ **BUZ 80**
parameter: I_D = 1.7 A, V_{GS} = 10 V, (spread)



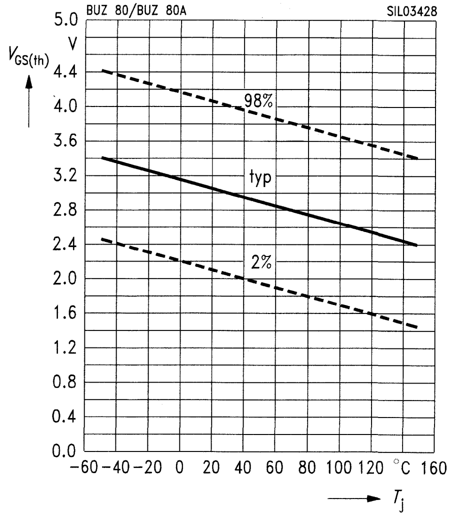
Drain-source on-resistance

$R_{DS\,(on)} = f(T_j)$ **BUZ 80 A**
parameter: I_D = 1.7 A, V_{GS} = 10 V, (spread)



Gate threshold voltage

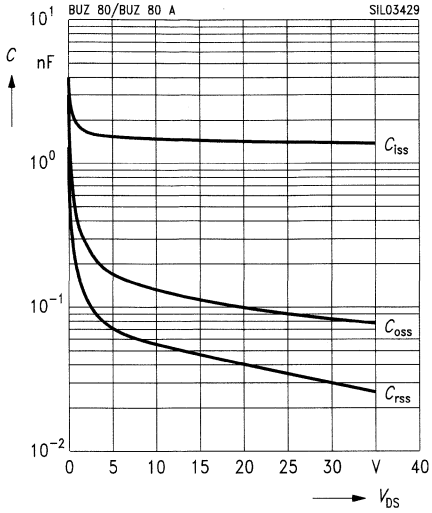
$V_{GS\,(th)} = f(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

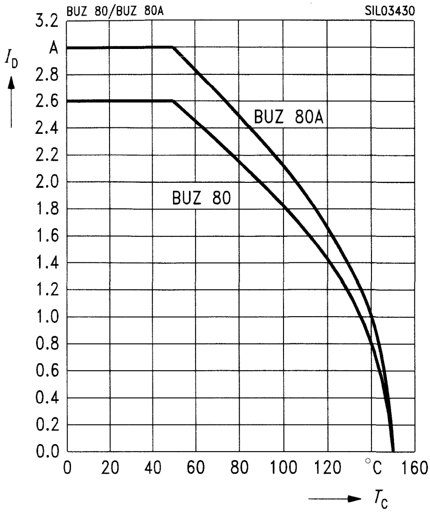
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

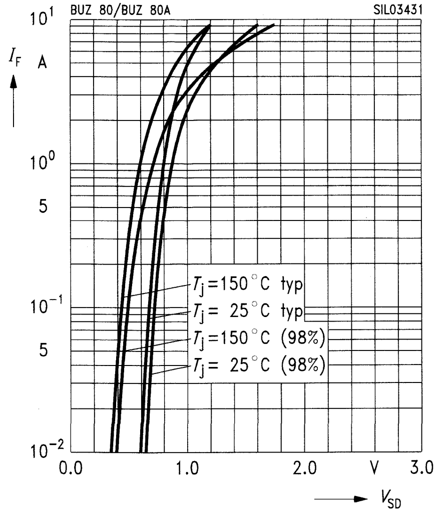
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

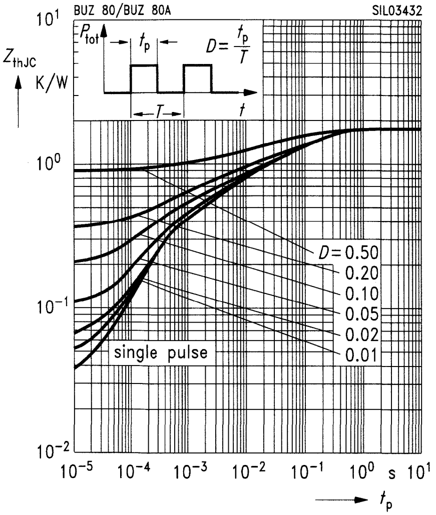
parameter: $t_p = 80$ µs, T_j



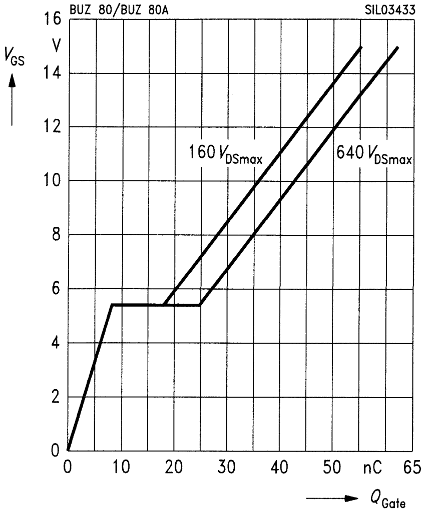
Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

parameter: $D = t_p / T$



Typ. gate charge
$V_{GS} = f\,(Q_{Gate})$
parameter: $I_{D\ puls} = 5$ A

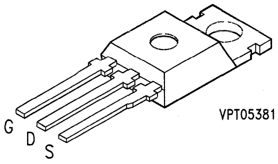


SIEMENS

SIPMOS® Power Transistor

BUZ 81

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 81	800 V	4.0 A	2.5 Ω	TO-220 AB	C67078-S1345-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 48 °C	I_D	**4.0**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**16**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**4.0**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**13**	mJ
Avalanche energy, single pulse I_D = 4.0 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 48 mH, T_j = 25 °C	E_{AS}	**410**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

Static characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	800	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 800 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 ˚C		–	0.1	1.0	
T_j = 125 ˚C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 2.8 A	$R_{DS\,(on)}$	–	2.0	2.5	Ω

Dynamic characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 2.8 A	g_{fs}	1.0	4.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	900	1350	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	95	140	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	50	75	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.1 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	15	25	ns
	t_r	–	65	85	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.1 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	200	270	
	t_f	–	65	85	

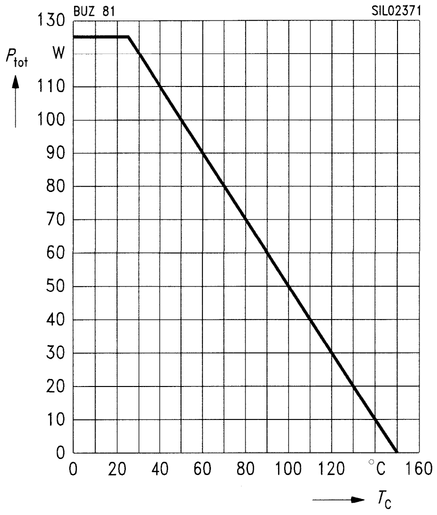
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	4.0	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	16	
Diode forward on-voltage I_S = 8 A, V_{GS} = 0 V	V_{SD}	–	1.0	1.4	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	0.3	–	µs
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	2.5	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

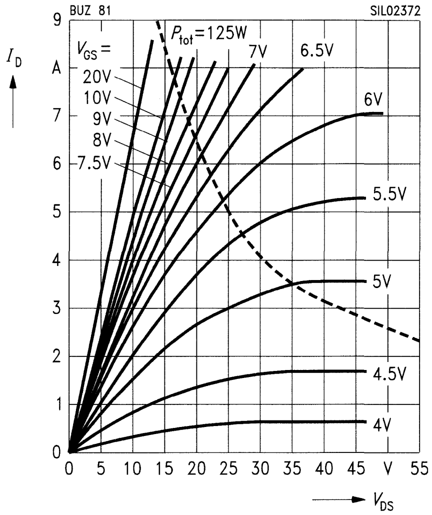
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

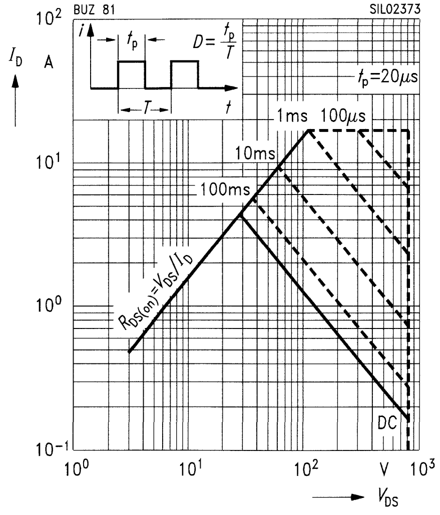
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

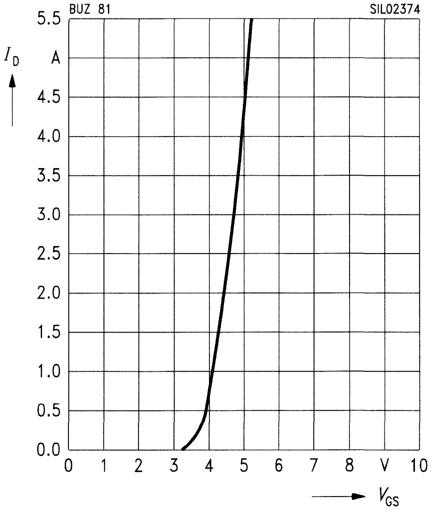
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

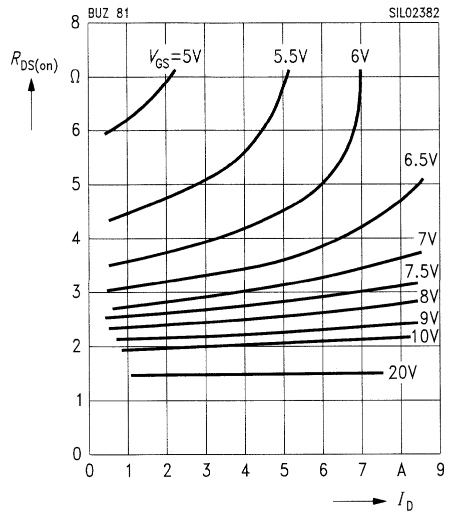
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



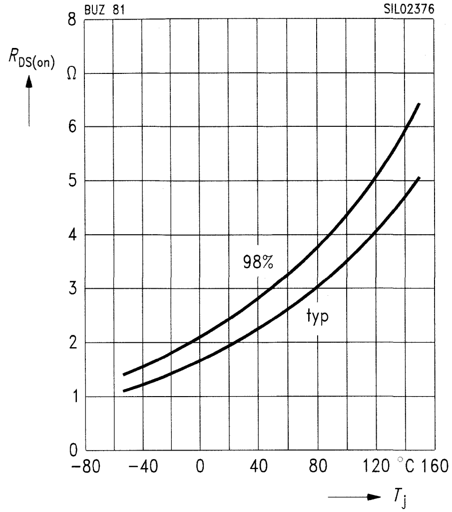
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



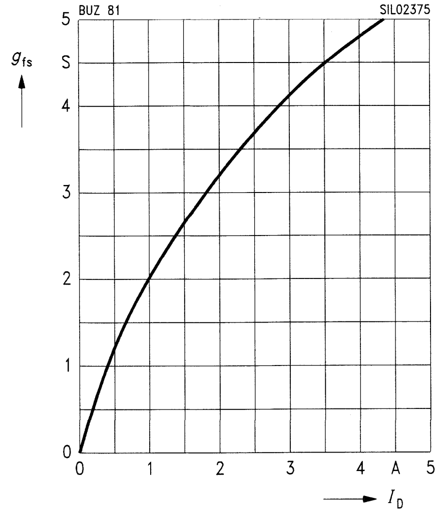
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 2.8 A, V_{GS} = 10 V, (spread)



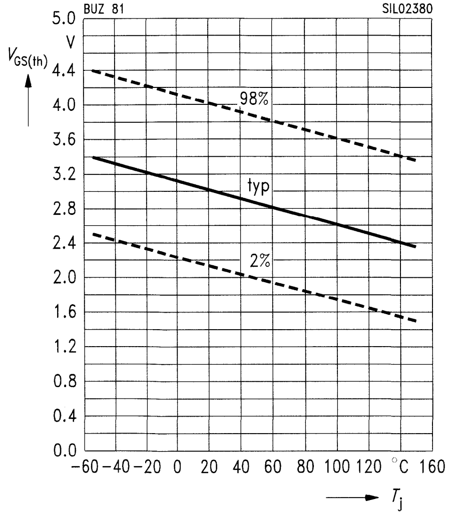
Typ.forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs

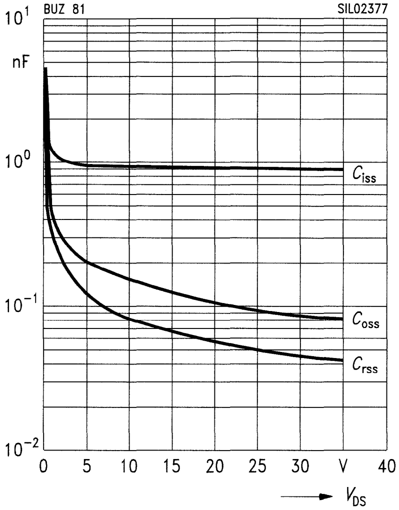


Gate threshold voltage

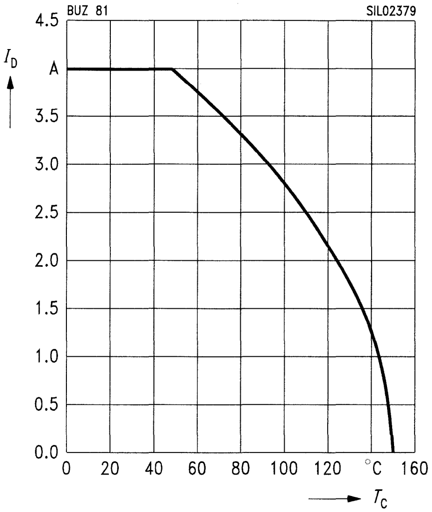
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



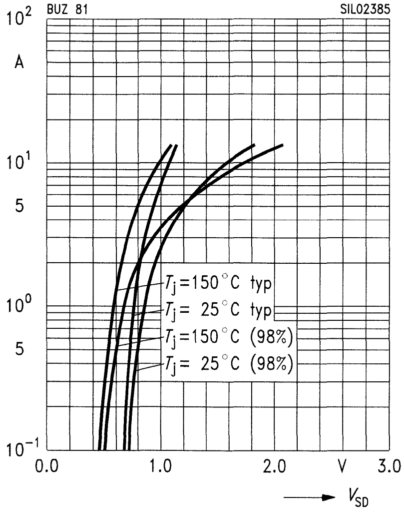
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



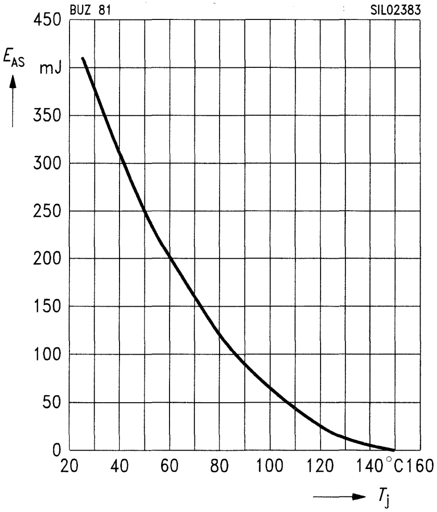
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j , $t_p = 80$ µs

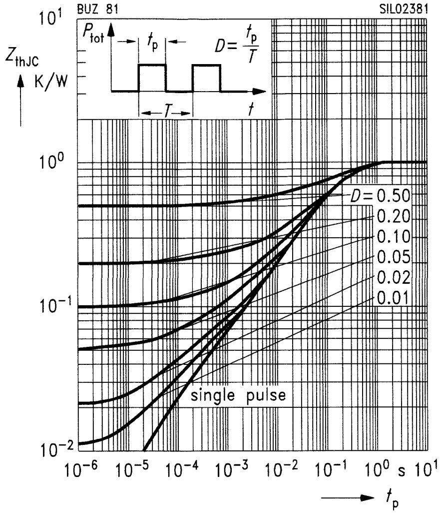


Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 4$ A, $V_{DD} = 50$ V
$R_{GS} = 25\ \Omega$, $L = 48$ mH



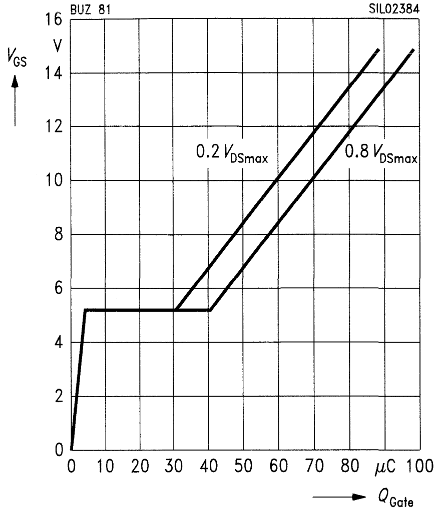
Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

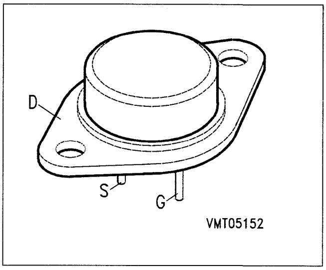
$V_{GS} = f(Q_{\text{Gate}})$
parameter: $I_{\text{D puls}} = 5.25$ A



SIPMOS® Power Transistors

BUZ 84
BUZ 84 A

- N channel
- Enhancement mode



Type	V_{DS}	I_D	T_C	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 84	800 V	5.3 A	25 ˚C	2.0 Ω	TO-204 AA	C67078-A1013-A2
BUZ 84 A	800 V	6.0 A	29 ˚C	1.5 Ω	TO-204 AA	C67078-A1013-A3

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		84	84 A	
Continuous drain current	I_D	**5.3**	**6.0**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**21**	**24**	
Drain source voltage	V_{DS}	**800**		V
Drain-gate voltage, R_{GS} = 20 kΩ	V_{DGR}	**800**		
Gate-source voltage	V_{GS}	**± 20**		
Power dissipation, T_C = 25 ˚C	P_{tot}	**125**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**C**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

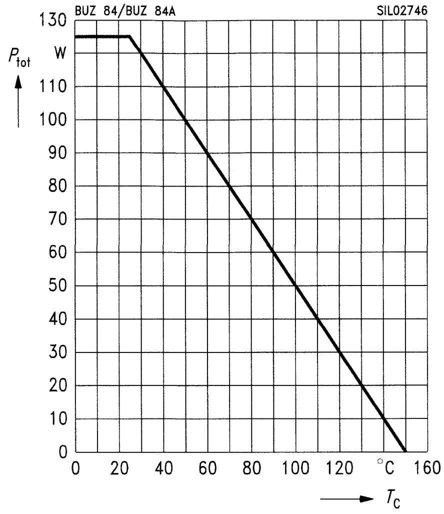
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	800	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 800 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	20	250	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS\,(on)}$				Ω
V_{GS} = 10 V, I_D = 3.0 A BUZ 84		–	1.6	2.0	
BUZ 84 A		–	1.3	1.5	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 3.0 A	g_{fs}	1.8	3.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	3.9	5.0	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	200	350	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	80	140	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	60	90	ns
	t_r	–	90	140	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	330	430	
	t_f	–	110	140	

Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

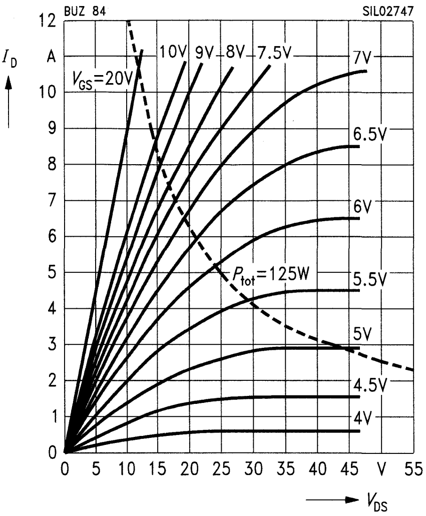
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current	I_S				A
T_C = 25 °C BUZ 84		–	–	5.3	
BUZ 84 A		–	–	6.0	
Pulsed reverse drain current	I_{SM}				
T_C = 25 °C BUZ 84		–	–	21	
BUZ 84 A		–	–	24	
Diode forward on-voltage I_S = 12 A, V_{GS} = 0 V	V_{SD}	–	1.1	1.5	V
Reverse recovery time V_R = 100 V, I_F = I_S, di_F / dt = 100 A/µs	t_{rr}	–	1.8	–	µs
Reverse recovery charge V_R = 100 V, I_F = I_S, di_F / dt = 100 A/µs	Q_{rr}	–	25	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

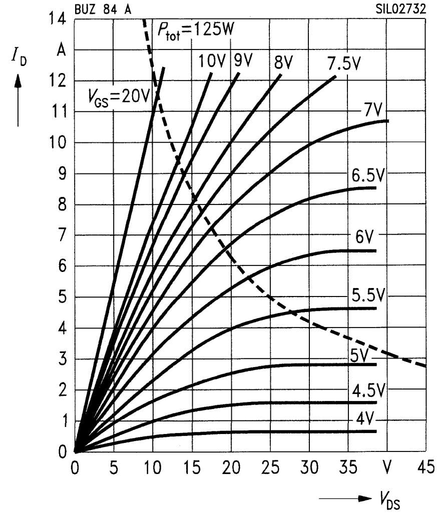
Total power dissipation
$P_{tot} = f(T_C)$



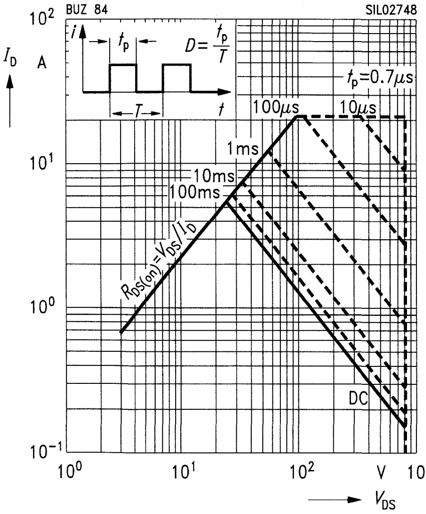
Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 84**
parameter: t_p = 80 µs



Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 84 A**
parameter: t_p = 80 µs



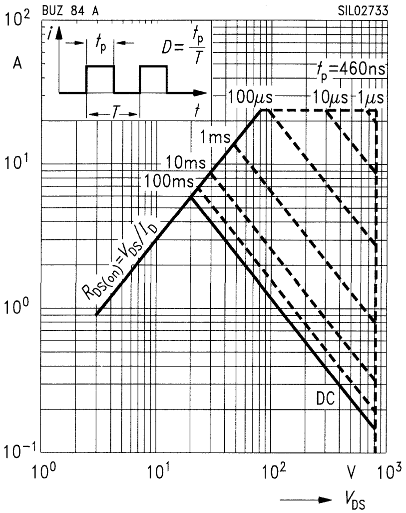
Safe operating area
$I_D = f(V_{DS})$ **BUZ 84**
parameter: D = 0.01, T_C = 25 °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 84 A**

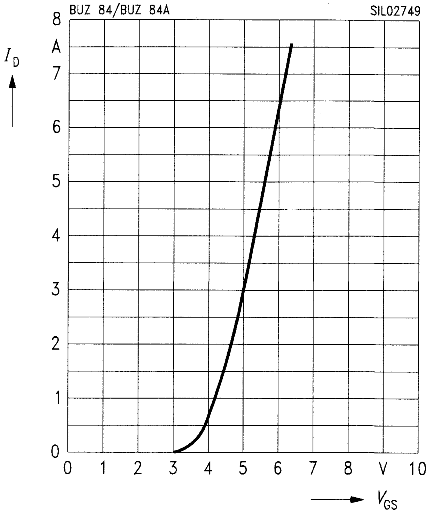
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

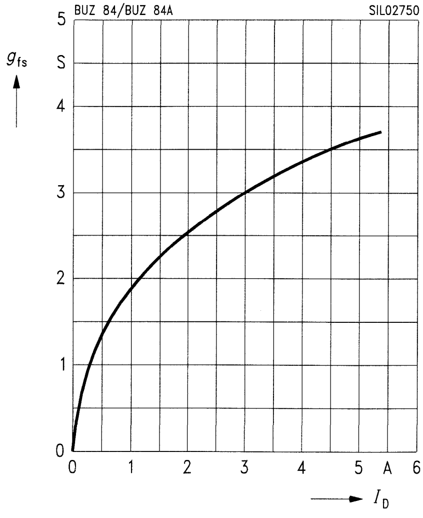
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



Typ. forward transconductance

$g_{fs} = f(I_D)$

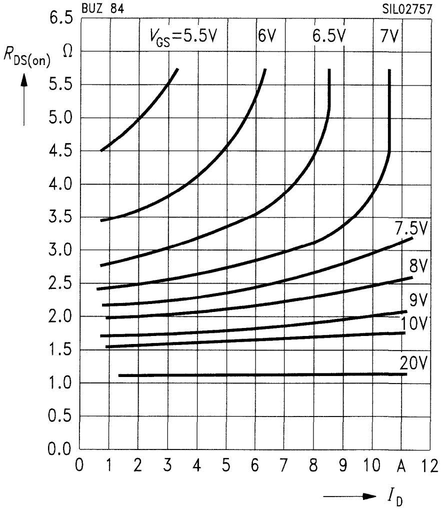
parameter: $t_p = 80$ µs



Typ. drain-source on-resistance

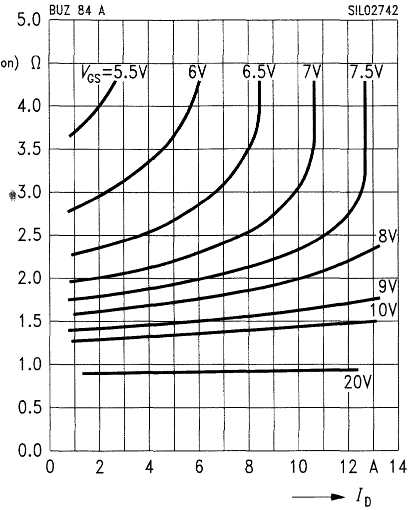
$R_{DS\,(on)} = f(I_D)$ **BUZ 84**

parameter: V_{GS}



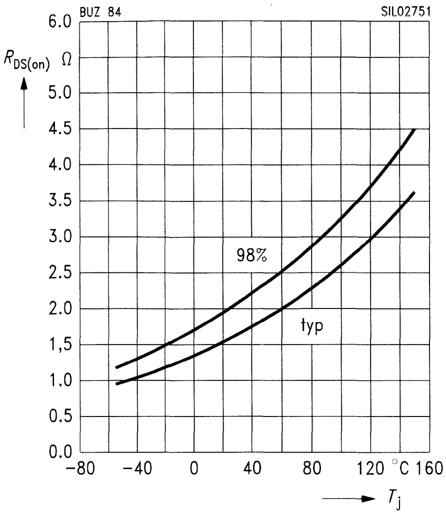
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 84 A**
parameter: V_{GS}



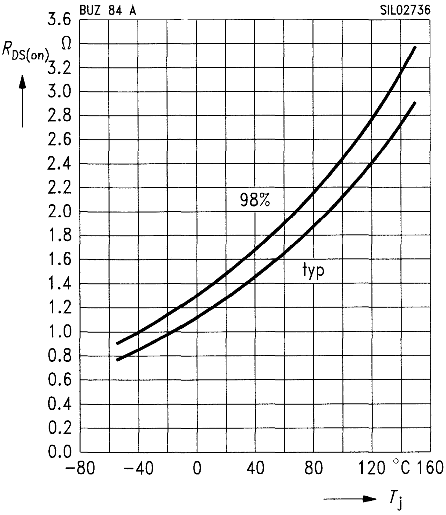
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 84**
parameter: I_D = 3.0 A, V_{GS} = 10 V, (spread)



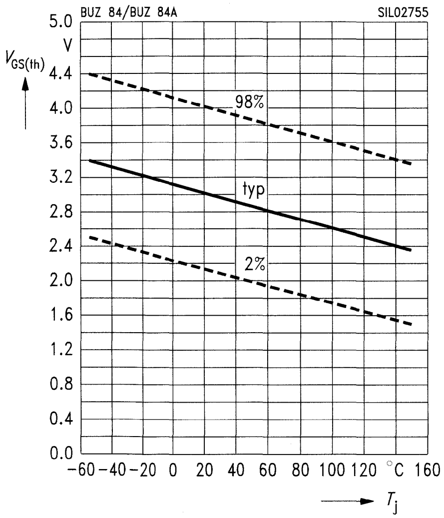
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 84 A**
parameter: I_D = 3.0 A, V_{GS} = 10 V, (spread)



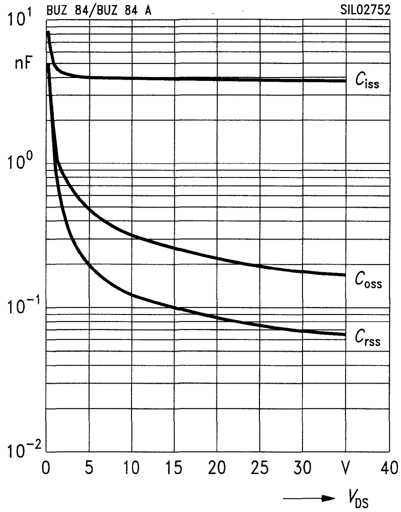
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



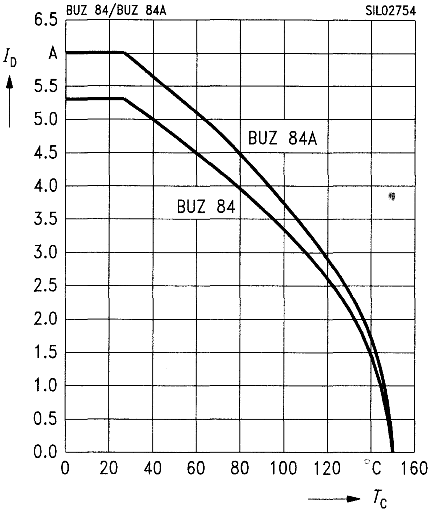
Typ. capacitances

$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



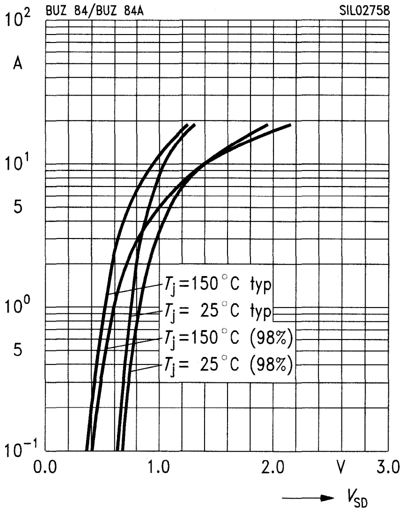
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



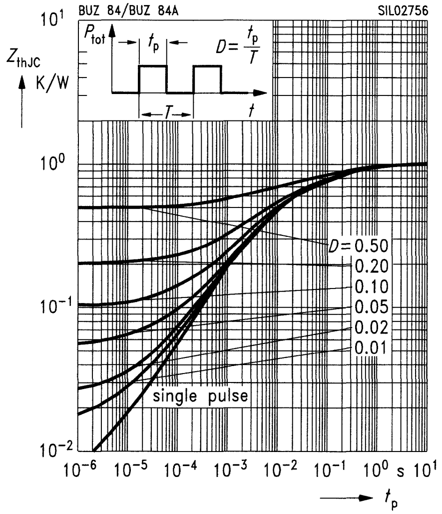
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs, (spread)

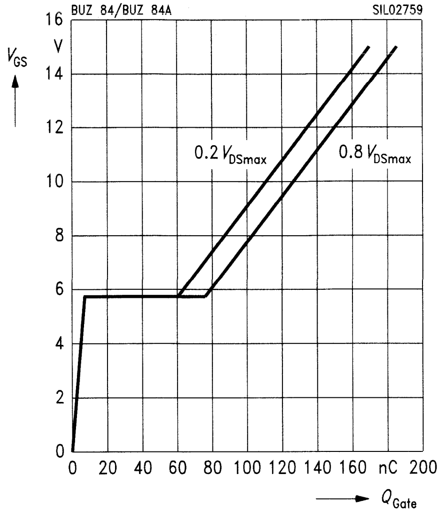


Transient thermal impedance

$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



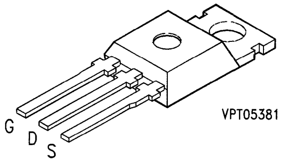
Typ. gate charge
$V_{GS} = f\,(Q_{Gate})$
parameter: $I_{D\ puls} = 9\ A$



SIPMOS® Power Transistors

BUZ 90
BUZ 90 A

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	T_C	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 90	600 V	4.5 A	28 ˚C	1.6 Ω	TO-220 AB	C67078-S1321-A2
BUZ 90 A	600 V	4.0 A	30 ˚C	2.0 Ω	TO-220 AB	C67078-S1321-A3

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		90	**90 A**	
Continuous drain current	I_D	**4.5**	**4.0**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**18**	**16**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**4.5**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**8.0**		mJ
Avalanche energy, single pulse I_D = 4.5 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 29 mH, T_j = 25 ˚C	E_{AS}	**320**		
Gate-source voltage	V_{GS}	**± 20**		V
Power dissipation, T_C = 25 ˚C	P_{tot}	**75**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

Static characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	600	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 600 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	µA
Drain-source on-resistance	$R_{DS\,(on)}$				Ω
V_{GS} = 10 V, I_D = 2.8 A BUZ 90		–	1.5	1.6	
BUZ 90 A		–	1.7	2.0	

Dynamic characteristics

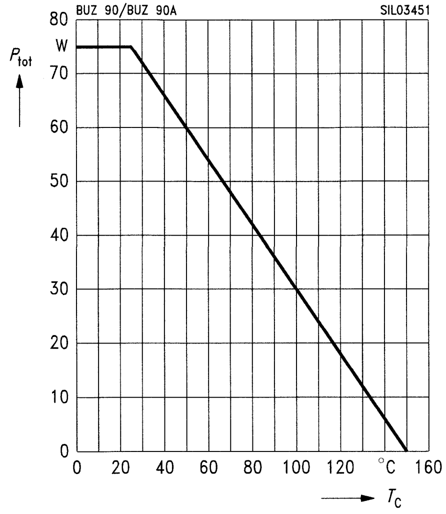
Parameter	Symbol	min.	typ.	max.	Unit
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 2.8 A	g_{fs}	2.5	3.8	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	780	1050	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	110	170	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	40	70	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.6 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	20	30	ns
	t_r	–	50	75	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.6 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	120	150	
	t_f	–	70	90	

Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

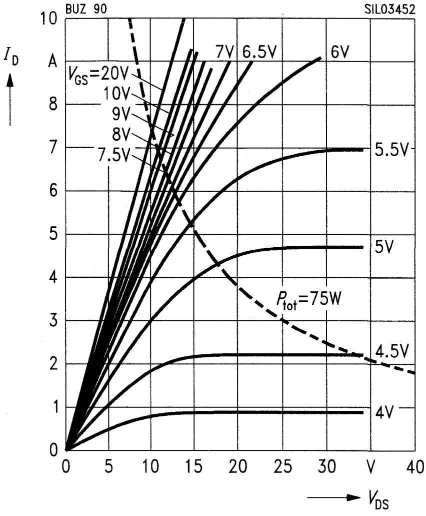
Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Reverse diode					
Continuous reverse drain current	I_S				A
T_C = 25 ˚C BUZ 90		–	–	4.5	
BUZ 90 A		–	–	4.0	
Pulsed reverse drain current	I_{SM}				
T_C = 25 ˚C BUZ 90		–	–	18	
BUZ 90 A		–	–	16	
Diode forward on-voltage I_S = 8.0 A, V_{GS} = 0 V	V_{SD}	–	1.1	1.2	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	350	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	3.0	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

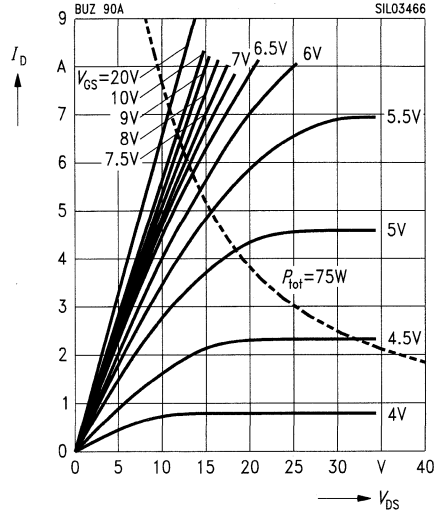
Total power dissipation
$P_{tot} = f(T_C)$



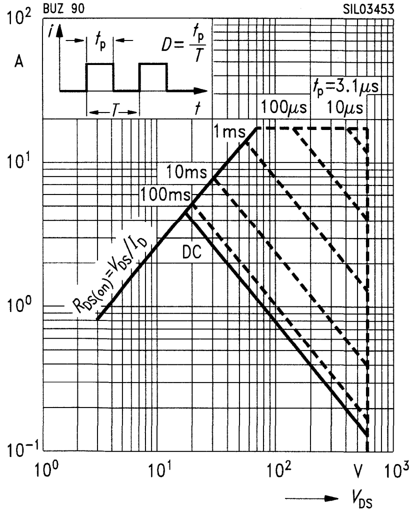
Typ. output characteristics
$I_D = f(V_{DS})$
BUZ 90
parameter: t_p = 80 µs



Typ. output characteristics
$I_D = f(V_{DS})$
BUZ 90 A
parameter: t_p = 80 µs



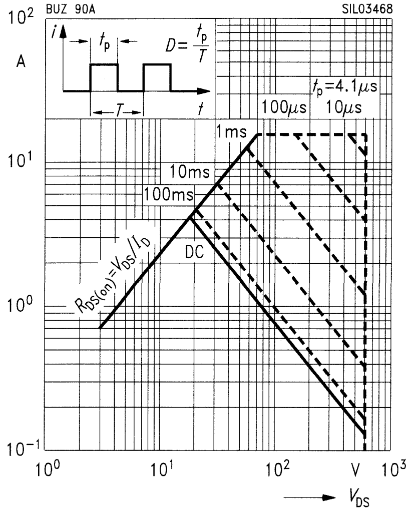
Safe operating area
$I_D = f(V_{DS})$
BUZ 90
parameter: D = 0.01, T_C = 25 °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 90 A**

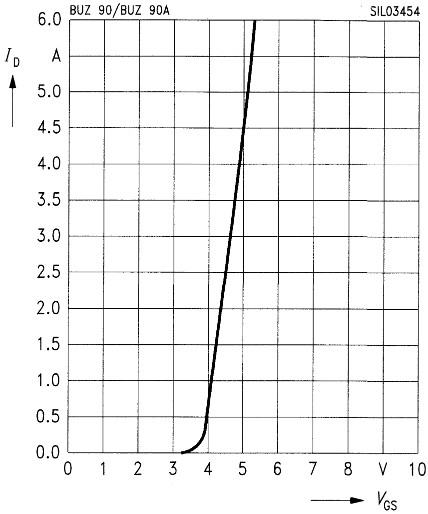
parameter: $D = 0.01$, $T_C = 25\ ^\circ C$



Typ. transfer characteristics

$I_D = f(V_{GS})$

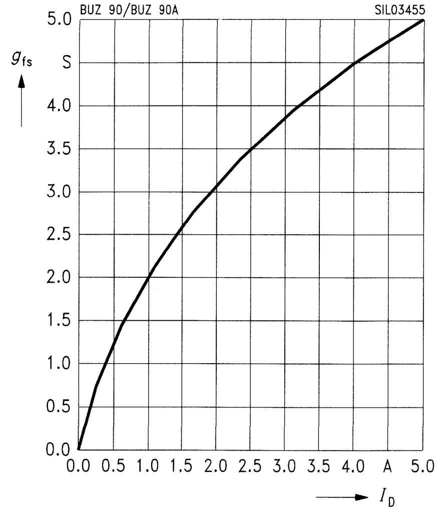
parameter: $t_p = 80\ \mu s$, $V_{DS} = 25\ V$



Typ. forward transconductance

$g_{fs} = f(I_D)$

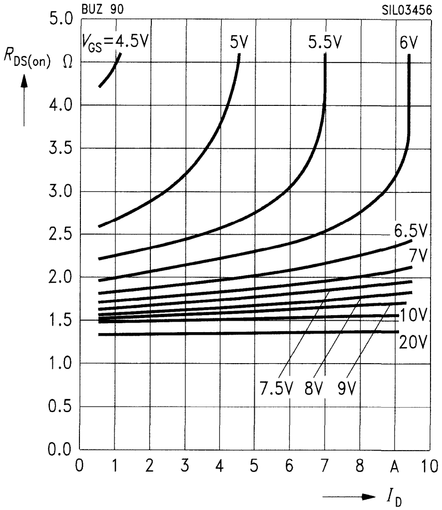
parameter: $t_p = 80\ \mu s$



Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 90**

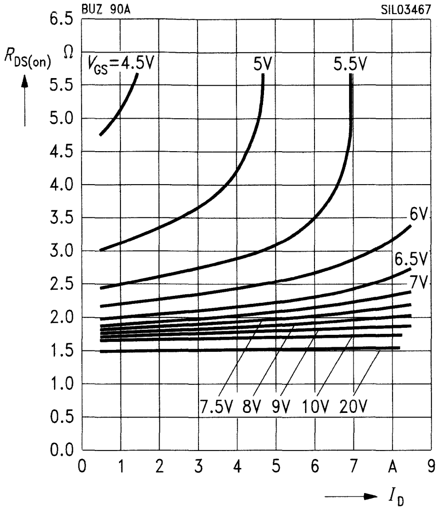
parameter: V_{GS}



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 90 A**

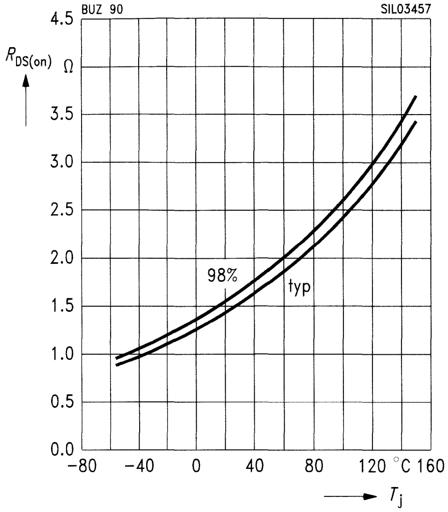
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 90**

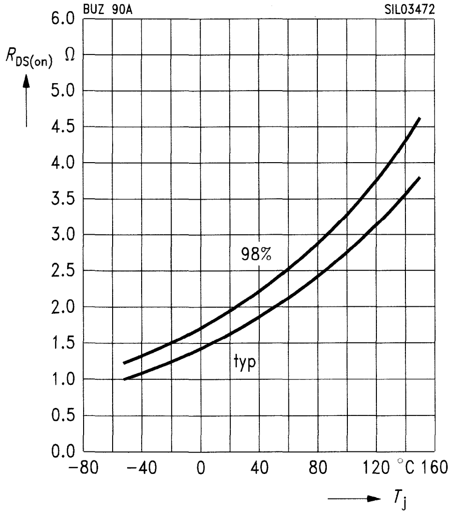
parameter: I_D = 2.8 A, V_{GS} = 10 V, (spread)



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 90 A**

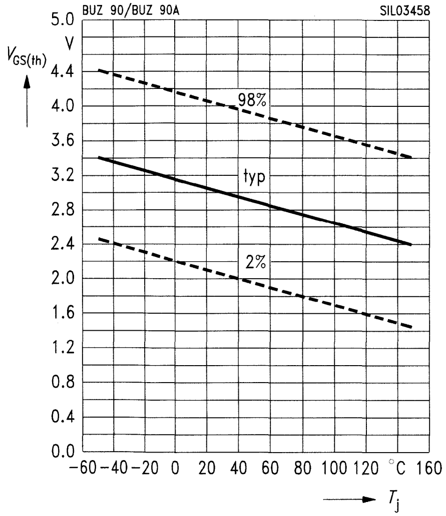
parameter: I_D = 2.8 A, V_{GS} = 10 V, (spread)



Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

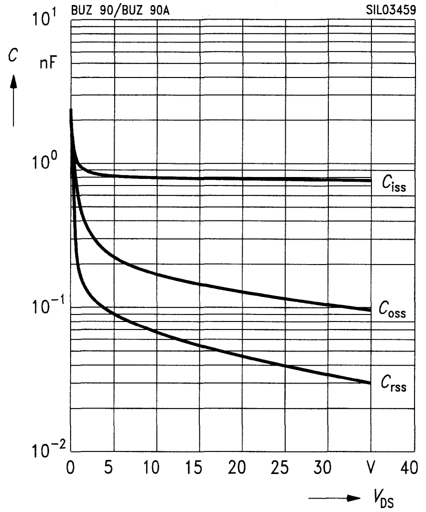
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

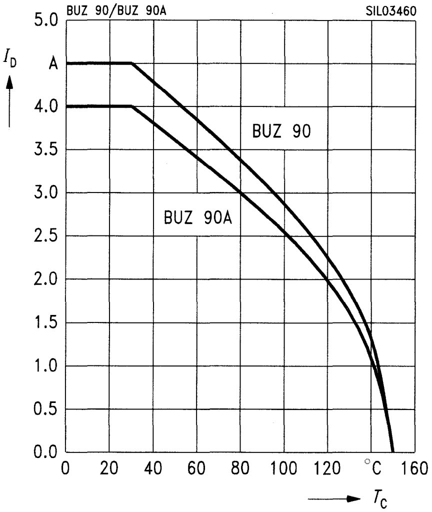
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

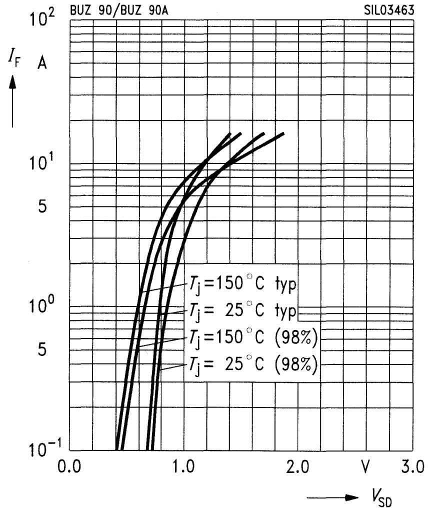
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

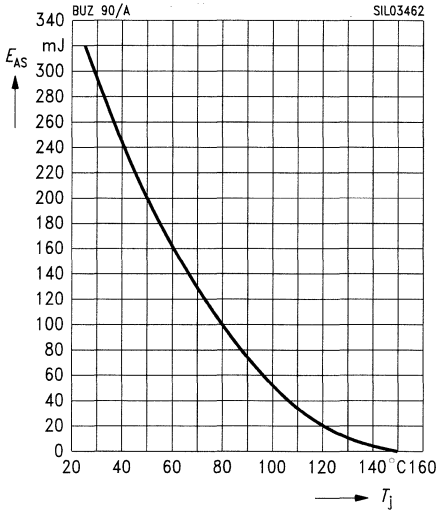
parameter: T_j, $t_p = 80$ µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

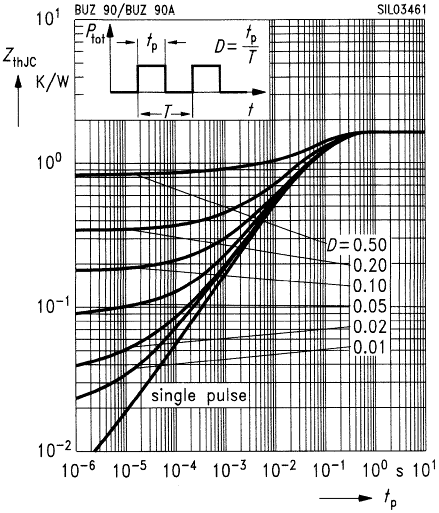
parameter: $I_D = 4.5$ A, $V_{DD} = 50$ V

$R_{GS} = 25\ \Omega$, $L = 29$ mH



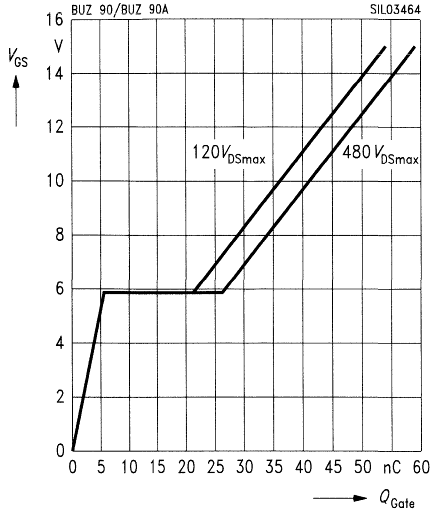
Transient thermal impedance

$Z_{\mathrm{th\,JC}} = f\,(t_p)$
parameter: $D = t_p\,/\,T$



Typ. gate charge

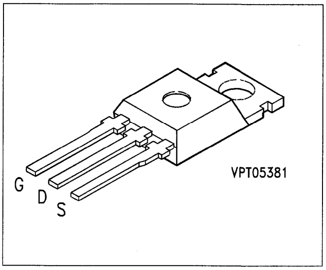
$V_{GS} = f\,(Q_{Gate})$
parameter: $I_{D\,puls}$ = 6.75 A



SIPMOS® Power Transistors

BUZ 91
BUZ 91 A

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	T_C	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 91	600 V	8.5 A	32 °C	0.8 Ω	TO-220 AB	C67078-S1342-A2
BUZ 91 A	600 V	8.0 A	33 °C	0.9 Ω	TO-220 AB	C67078-S1342-A3

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		91	91 A	
Continuous drain current	I_D	8.5	8.0	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	34	32	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	8.0		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	13		mJ
Avalanche energy, single pulse $I_D = 8$ A, $V_{DD} = 50$ V, $R_{GS} = 25\ \Omega$ $L = 16.3$ mH, $T_j = 25$ °C	E_{AS}	570		
Gate-source voltage	V_{GS}	± 20		V
Power dissipation, $T_C = 25$ °C	P_{tot}	150		W
Operating and storage temperature range	T_j , T_{stg}	– 55 ... + 150		°C

Thermal resistance, chip-case	$R_{th\,JC}$	≤ 0.83	K/W
DIN humidity category, DIN 40 040		E	–
IEC climatic category, DIN IEC 68-1		55/150/56	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	**typ.**	**max.**	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	600	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 600 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	µA
Drain-source on-resistance V_{GS} = 10 V, I_D = 5.0 A	$R_{DS\,(on)}$	–	0.7	0.8	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 5.0 A	g_{fs}	5.0	8.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1400	2100	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	180	270	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	65	100	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{CC} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	20	30	ns
	t_r	–	70	110	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{CC} = 30 V, V_{GS} = 10 V, I_D = 3.07 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	250	330	
	t_f	–	80	100	

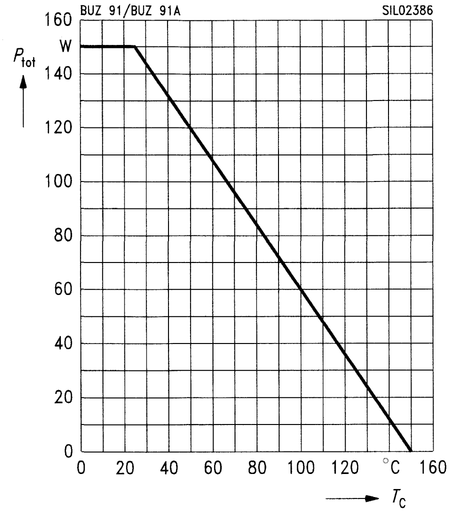
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Reverse diode					
Continuous reverse drain current T_C = 25 °C BUZ 91 BUZ 91 A	I_S	 – –	 – –	 8.5 8.0	A
Pulsed reverse drain current T_C = 25 °C BUZ 91 BUZ 91 A	I_{SM}	–	 – –	 34 32	
Diode forward on-voltage I_S = 16 A, V_{GS} = 0 V	V_{SD}	–	1.1	1.2	V
Reverse recovery time V_R = 100 V, I_F = I_S, di_F / dt = 100 A/µs	t_{rr}	–	480	–	ns
Reverse recovery charge V_R = 100 V, I_F = I_S, di_F / dt = 100 A/µs	Q_{rr}	–	6.5	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

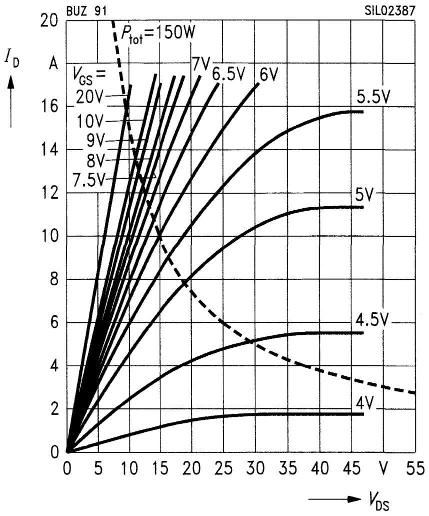
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 91**

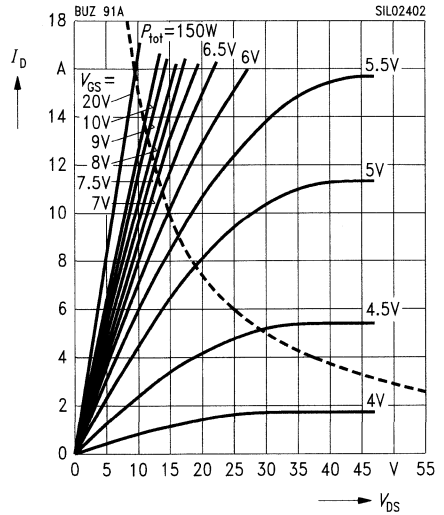
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 91 A**

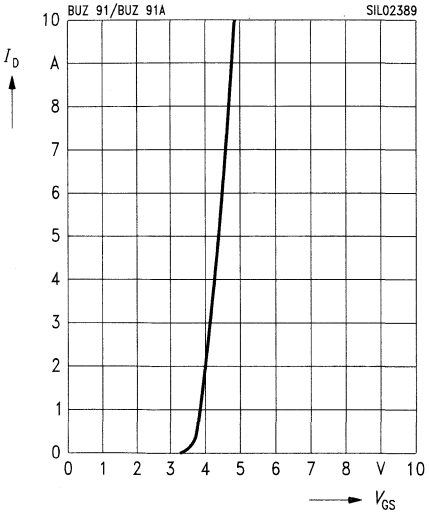
parameter: t_p = 80 µs



Typ. transfer characteristics

$I_D = f(V_{GS})$

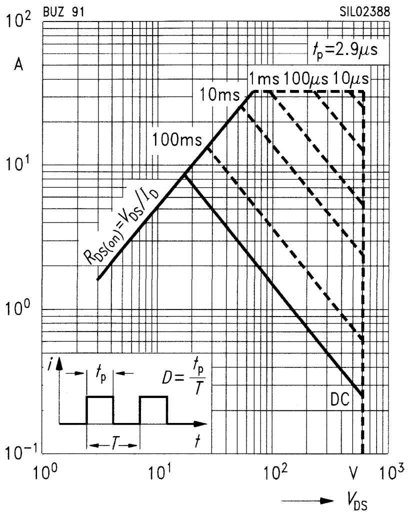
parameter: t_p = 80 µs, V_{DS} = 25 V



Safe operating area

$I_D = f(V_{DS})$ **BUZ 91**

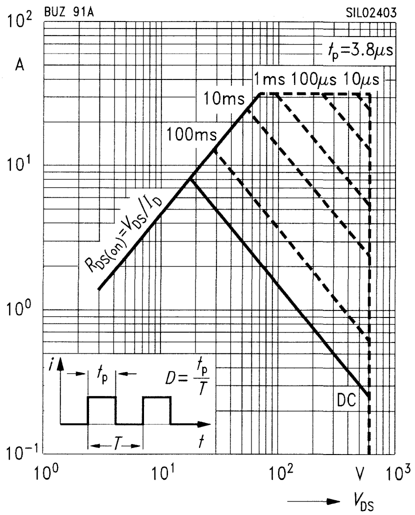
parameter: $D = 0.01$, $T_C = 25$ °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 91 A**

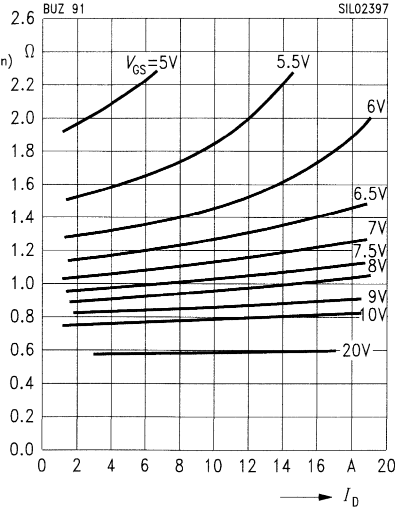
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$ **BUZ 91**

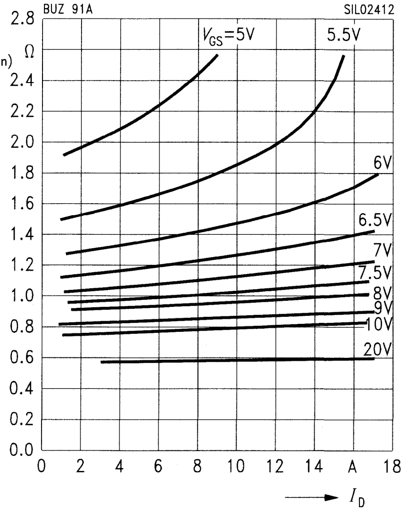
parameter: V_{GS}



Typ. drain-source on-resistance

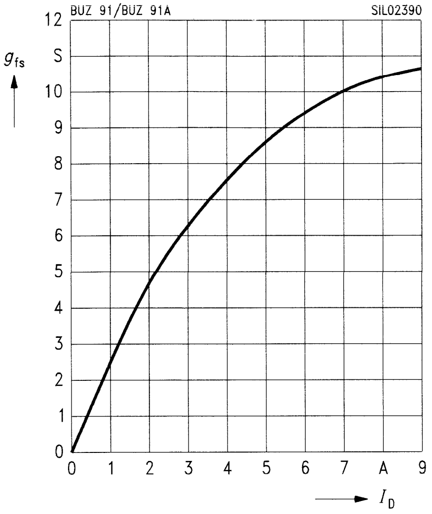
$R_{DS\,(on)} = f(I_D)$ **BUZ 91 A**

parameter: V_{GS}



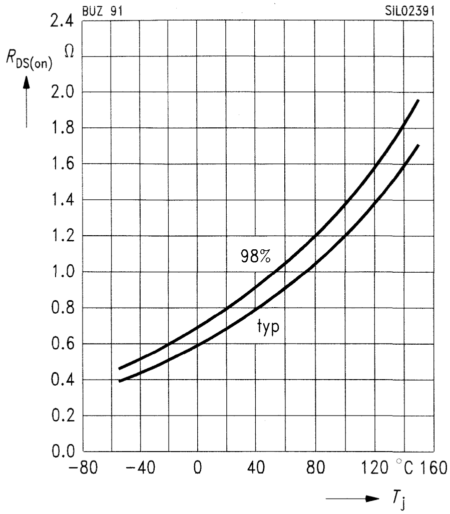
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: t_p = 80 µs



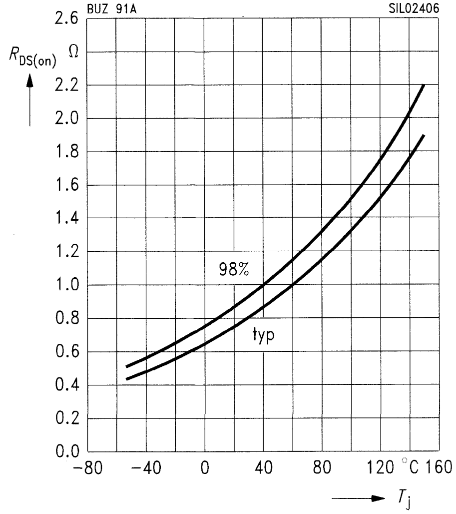
Drain-source on-resistance

$R_{DS(on)} = f(T_j)$ **BUZ 91**
parameter: I_D = 5 A, V_{GS} = 10 V, (spread)



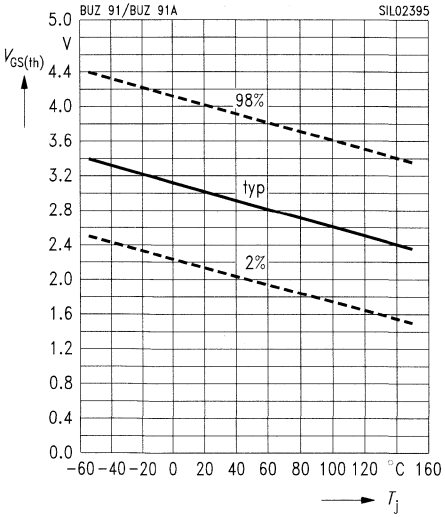
Drain-source on-resistance

$R_{DS(on)} = f(T_j)$ **BUZ 91 A**
parameter: I_D = 5 A, V_{GS} = 10 V, (spread)

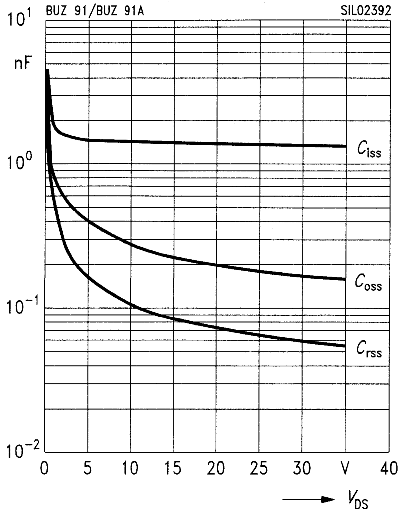


Gate threshold voltage

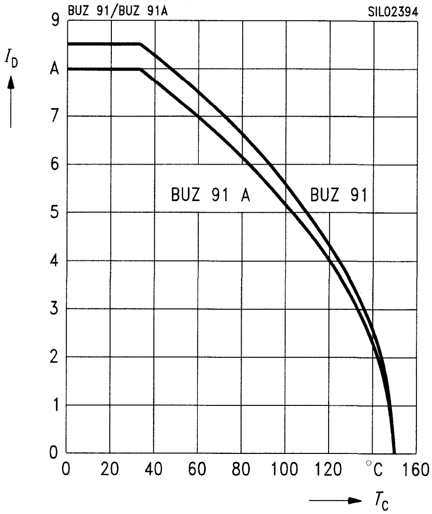
$V_{GS(th)} = f(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



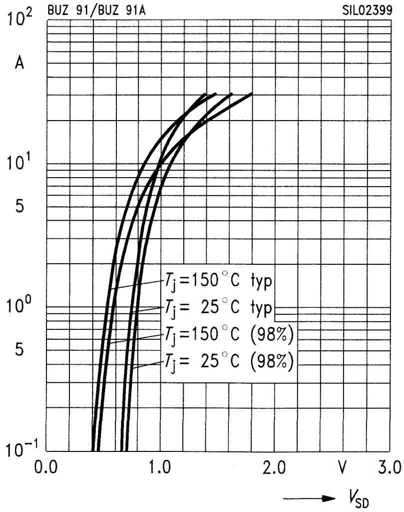
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



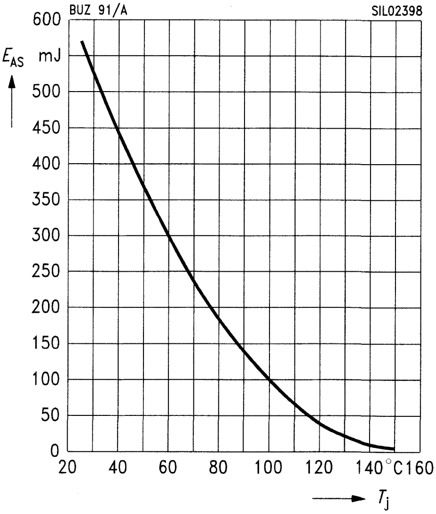
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j , $t_p = 80$ µs, (spread)

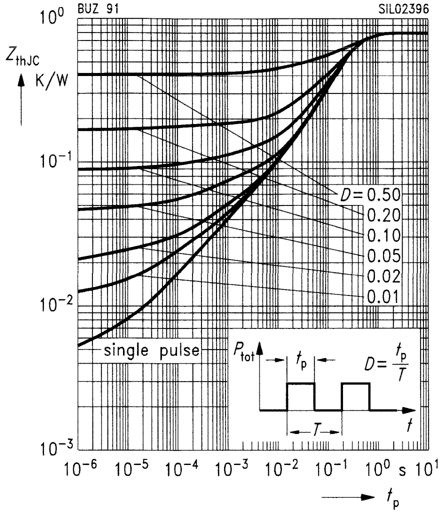


Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 8$ A, $V_{DD} = 50$ V
$R_{GS} = 25\ \Omega$, $L = 16.3$ mH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$

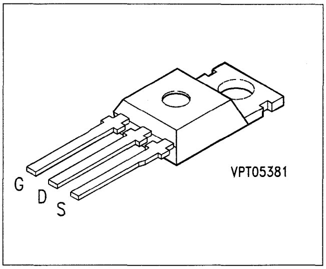


SIEMENS

SIPMOS® Power Transistors

BUZ 92
BUZ 93

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 92	600 V	3.3 A	3.0 Ω	TO-220 AB	C67078-S1343-A2
BUZ 93	600 V	3.6 A	2.5 Ω	TO-220 AB	C67078-S1346-A2

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		92	93	
Continuous drain current, T_C = 25 ˚C	I_D	**3.3**	**3.6**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**13**	**14.5**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**3.3**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**6**		mJ
Avalanche energy, single pulse I_D = 3.3 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 37 mH, T_j = 25 ˚C	E_{AS}	**220**		
Gate-source voltage	V_{GS}	**± 20**		V
Power dissipation, T_C = 25 ˚C	P_{tot}	**80**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.56**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	600	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 600 V, V_{GS} = 0 V T_j = 25 °C T_j = 125 °C	I_{DSS}	 – –	 0.1 10	 1.0 100	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 2.0 A BUZ 92 BUZ 93	$R_{DS\,(on)}$	 – –	 2.6 2.0	 3.0 2.5	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 2.0 A	g_{fs}	2.1	3.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	600	900	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	65	100	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	25	40	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	10	15	ns
	t_r	–	50	70	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	70	95	
	t_f	–	40	55	

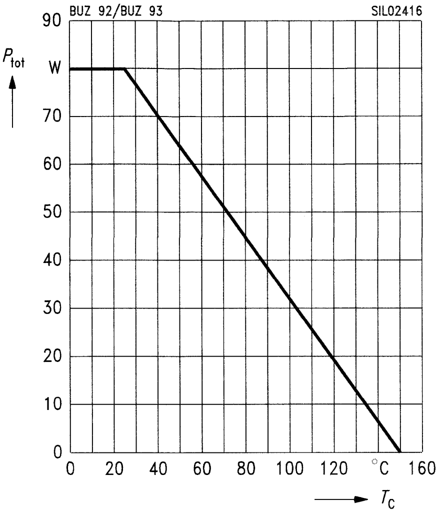
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter		Symbol	Values			Unit
			min.	typ.	max.	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 °C	BUZ 92		–	–	3.3	
	BUZ 93		–	–	3.6	
Pulsed reverse drain current		I_{SM}				
T_C = 25 °C	BUZ 92		–	–	13	
	BUZ 93		–	–	14.5	
Diode forward on-voltage I_S = 6.6 A, V_{GS} = 0 V		V_{SD}	–	1.0	1.4	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		t_{rr}	–	300	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		Q_{rr}	–	2.5	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

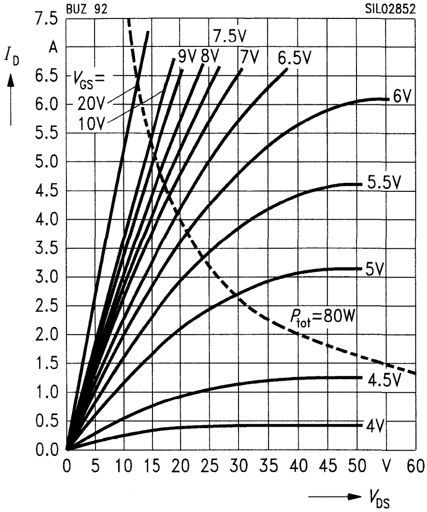
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 92**

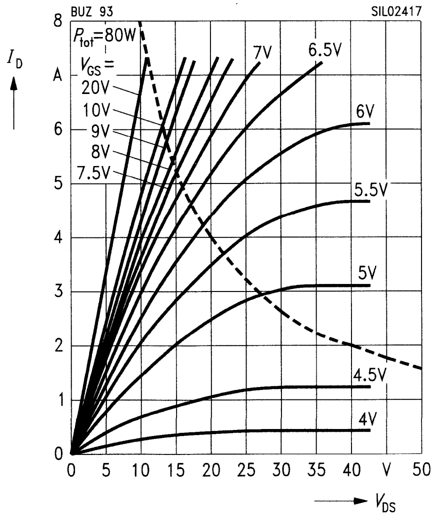
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 93**

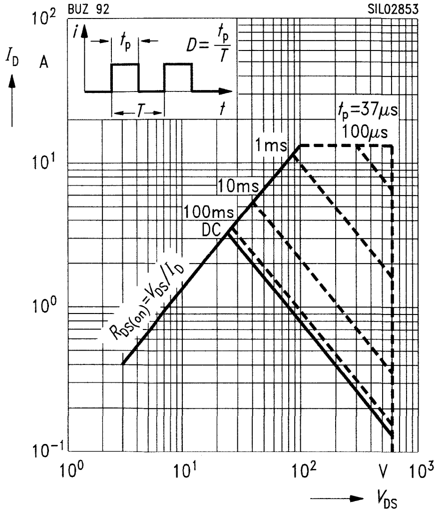
parameter: t_p = 80 µs



Safe operating area

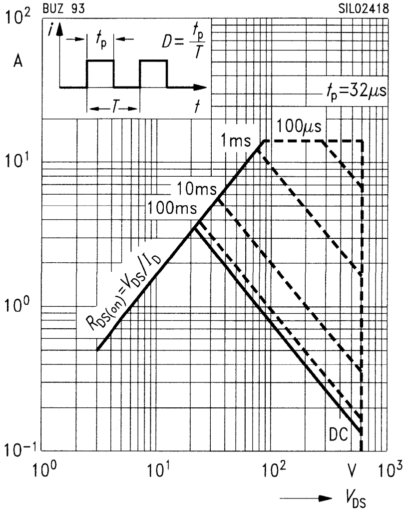
$I_D = f(V_{DS})$ **BUZ 92**

parameter: D = 0.01, T_C = 25 °C



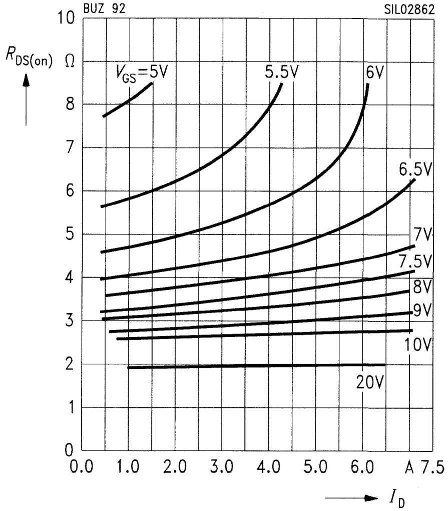
Safe operating area

$I_D = f(V_{DS})$ **BUZ 93**
parameter: $D = 0.01$, $T_C = 25$ °C



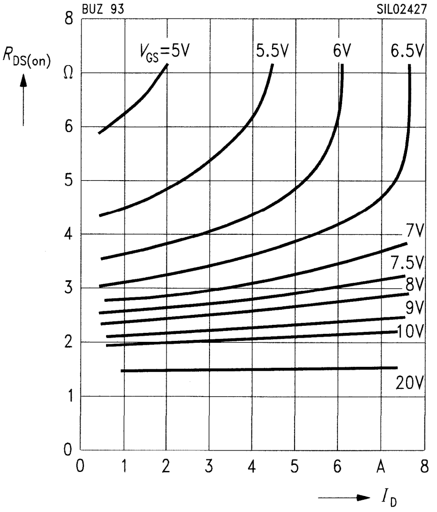
Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$ **BUZ 92**
parameter: V_{GS}



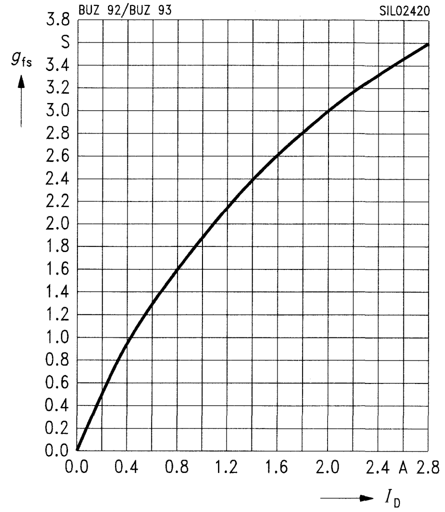
Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$ **BUZ 93**
parameter: V_{GS}



Typ. forward transconductance

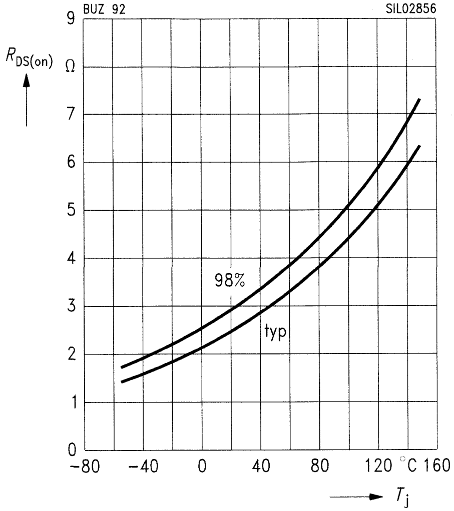
$g_{fs} = f(I_D)$
parameter: t_p = 80 µs



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 92**

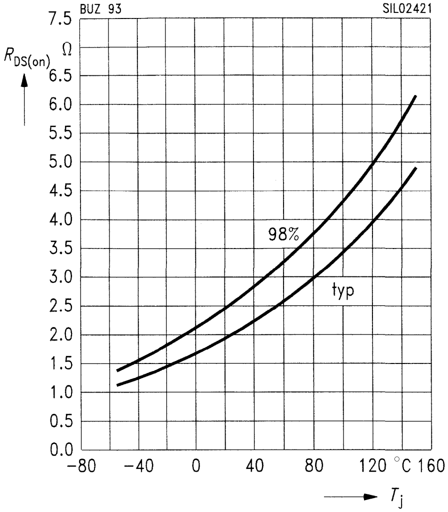
parameter: I_D = 2 A, V_{GS} = 10 V, (spread)



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 93**

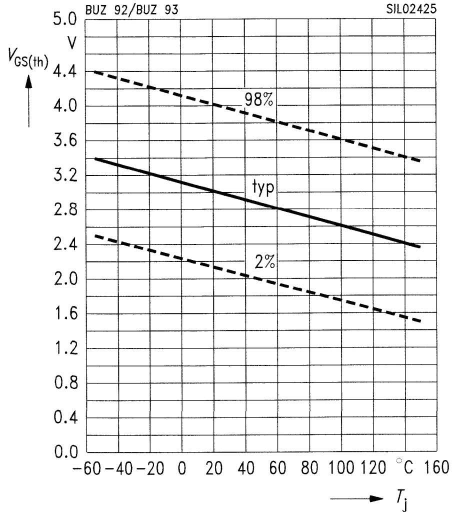
parameter: I_D = 2 A, V_{GS} = 10 V, (spread)



Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

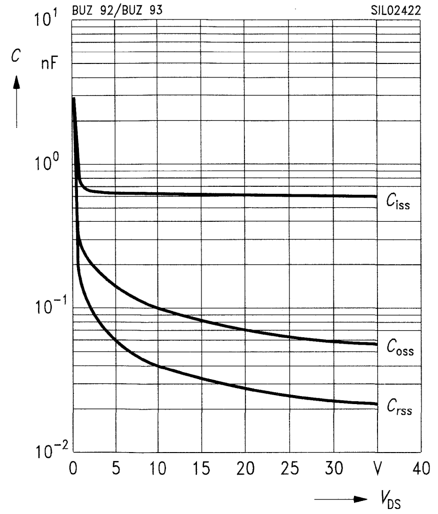
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

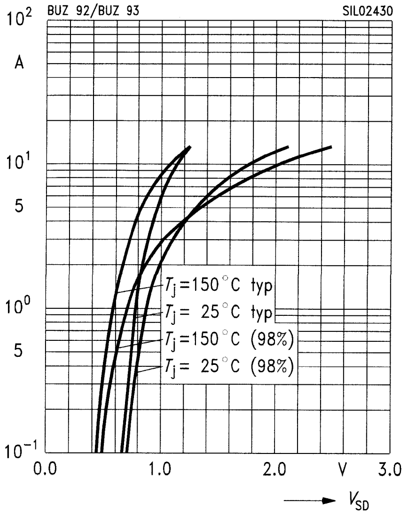
$C = f\,(V_{DS})$

parameter: V_{GS} = 0 V, f = 1 MHz



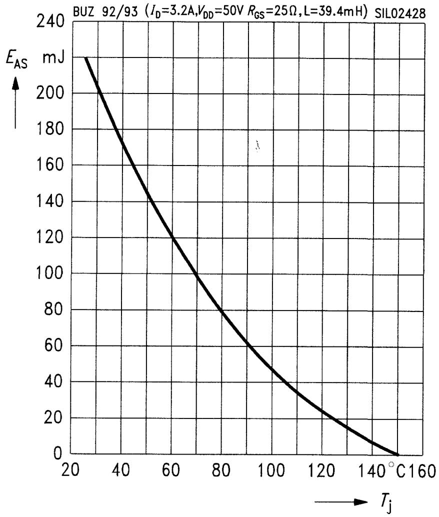
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: T_j , t_p = 80 µs, (spread)



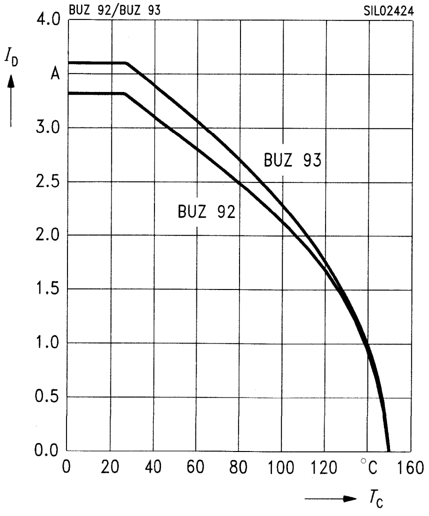
Avalanche energy $E_{AS} = f(T_j)$

parameter: I_D = 3.2 A, V_{DD} = 50 V
R_{GS} = 25 Ω, L = 39.4 mH



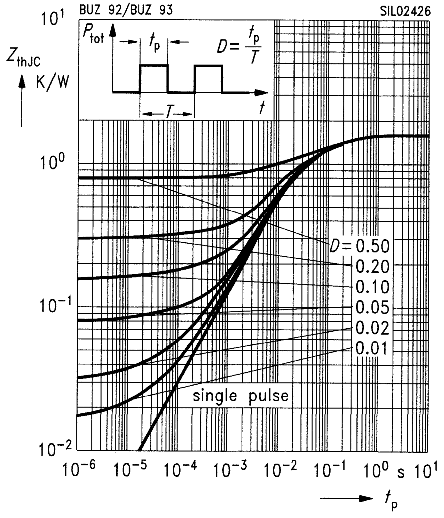
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq$ 10 V

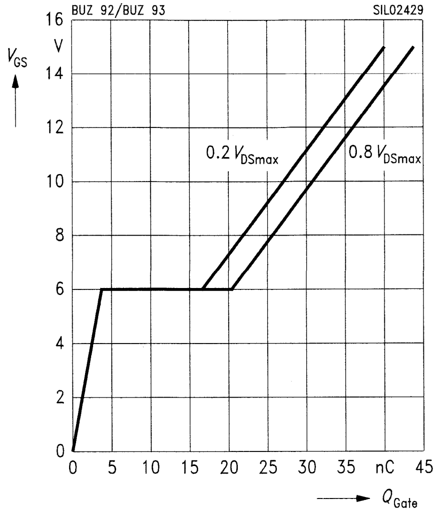


Transient thermal impedance

$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



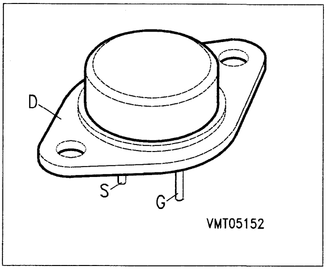
Typ. gate charge
$V_{GS} = f\,(Q_{Gate})$
parameter: $I_{D\ puls} = 4.8$ A



SIPMOS® Power Transistor

BUZ 94

- N channel
- Enhancement mode



Type	V_{DS}	I_D	$R_{DS\,(on)}$	**Package** [1]	**Ordering Code**
BUZ 94	600 V	7.8 A	0.9 Ω	TO-204 AA	C67078-A1019-A2

Maximum Ratings

Parameter	**Symbol**	**Values**	**Unit**
Continuous drain current, T_C = 27 °C	I_D	**7.8**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**31**	
Drain-source voltage	V_{DS}	**600**	V
Drain-gate voltage, R_{GS} = 20 kΩ	V_{DGR}	**600**	
Gate-source voltage	V_{GS}	**± 20**	
Power dissipation, T_C = 25 °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**C**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	600	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.9	
Zero gate voltage drain current V_{DS} = 600 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 ˚C		–	20	250	
T_j = 125 ˚C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 5.0 A	$R_{DS\,(on)}$	–	0.8	0.9	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 5.0 A	g_{fs}	2.7	5.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	3.8	4.9	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	250	400	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	100	170	
Turn-on time t_{on}, ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.8 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	50	75	ns
	t_r	–	80	120	
Turn-off time t_{off}, ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.8 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	330	430	
	t_f	–	110	140	

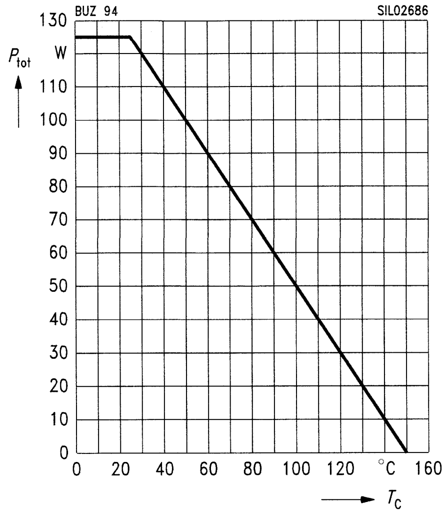
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	7.5	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	30	
Diode forward on-voltage I_S = 15 A, V_{GS} = 0 V	V_{SD}	–	1.3	1.7	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	1.2	–	µs
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	12	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

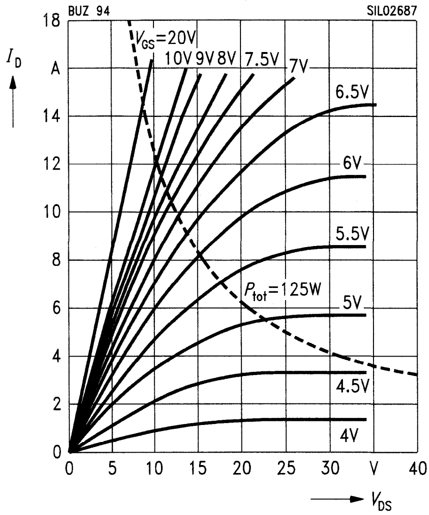
Total power dissipation

$P_{tot} = f\,(T_C)$



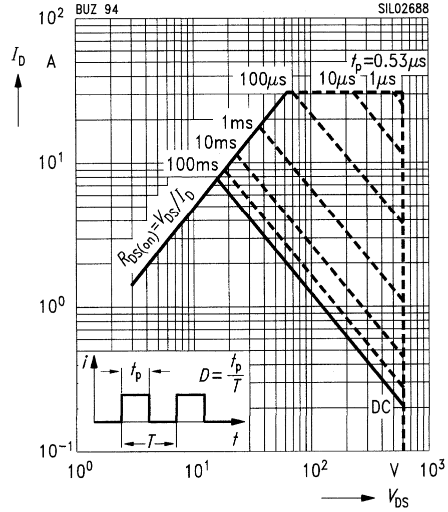
Typ. output characteristics

$I_D = f\,(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



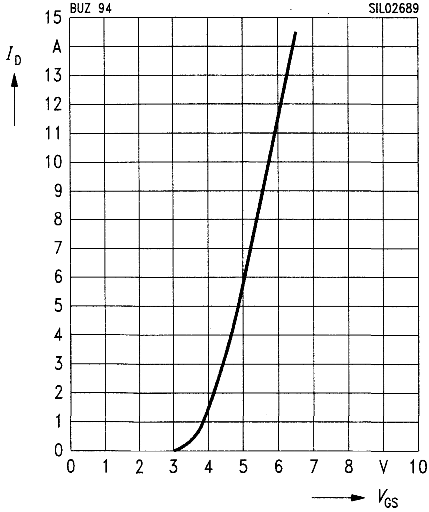
Safe operating area

$I_D = f\,(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

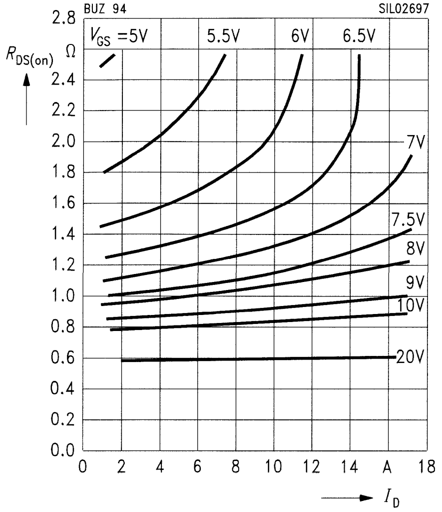
$I_D = f\,(V_{GS})$
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$

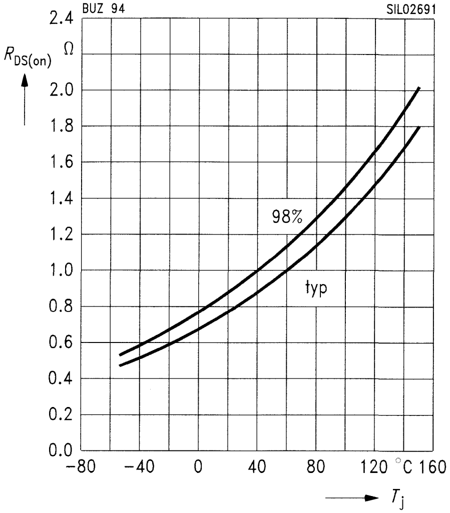
parameter: V_{GS}



Drain-source on-resistance

$R_{DS(on)} = f(T_j)$

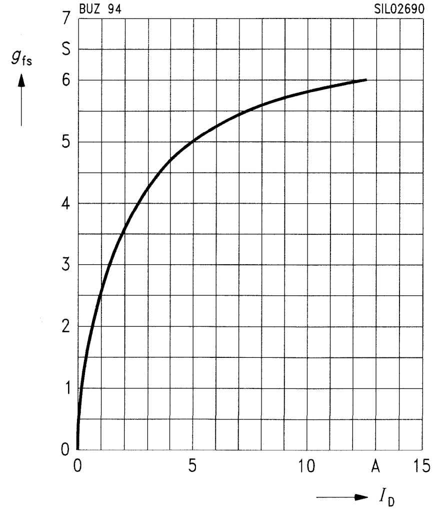
parameter: I_D = 5.0 A, V_{GS} = 10 V, (spread)



Typ. forward transconductance

$g_{fs} = f(I_D)$

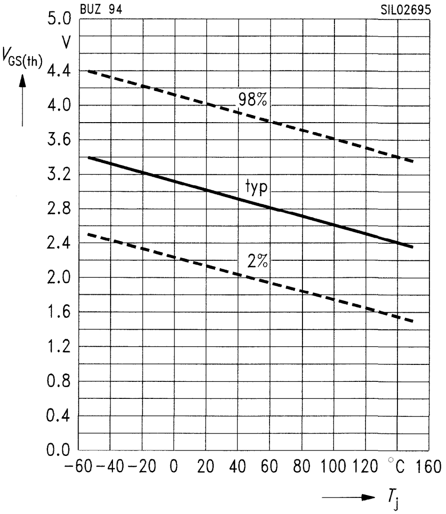
parameter: t_p = 80 µs



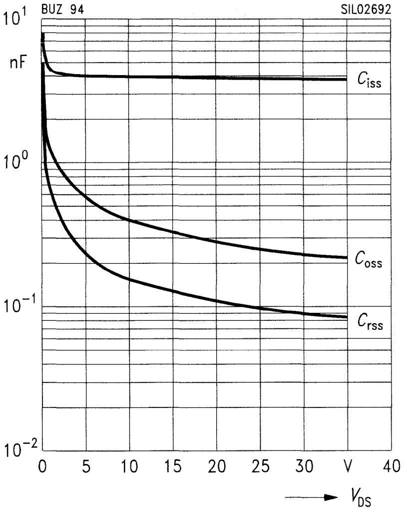
Gate threshold voltage

$V_{GS(th)} = f(T_j)$

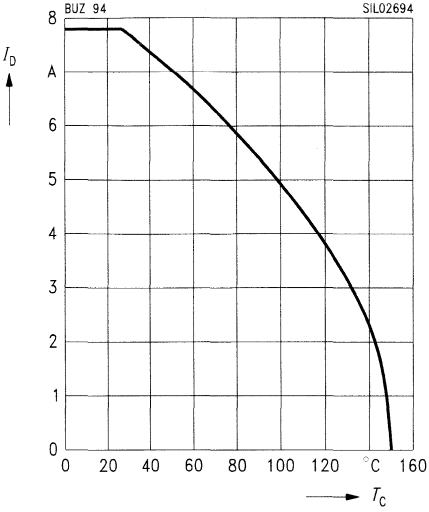
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



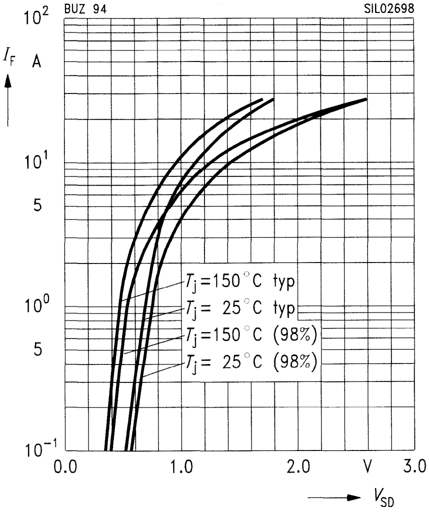
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



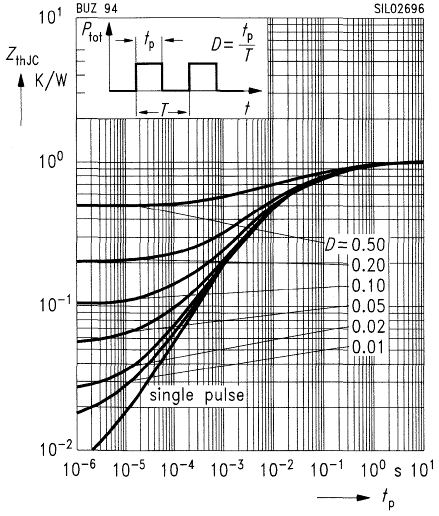
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j , $t_p = 80$ µs, (spread)



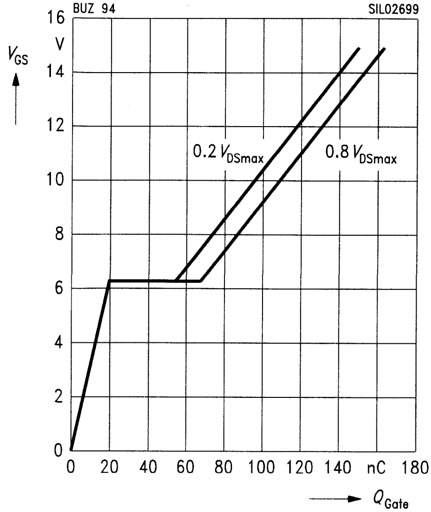
Transient thermal impedance
$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f\,(Q_{Gate})$

parameter: $I_{D\,puls}$ = 11.7 A

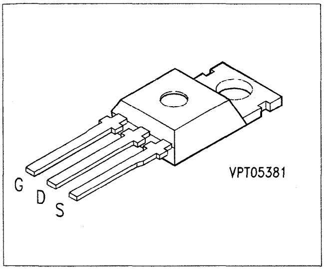


SIEMENS

SIPMOS® Power Transistor

BUZ 100

- N channel
- Enhancement mode
- Avalanche-rated
- dv/dt rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 100	50 V	60 A	0.018 Ω	TO-220 AB	C67078-S1348-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 101 °C	I_D	**60**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**240**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**60**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**28**	mJ
Avalanche energy, single pulse I_D = 60 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 79 µH, T_j = 25 °C	E_{AS}	**285**	
Reverse diode dv/dt I_S = 60 A, V_{DS} = 40 $T_{S\,max}$ = di/dt = 200 A/µs	dv/dt	**6.0**	kV/ µs
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**250**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 175**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 0.6**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

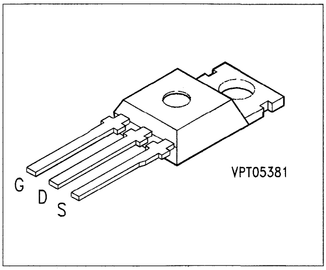
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	50	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 50 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 150 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 60 A	$R_{DS(on)}$	–	0.014	0.018	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 60 A	g_{fs}	25.0	39.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	2400	3200	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	800	1200	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	300	450	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	40	60	ns
	t_r	–	100	150	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	250	335	
	t_f	–	140	190	

Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	60	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	240	
Diode forward on-voltage I_S = 120 A, V_{GS} = 0 V	V_{SD}	–	1.4	1.8	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	70	–	µs
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.16	–	µC

SIPMOS® Power Transistor **BUZ 171**

- P channel
- Enhancement mode
- Avalanche rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	**Package** [1]	**Ordering Code**
BUZ 171	– 50 V	– 8.0 A	0.3 Ω	TO-220 AB	C67078-S1450-A2

Maximum Ratings

Parameter	**Symbol**	**Values**	**Unit**
Continuous drain current, T_C = 30 ˚C	I_D	**– 8.0**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**– 32**	
Avalanche energy, single pulse I_D = – 8.0 A, V_{DD} = – 25 V, R_{GS} = 25 Ω L = 1.88 mH, T_j = 25 ˚C	E_{AS}	**120**	mJ
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 ˚C	P_{tot}	**40**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

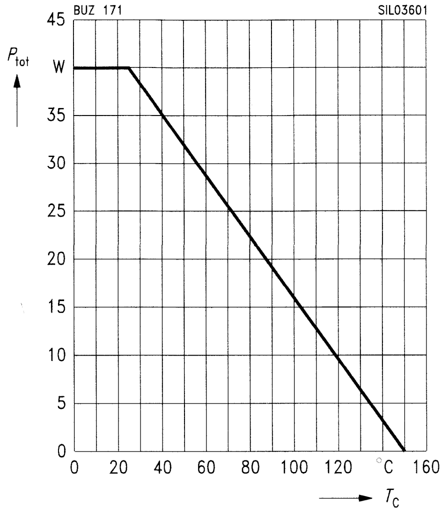
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = – 0.25 mA	$V_{(BR)\,DSS}$	– 50	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = – 1 mA	$V_{GS\,(th)}$	– 2.1	– 3.0	– 4.0	
Zero gate voltage drain current V_{DS} = – 50 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	– 20	– 250	
T_j = 125 °C		–	– 100	– 1000	
Gate-source leakage current V_{GS} = – 20 V, V_{DS} = 0 V	I_{GSS}	–	– 10	– 100	nA
Drain-source on-resistance V_{GS} = – 10 V, I_D = – 5.0 A	$R_{DS\,(on)}$	–	0.25	0.3	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = – 5.0 A	g_{fs}	1.5	2.3	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{iss}	–	850	1300	pF
Output capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{oss}	–	350	550	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{rss}	–	130	200	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = – 30 V, V_{GS} = – 10 V, I_D = – 2.9 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	20	30	ns
	t_r	–	60	95	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = – 30 V, V_{GS} = – 10 V, I_D = – 2.9 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	70	90	
	t_f	–	55	75	

Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

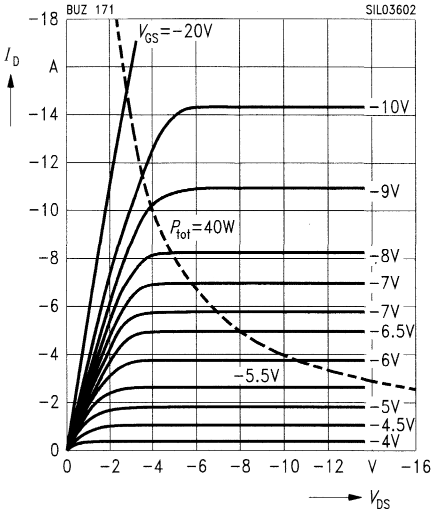
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	– 8.0	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	– 32	
Diode forward on-voltage I_S = – 16 A, V_{GS} = 0 V	V_{SD}	–	– 1.0	– 1.7	V
Reverse recovery time V_R = – 30 V, I_F = I_S, di_F / dt = – 100 A/µs	t_{rr}	–	90	–	ns
Reverse recovery charge V_R = – 30 V, I_F = I_S, di_F / dt = – 100 A/µs	Q_{rr}	–	0.23	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

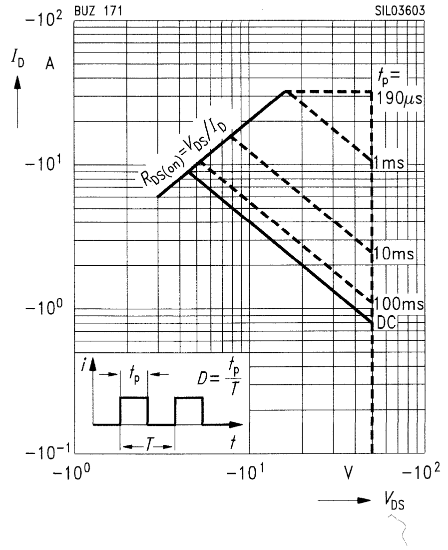
Total power dissipation
$P_{tot} = f(T_C)$



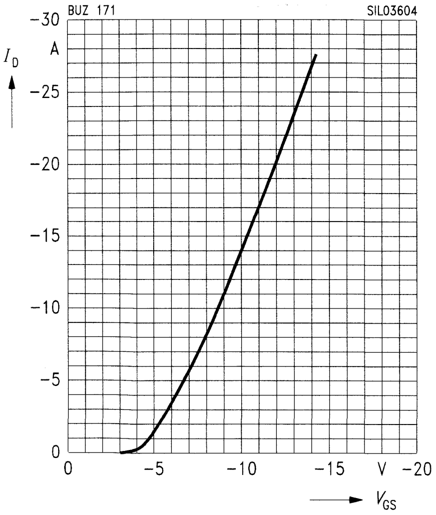
Typ. output characteristics
$I_D = f(V_{DS})$
parameter: t_p = 80 µs



Safe operating area
$I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



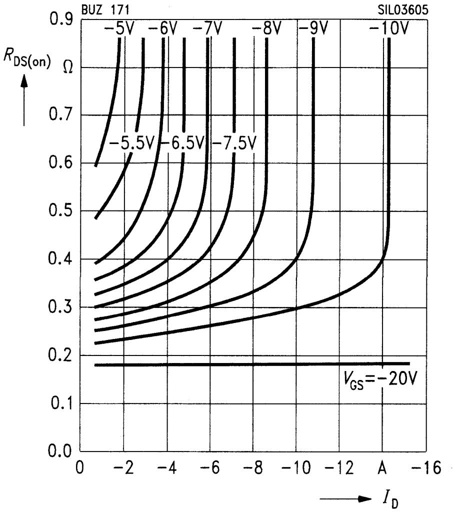
Typ. transfer characteristics
$I_D = f(V_{GS})$
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

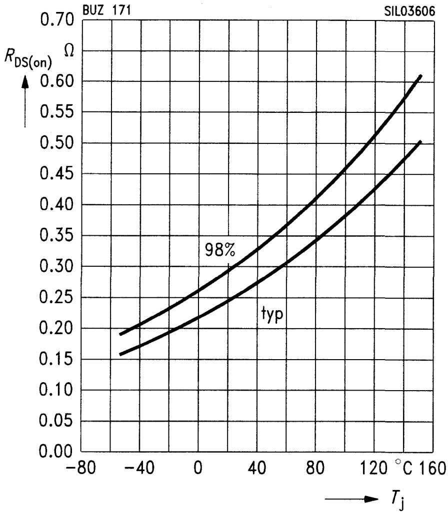
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

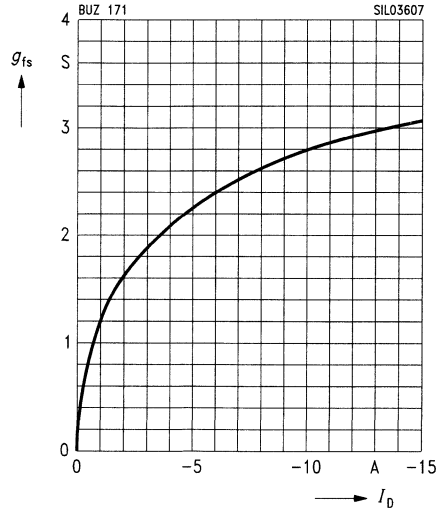
parameter: $I_D = -5$ A, $V_{GS} = -10$ V, (spread)



Typ. forward transconductance

$g_{fs} = f\,(I_D)$

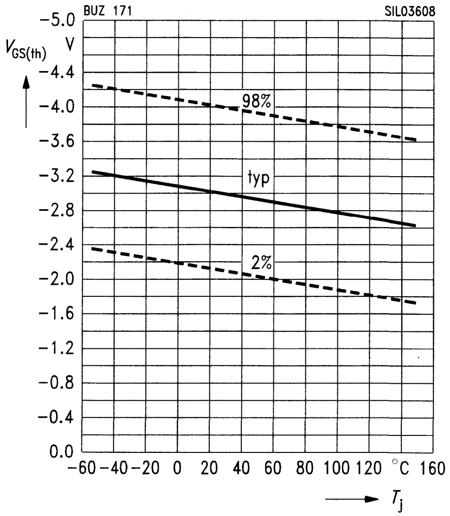
parameter: $t_p = 80$ µs



Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

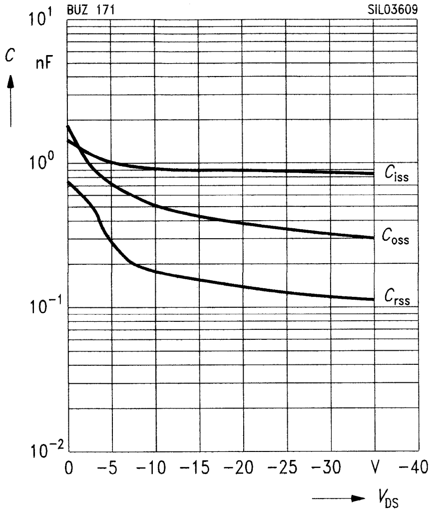
parameter: $V_{GS} = V_{DS}$, $I_D = -1$ mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

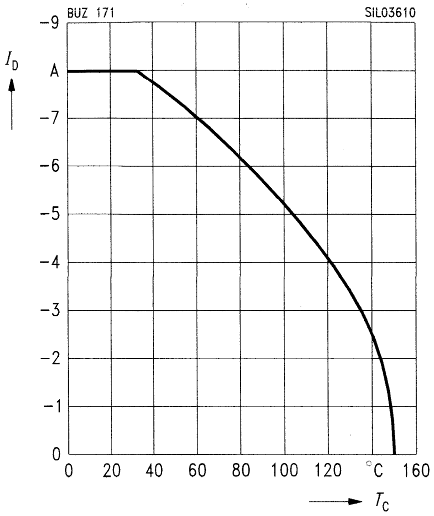
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

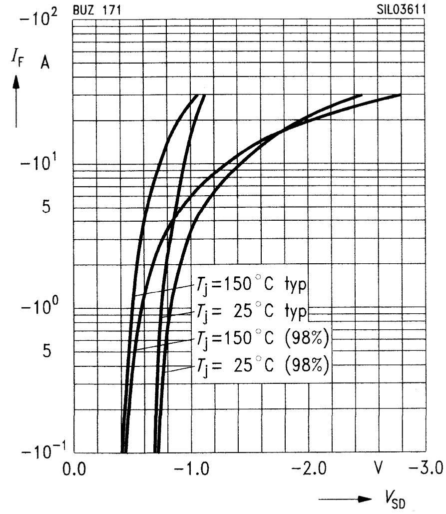
parameter: $V_{GS} \geq -10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

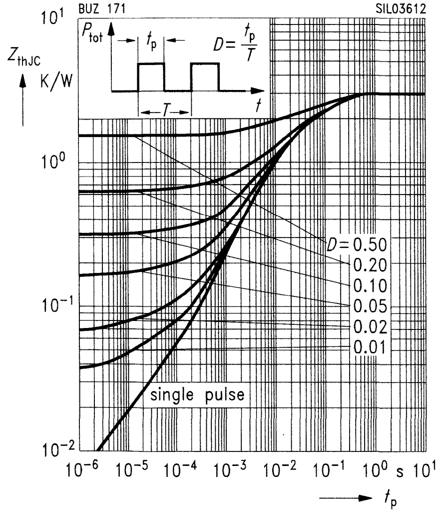
parameter: T_j , $t_p = 80$ µs, (spread)



Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

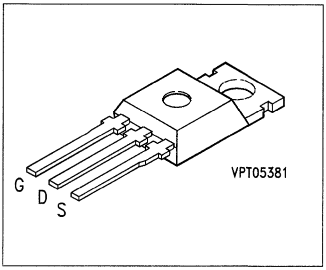
parameter: $D = t_p / T$



SIPMOS® Power Transistor

BUZ 172

- P channel
- Enhancement mode
- Avalanche rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 172	– 100 V	– 5.5 A	0.6 Ω	TO-220 AB	C67078-A1451-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 37 °C	I_D	**– 5.5**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**– 22.0**	
Avalanche energy, single pulse V_{DD} = – 25 V, R_{GS} = 25 Ω, T_j = 25 °C I_D = – 5.5 A, L = 8.4 mH	E_{AS}	**170**	mJ
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**40**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = – 0.25 mA	$V_{(BR)\,DSS}$	– 100	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = – 1 mA	$V_{GS\,(th)}$	– 2.1	– 3.0	– 4.0	
Zero gate voltage drain current V_{DS} = – 100 V, V_{GS} = 0 V T_j = 25 °C T_j = 125 °C	I_{DSS}	 – –	 – 20 – 100	 – 250 – 1000	µA
Gate-source leakage current V_{GS} = – 20 V, V_{DS} = 0 V	I_{GSS}	–	– 10	– 100	nA
Drain-source on-resistance V_{GS} = – 10 V, I_D = – 3.7 A	$R_{DS\,(on)}$	–	0.4	0.6	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = – 3.7 A	g_{fs}	1.0	2.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{iss}	–	800	1200	pF
Output capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{oss}	–	220	330	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{rss}	–	90	140	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = – 30 V, V_{GS} = – 10 V, I_D = – 2.8 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	20	30	ns
	t_r	–	60	95	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = – 30 V, V_{GS} = – 10 V, I_D = – 2.8 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	70	90	
	t_f	–	55	75	

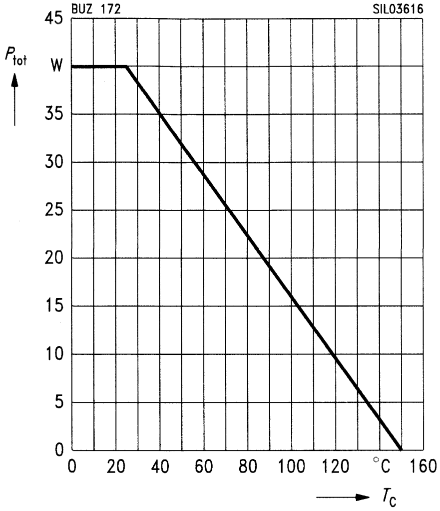
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	– 5.5	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	– 22.0	
Diode forward on-voltage I_S = – 11 A, V_{GS} = 0 V	V_{SD}	–	– 1.0	– 1.3	V
Reverse recovery time V_R = – 30 V, $I_F = I_S$, di_F / dt = – 100 A/µs	t_{rr}	–	200	–	ns
Reverse recovery charge V_R = – 30 V, $I_F = I_S$, di_F / dt = – 100 A/µs	Q_{rr}	–	0.75	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

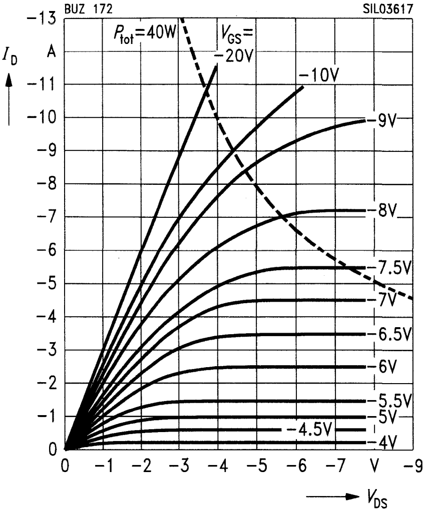
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

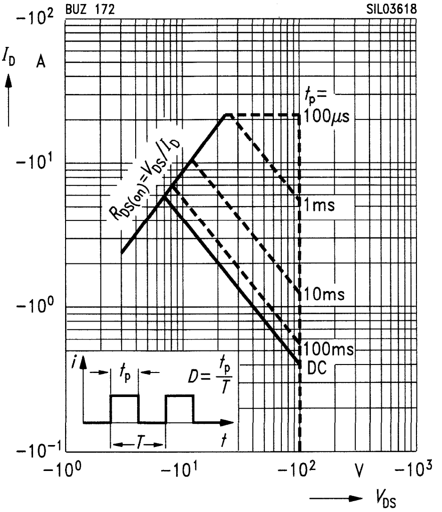
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

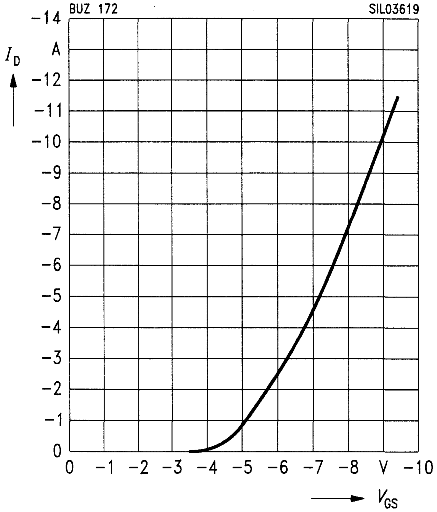
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

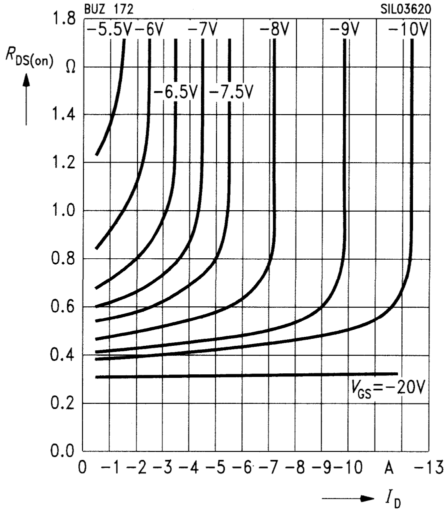
parameter: t_p = 80 µs, V_{DS} = – 25 V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

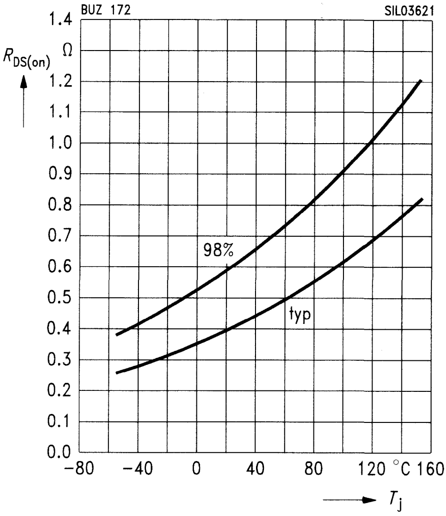
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

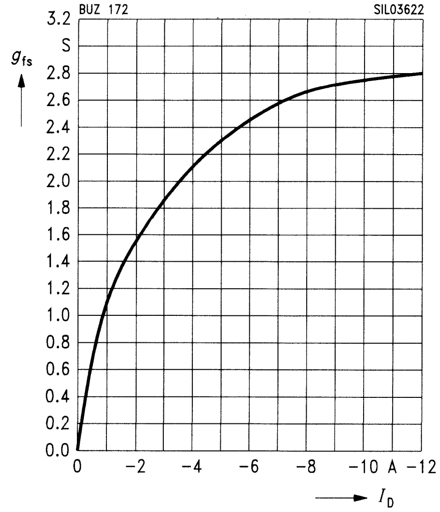
parameter: $I_D = -3.7$ A, $V_{GS} = -10$ V, (spread)



Typ. forward transconductance

$g_{fs} = f\,(I_D)$

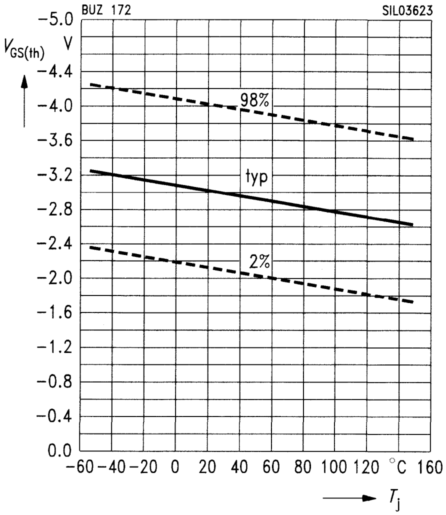
parameter: $t_p = 80$ µs



Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

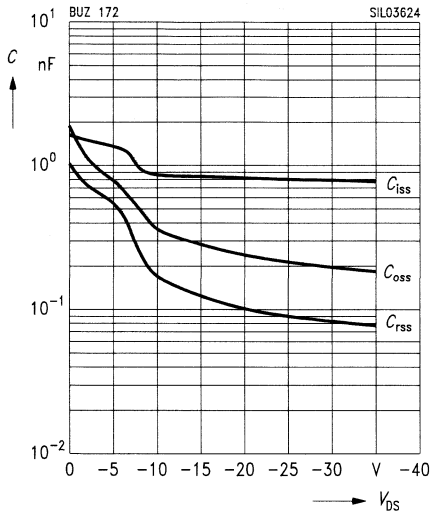
parameter: $V_{GS} = V_{DS}$, $I_D = -1$ mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

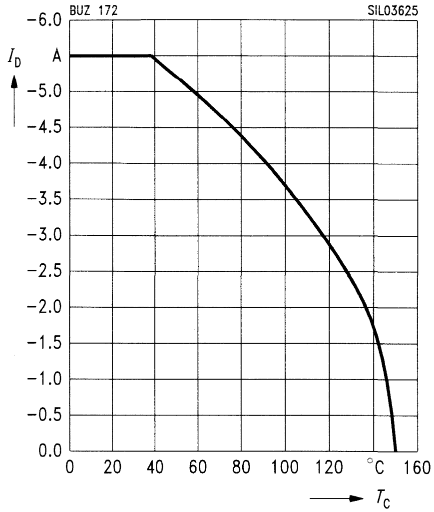
parameter: V_{GS} = 0 V, f = 1 MHz



Drain current

$I_D = f(T_C)$

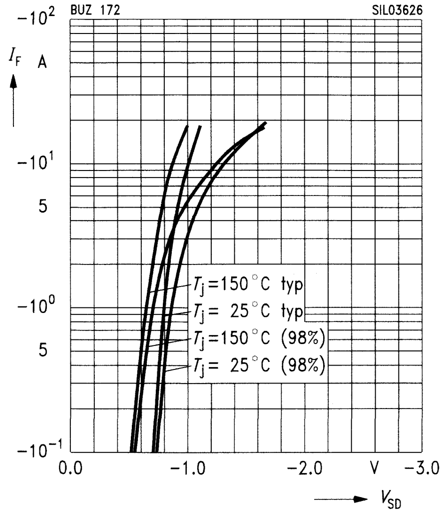
parameter: $V_{GS} \geq -10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

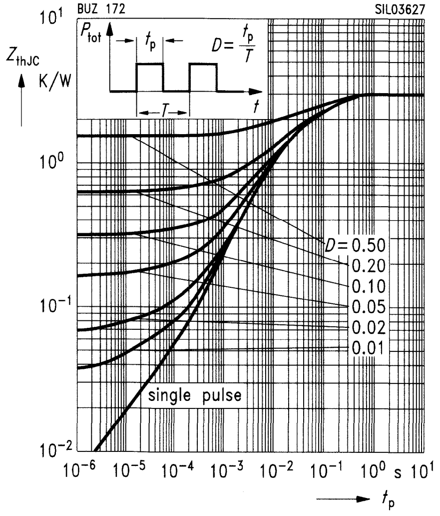
parameter: t_p = 80 µs, T_j



Transient thermal impedance

$Z_{thJC} = f(t_p)$

parameter: $D = t_p / T$

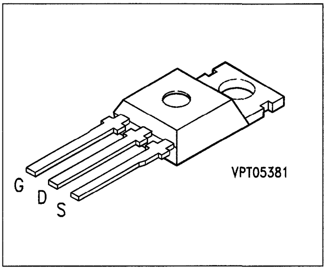


SIEMENS

SIPMOS® Power Transistor

BUZ 173

- P channel
- Enhancement mode
- Avalanche rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 173	– 200 V	– 3.6 A	1.5 Ω	TO-220 AB	C67078-A1452-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 30 ˚C	I_D	**– 3.6**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**– 14.0**	
Avalanche energy, single pulse V_{DD} = – 50 V, R_{GS} = 25 Ω, T_j = 25 ˚C I_D = – 3.6 A, L = 23 mH	E_{AS}	**200**	mJ
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 ˚C	P_{tot}	**40**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 3.1**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = – 0.25 mA	$V_{(BR)DSS}$	– 200	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = – 1 mA	$V_{GS(th)}$	– 2.1	– 3.0	– 4.0	
Zero gate voltage drain current V_{DS} = – 200 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 ˚C		–	– 20	– 250	
T_j = 125 ˚C		–	– 100	– 1000	
Gate-source leakage current V_{GS} = – 20 V, V_{DS} = 0 V	I_{GSS}	–	– 10	– 100	nA
Drain-source on-resistance V_{GS} = – 10 V, I_D = – 2.3 A	$R_{DS(on)}$	–	1.2	1.5	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = – 2.3 A	g_{fs}	1.1	2.2	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{iss}	–	750	1150	pF
Output capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{oss}	–	125	190	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{rss}	–	40	60	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = – 30 V, V_{GS} = – 10 V, I_D = – 2.6 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	20	30	ns
	t_r	–	60	95	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = – 30 V, V_{GS} = – 10 V, I_D = – 2.6 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	70	90	
	t_f	–	55	75	

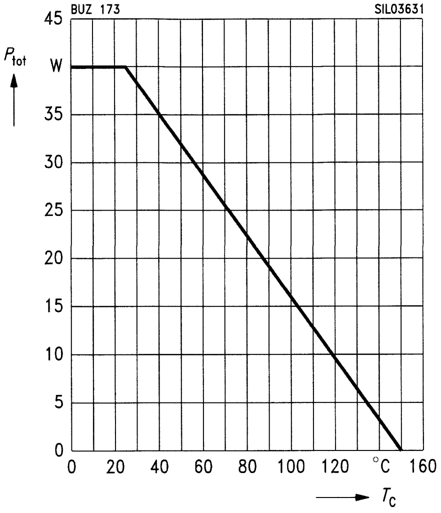
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	– 3.6	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	– 14.0	
Diode forward on-voltage I_S = – 7.2 A, V_{GS} = 0 V	V_{SD}	–	– 1.0	– 1.3	V
Reverse recovery time V_R = – 30 V, I_F = I_S, di_F / dt = – 100 A/µs	t_{rr}	–	200	–	ns
Reverse recovery charge V_R = – 30 V, I_F = I_S, di_F / dt = – 100 A/µs	Q_{rr}	–	0.75	–	µC

Characteristics at T_j = 25 ˚C, unless otherwise specified.

Total power dissipation

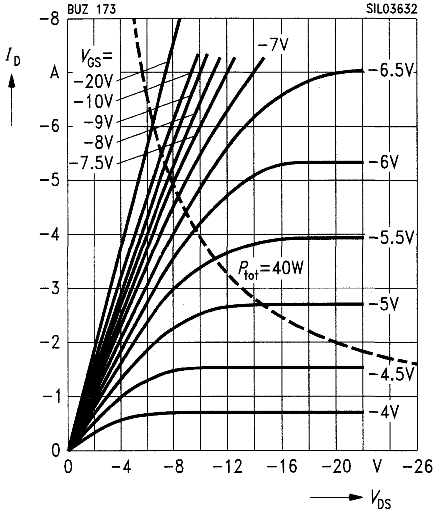
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

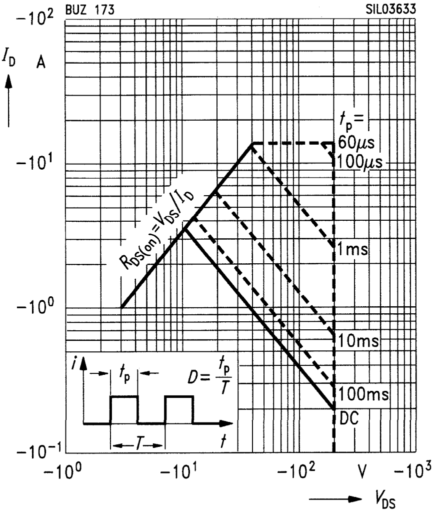
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

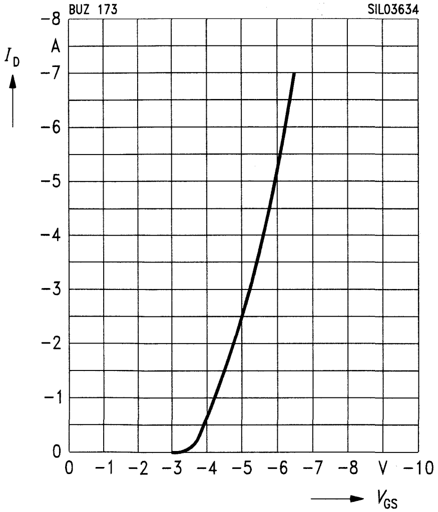
parameter: D = 0.01, T_C = 25 ˚C



Typ. transfer characteristics

$I_D = f(V_{GS})$

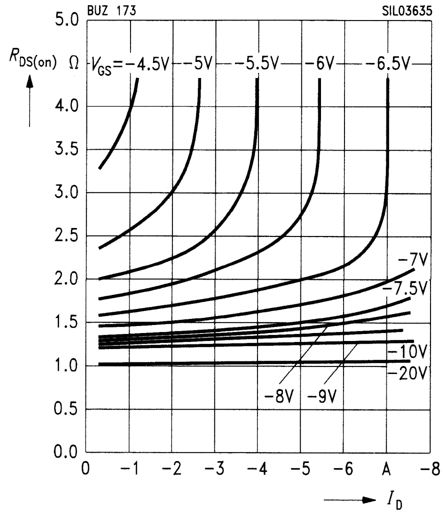
parameter: t_p = 80 µs, V_{DS} = – 25 V



Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$

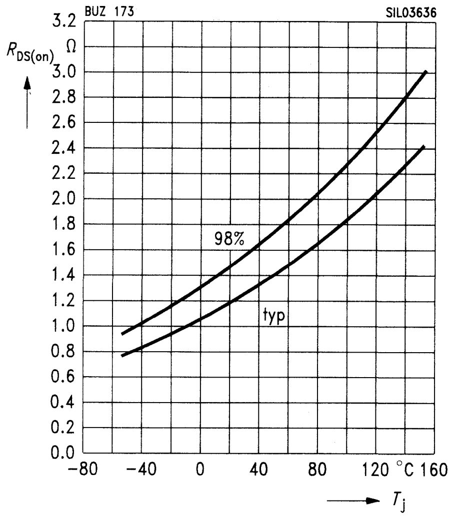
parameter: V_{GS}



Drain-source on-resistance

$R_{DS(on)} = f(T_j)$

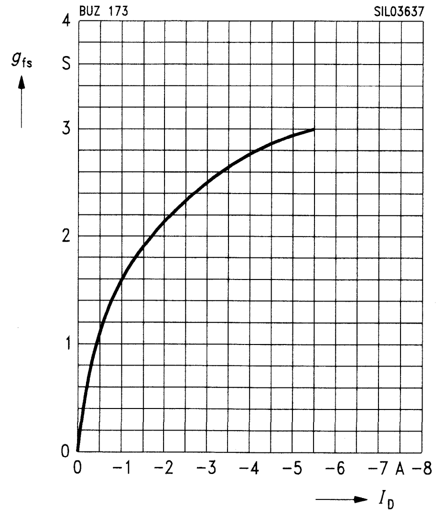
parameter: I_D = – 2.3 A, V_{GS} = – 10 V, (spread)



Typ. forward transconductance

$g_{fs} = f(I_D)$

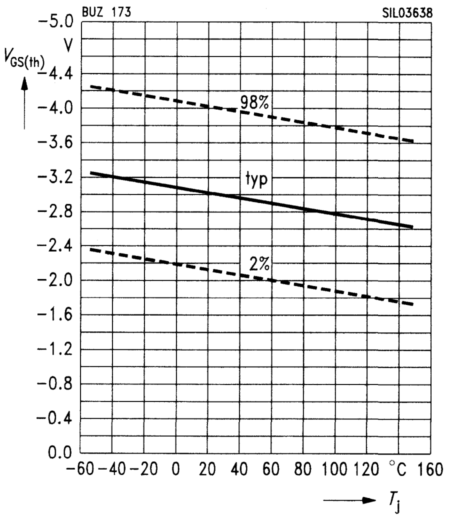
parameter: t_p = 80 µs



Gate threshold voltage

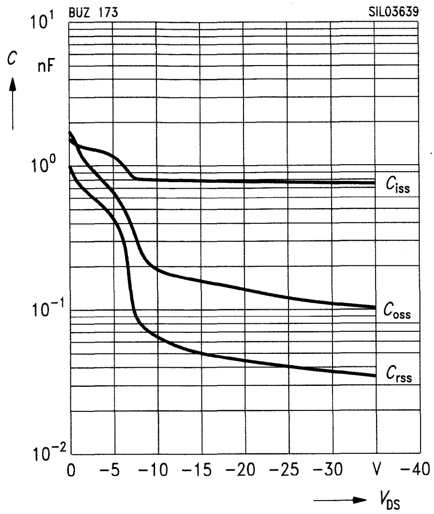
$V_{GS(th)} = f(T_j)$

parameter: $V_{GS} = V_{DS}$, I_D = – 1 mA, (spread)



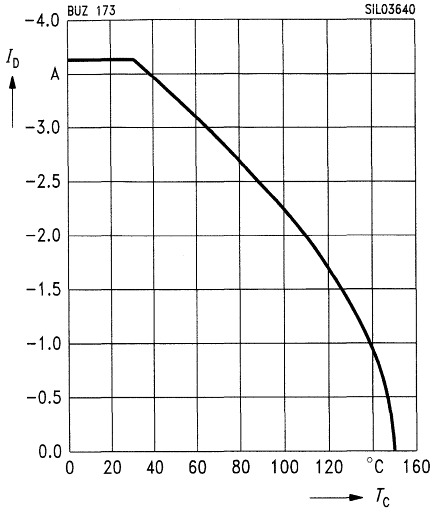
Typ. capacitances

$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



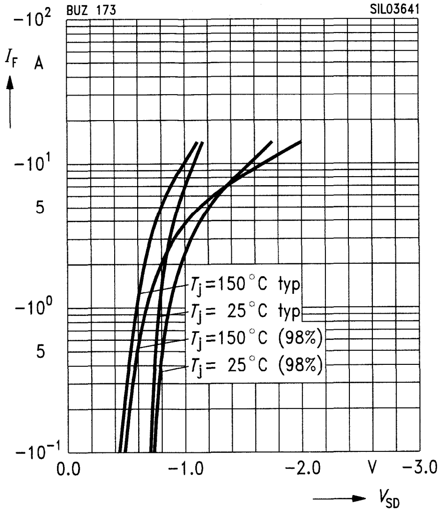
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq -10$ V



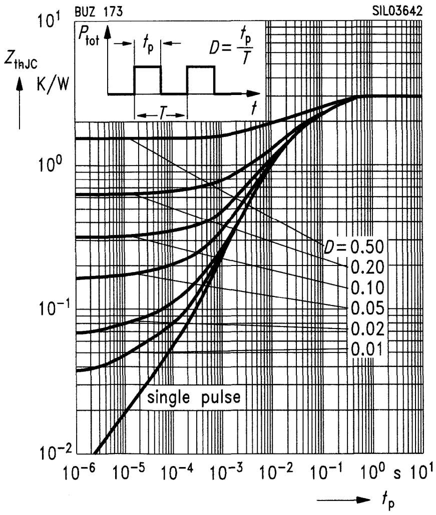
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: $t_p = 80$ µs, T_j



Transient thermal impedance

$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$

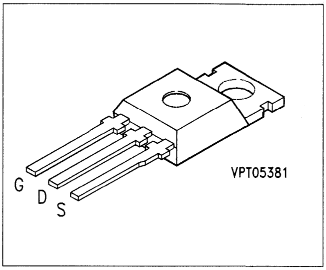


SIEMENS

SIPMOS® Power Transistor

BUZ 205

- N channel
- Enhancement mode
- FREDFET



Type	V_{DS}	I_D	$R_{DS(on)}$	**Package** [1]	**Ordering Code**
BUZ 205	400 V	6.0 A	1.0 Ω	TO-220 AB	C67078-A1401-A2

Maximum Ratings

Parameter	**Symbol**	**Values**	**Unit**
Continuous drain current, T_C = 35 °C	I_D	**6.0**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**24**	
Drain-source voltage	V_{DS}	**400**	V
Drain-gate voltage, R_{GS} = 20 kΩ	V_{DGR}	**400**	
Gate-source voltage	V_{GS}	**± 20**	
Power dissipation, T_C = 25 °C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

Static characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Drain-source breakdown voltage $V_{GS} = 0$ V, $I_D = 0.25$ mA	$V_{(BR)DSS}$	400	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, $I_D = 1$ mA	$V_{GS(th)}$	2.1	4.0	4.0	
Zero gate voltage drain current $V_{DS} = 400$ V, $V_{GS} = 0$ V	I_{DSS}				µA
T_j = 25 °C		–	20	250	
T_j = 125 °C		–	100	1000	
Gate-source leakage current $V_{GS} = 20$ V, $V_{DS} = 0$ V	I_{GSS}	–	10	100	nA
Drain-source on-resistance $V_{GS} = 10$ V, $I_D = 4.0$ A	$R_{DS(on)}$	–	0.9	1.0	Ω

Dynamic characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, $I_D = 4.0$ A	g_{fs}	1.7	2.9	–	S
Input capacitance $V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	C_{iss}	–	1500	2000	pF
Output capacitance $V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	C_{oss}	–	120	180	
Reverse transfer capacitance $V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	C_{rss}	–	35	60	
Turn-on time t_{on}, ($t_{on} = t_{d(on)} + t_r$) $V_{DD} = -30$ V, $V_{GS} = 10$ V, $I_D = 2.7$ A, $R_{GS} = 50\ \Omega$	$t_{d(on)}$	–	30	45	ns
	t_r	–	40	60	
Turn-off time t_{off}, ($t_{off} = t_{d(off)} + t_f$) $V_{DD} = -30$ V, $V_{GS} = 10$ V, $I_D = 2.7$ A, $R_{GS} = 50\ \Omega$	$t_{d(off)}$	–	110	140	
	t_f	–	50	65	

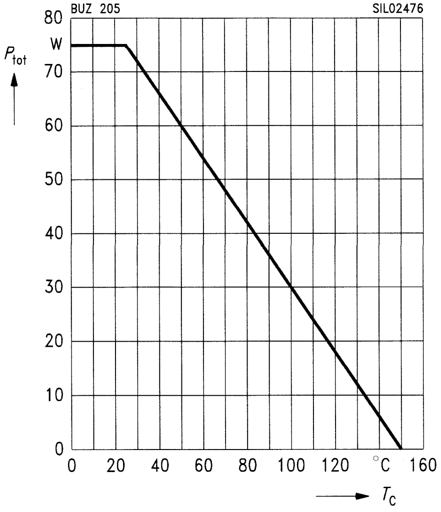
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	6.0	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	24	
Diode forward on-voltage I_S = 12 A, V_{GS} = 0 V	V_{SD}	–	1.3	1.6	V
Reverse recovery time V_R = 100 V, $I_F = I_{DR}$, di_F / dt = 100 A/µs	t_{rr}	–	180	250	ns
Reverse recovery charge V_R = 100 V, $I_F = I_{DR}$, di_F / dt = 100 A/µs	Q_{rr}	–	0.65	1.2	µC

Characteristics at T_j = 25 ˚C, unless otherwise specified.

Total power dissipation

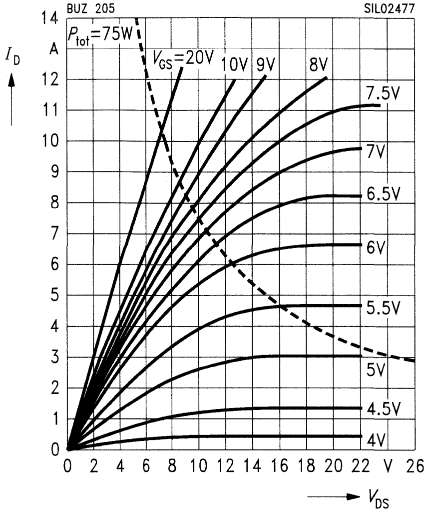
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

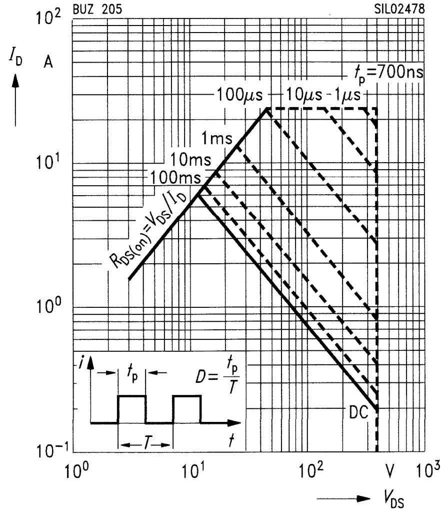
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

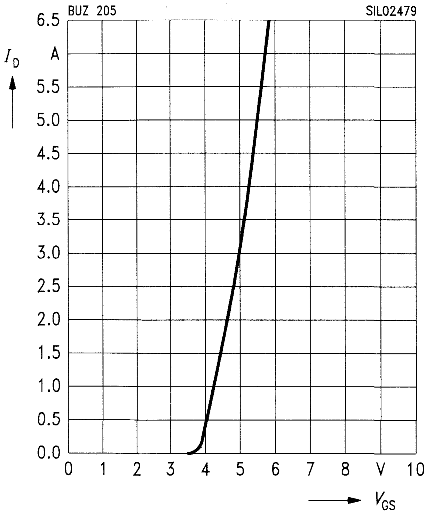
parameter: D = 0.01, T_C = 25 ˚C



Typ. transfer characteristics

$I_D = f(V_{GS})$

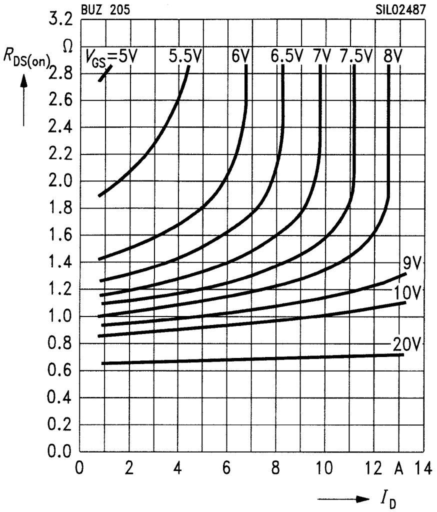
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$

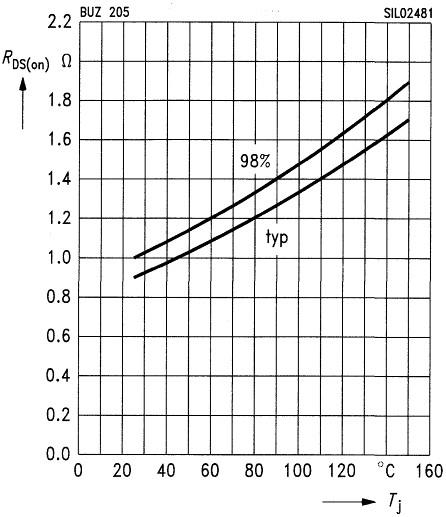
parameter: V_{GS}



Drain-source on-resistance

$R_{DS(on)} = f(T_j)$

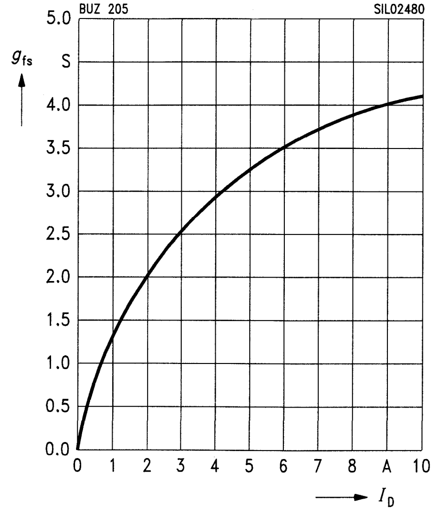
parameter: I_D = 4.0 A, V_{GS} = 10 V, (spread)



Typ. forward transconductance

$g_{fs} = f(I_D)$

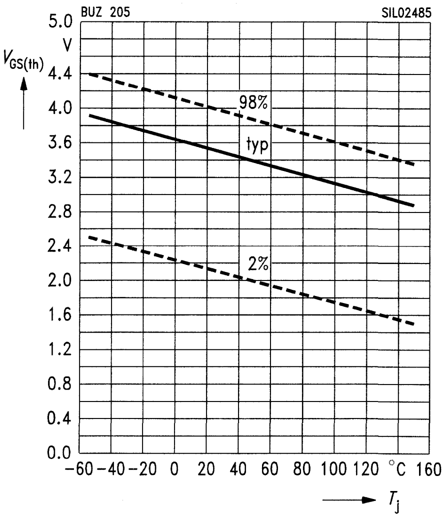
parameter: t_p = 80 µs



Gate threshold voltage

$V_{GS(th)} = f(T_j)$

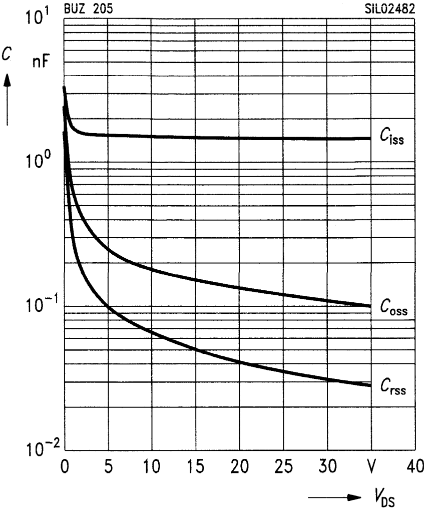
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

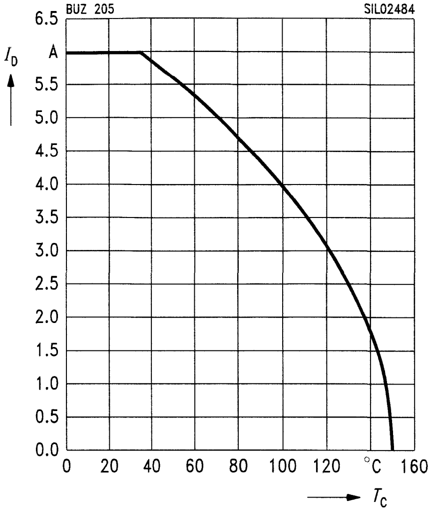
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

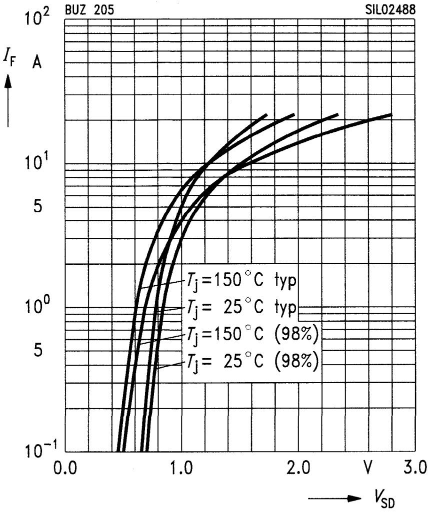
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

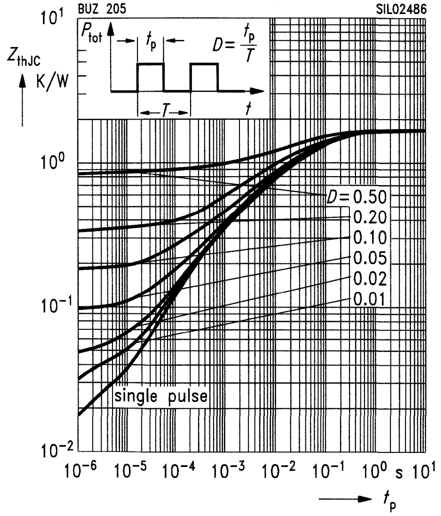
parameter: $t_p = 80$ µs, T_j



Transient thermal impedance

$Z_{thJC} = f(t_p)$

parameter: $D = t_p / T$

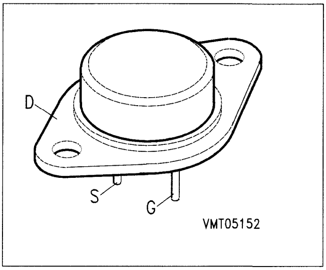


SIEMENS

SIPMOS® Power Transistors

BUZ 210
BUZ 211

- N channel
- Enhancement mode
- FREDFET



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 210	500 V	10.5 A	0.6 Ω	TO-204 AA	C67078-A1102-A2
BUZ 211	500 V	9.0 A	0.8 Ω	TO-204 AA	C67078-A1100-A2

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		210	211	
Continuous drain current, T_C = 25 ˚C	I_D	**10.5**	**9.0**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**42**	**36**	
Drain-source voltage	V_{DS}	**500**		V
Drain-gate voltage, R_{GS} = 20 kΩ	V_{DGR}	**500**		
Gate-source voltage	V_{GS}	**± 20**		
Power dissipation, T_C = 25 ˚C	P_{tot}	**125**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**C**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	500	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 500 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	20	250	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS(on)}$				Ω
V_{GS} = 10 V, I_D = 6.5 A BUZ 210		–	0.55	0.6	
BUZ 211		–	0.7	0.8	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 6.5 A	g_{fs}	2.7	5.3	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	3800	4900	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	250	400	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	100	170	
Turn-on time t_{on}, ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.8 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	50	75	ns
	t_r	–	80	120	
Turn-off time t_{off}, ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.8 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	330	430	
	t_f	–	110	140	

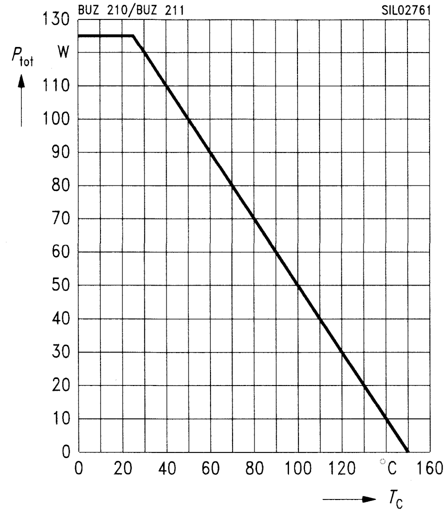
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Reverse diode					
Continuous reverse drain current T_C = 25 °C BUZ 210 BUZ 211	I_S	 – –	 – –	 10.5 9.0	A
Pulsed reverse drain current T_C = 25 °C BUZ 210 BUZ 211	I_{SM}	 – –	 – –	 42 36	
Diode forward on-voltage I_S = 21 A, V_{GS} = 0 V	V_{SD}	–	1.3	1.7	V
Reverse recovery time V_R = 100 V, I_F = I_S, di_F / dt = 100 A/µs	t_{rr}	–	180	250	ns
Reverse recovery charge V_R = 100 V, I_F = I_S, di_F / dt = 100 A/µs	Q_{rr}	–	0.65	1.2	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

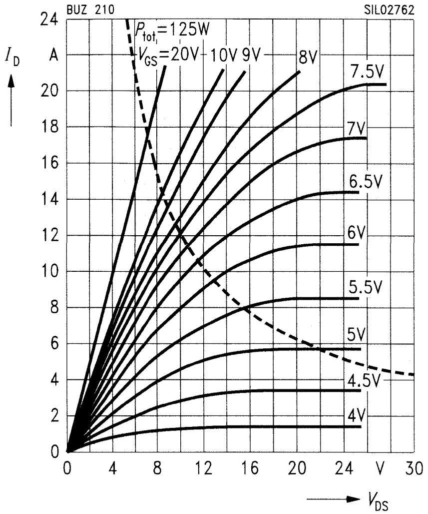
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 210**

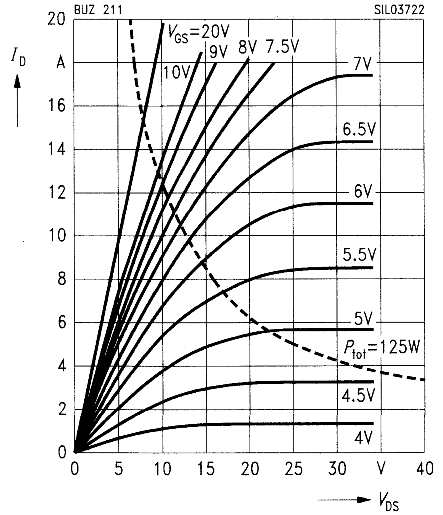
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 211**

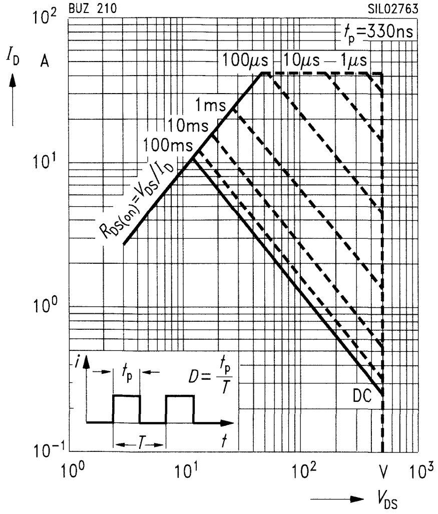
parameter: t_p = 80 µs



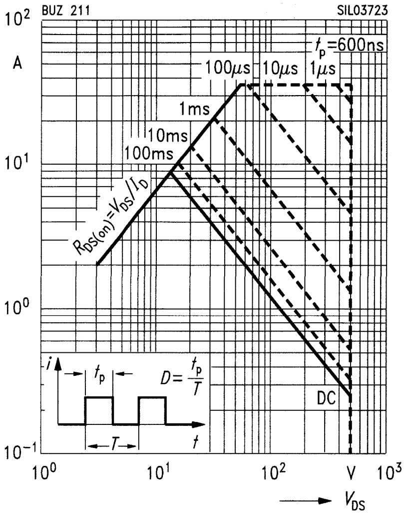
Safe operating area

$I_D = f(V_{DS})$ **BUZ 210**

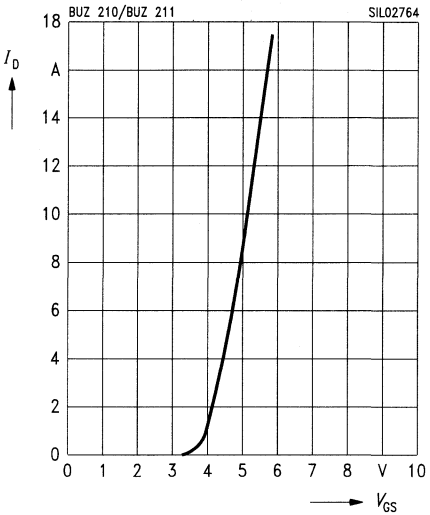
parameter: D = 0.01, T_C = 25 °C



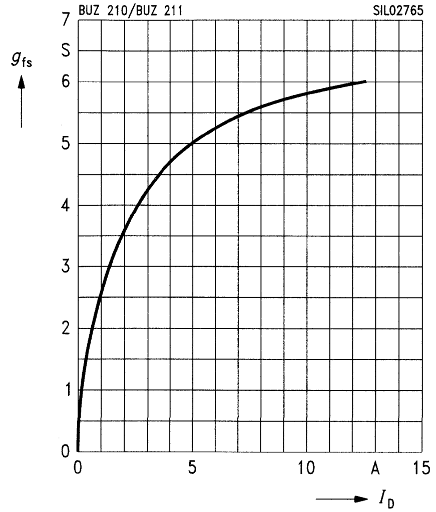
Safe operating area
$I_D = f(V_{DS})$ **BUZ 211**
parameter: $D = 0.01$, $T_C = 25$ °C



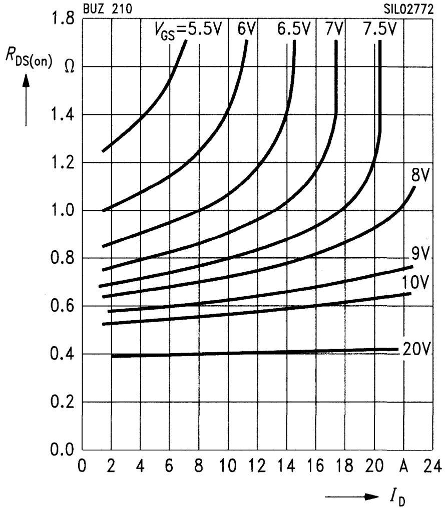
Typ. transfer characteristics
$I_D = f(V_{GS})$
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



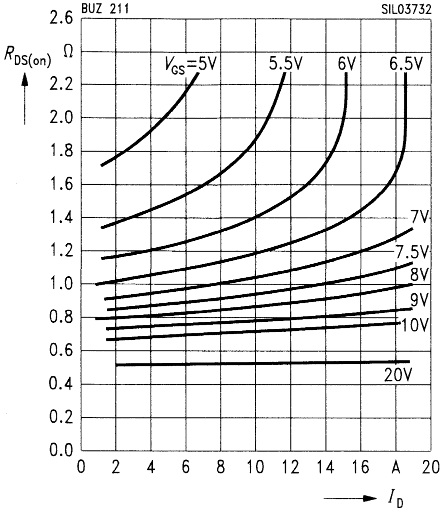
Typ. forward transconductance
$g_{fs} = f(I_D)$
parameter: $t_p = 80$ µs



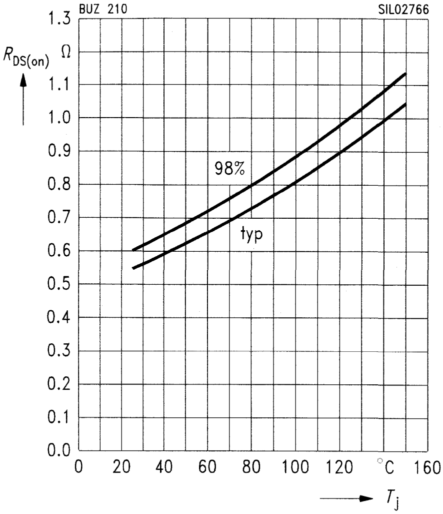
Typ. drain-source on-resistance
$R_{DS\,(on)} = f(I_D)$ **BUZ 210**
parameter: V_{GS}



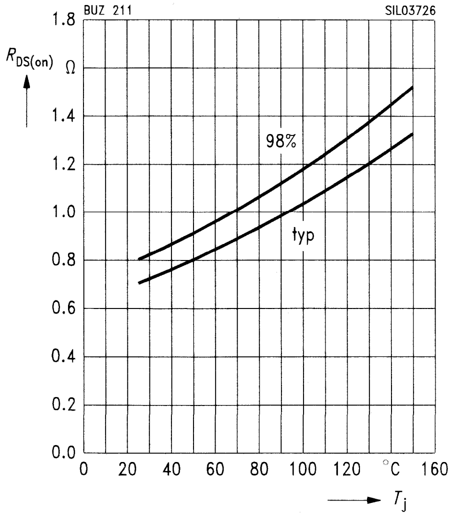
Typ. drain-source on-resistance
$R_{DS\,(on)} = f\,(I_D)$ **BUZ 211**
parameter: V_{GS}



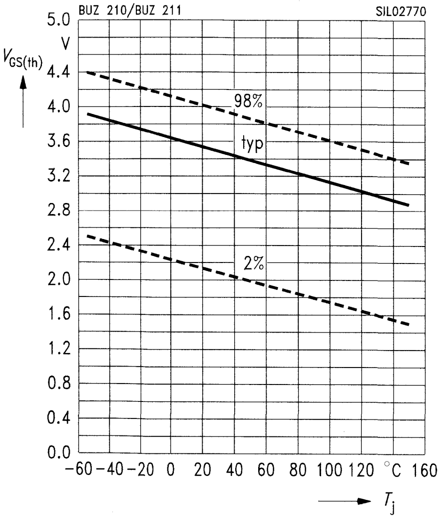
Drain-source on-resistance
$R_{DS\,(on)} = f\,(T_j)$ **BUZ 210**
parameter: I_D = 6.5 A, V_{GS} = 10 V, (spread)



Drain-source on-resistance
$R_{DS\,(on)} = f\,(T_j)$ **BUZ 211**
parameter: I_D = 6.5 A, V_{GS} = 10 V, (spread)



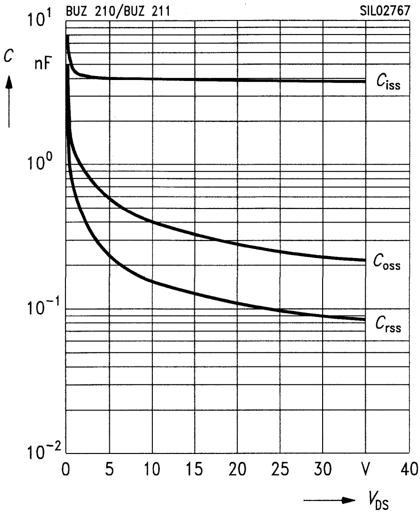
Gate threshold voltage
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA



Typ. capacitances

$C = f(V_{DS})$

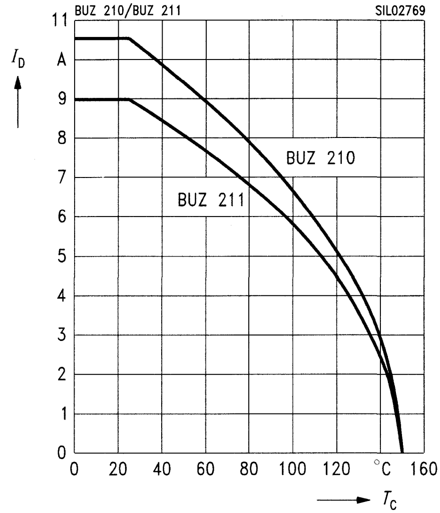
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

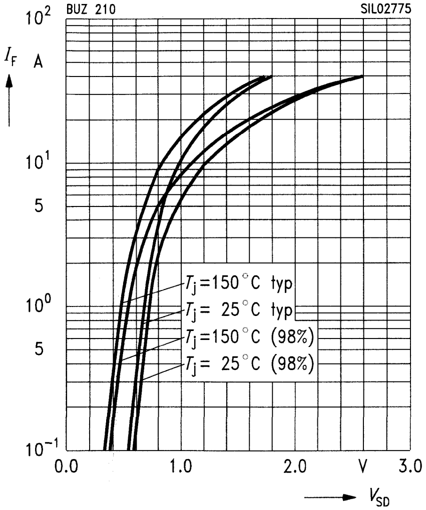
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

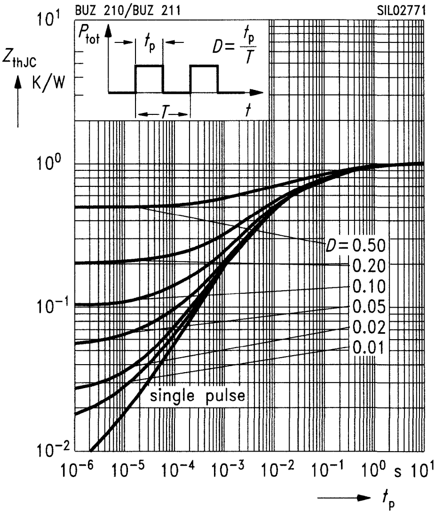
parameter: $t_p = 80$ µs, T_j



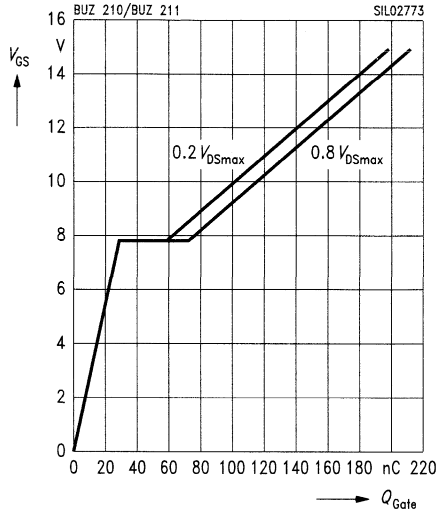
Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

parameter: $D = t_p / T$

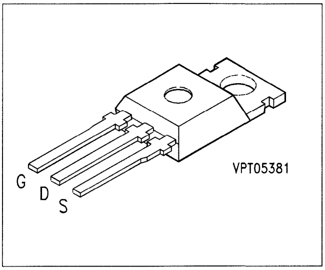


Typ. gate charge
$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls}$ = 14.4 A



SIPMOS® Power Transistor **BUZ 215**

- N channel
- Enhancement mode
- FREDFET



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 215	500 V	5.0 A	1.5 Ω	TO-220 AB	C67078-A1400-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 30 ˚C	I_D	**5.0**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**20**	
Drain-source voltage	V_{DS}	**500**	V
Drain-gate voltage, R_{GS} = 20 kΩ	V_{DGR}	**500**	
Gate-source voltage	V_{GS}	**± 20**	
Power dissipation, T_C = 25 ˚C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	500	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 500 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	20	250	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 3.2 A	$R_{DS\,(on)}$	–	1.4	1.5	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 3.2 A	g_{fs}	1.5	2.7	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1500	2000	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	110	170	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	40	70	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = – 30 V, V_{GS} = 10 V, I_D = 2.6 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	30	45	ns
	t_r	–	40	60	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = – 30 V, V_{GS} = 10 V, I_D = 2.6 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	110	140	
	t_f	–	50	65	

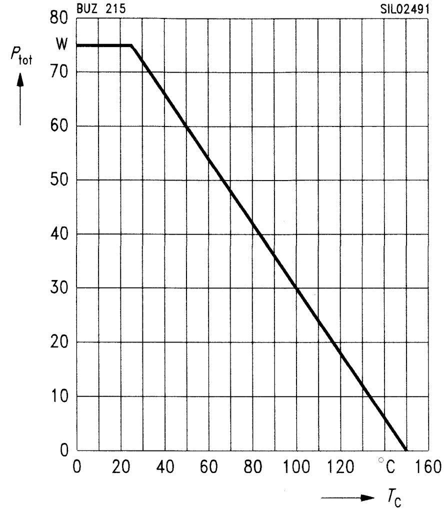
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	5.0	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	20	
Diode forward on-voltage I_S = 10 A, V_{GS} = 0 V	V_{SD}	–	1.3	1.6	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	180	250	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.65	1.2	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

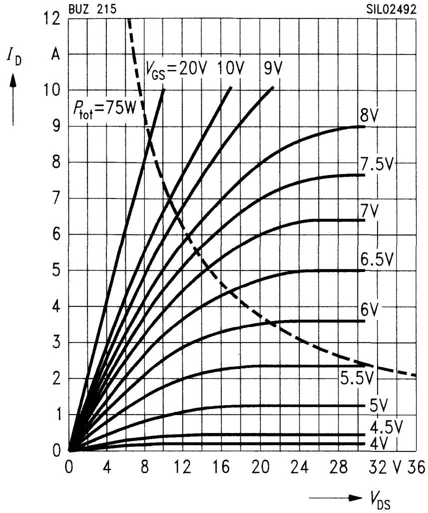
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

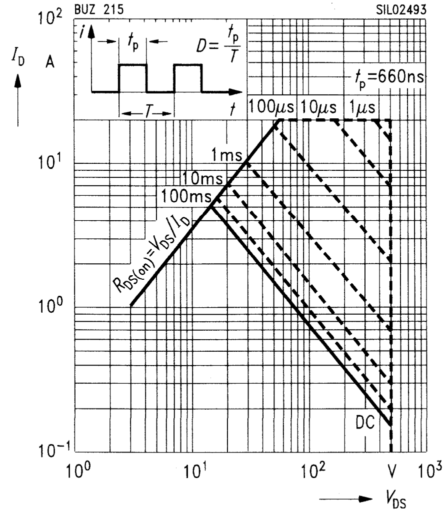
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

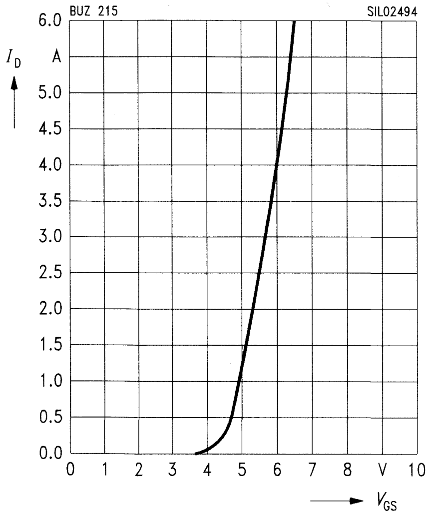
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

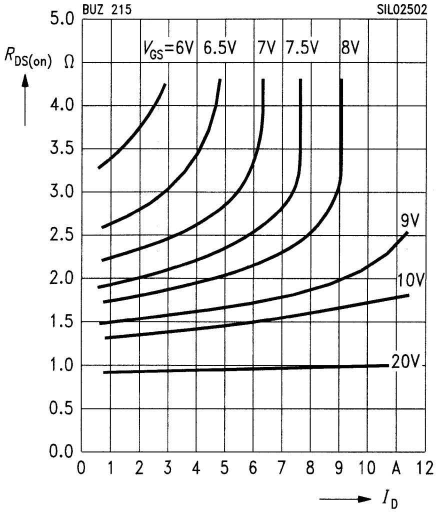
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



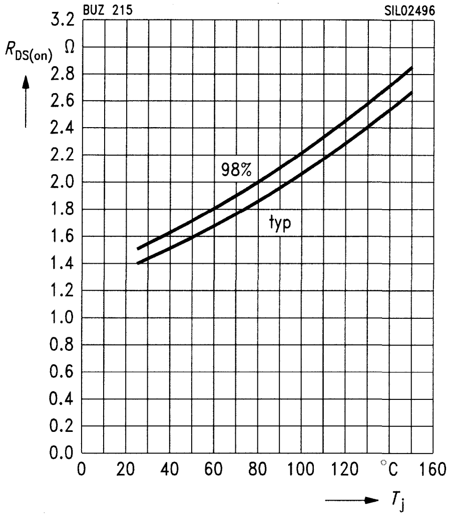
Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}



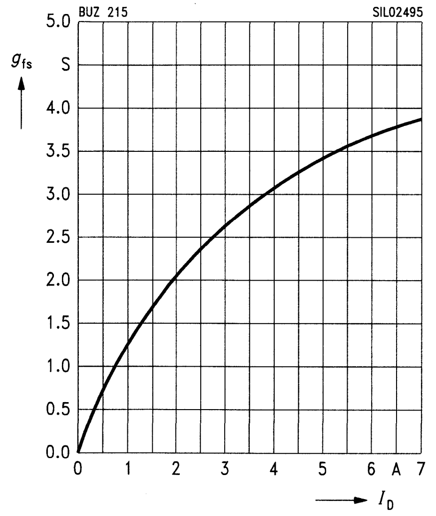
Drain-source on-resistance

$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 3.2 A, V_{GS} = 10 V, (spread)



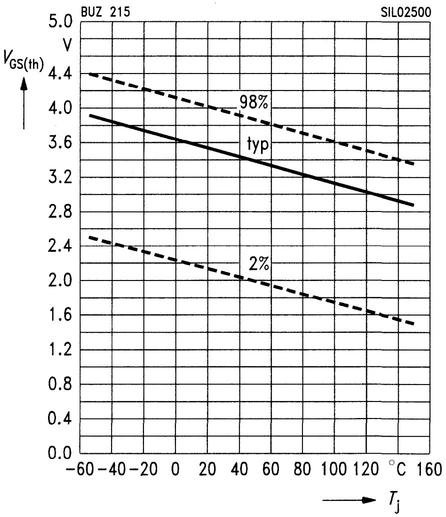
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

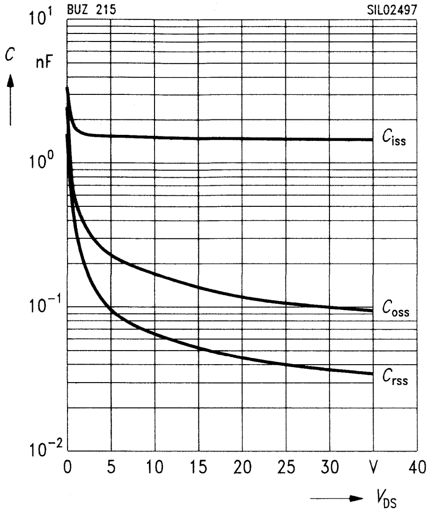
$V_{GS\,(th)} = f(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

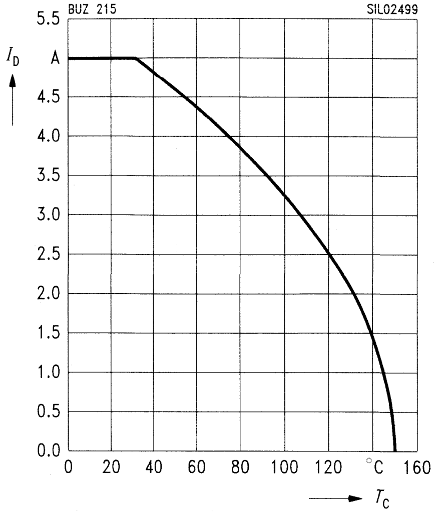
parameter: V_{GS} = 0 V, f = 1 MHz



Drain current

$I_D = f(T_C)$

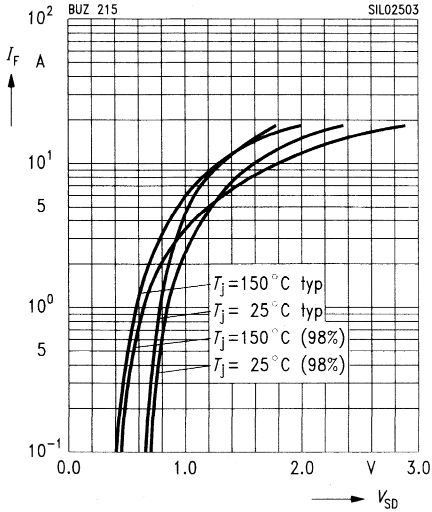
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

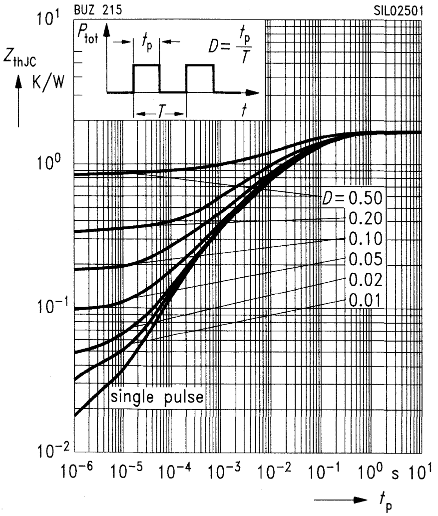
parameter: t_p = 80 µs, T_j



Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

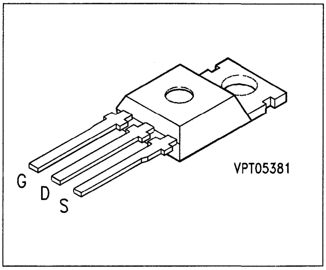
parameter: $D = t_p / T$



SIPMOS® Power Transistor

BUZ 255

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 255	250 V	13.0 A	0.24 Ω	TO-220 AB	C67078-S1406-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 31 ˚C	I_D	**13**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**52**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**13**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**9**	mJ
Avalanche energy, single pulse I_D = 13 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 1.89 mH, T_j = 25 ˚C	E_{AS}	**200**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 ˚C	P_{tot}	**95**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.32**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	250	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 250 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 8.5 A	$R_{DS(on)}$	–	0.22	0.24	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 8.5 A	g_{fs}	5.0	9.4	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	970	1300	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	165	250	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	85	130	
Turn-on time t_{on}, ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	15	25	ns
	t_r	–	60	90	
Turn-off time t_{off}, ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	160	250	
	t_f	–	60	80	

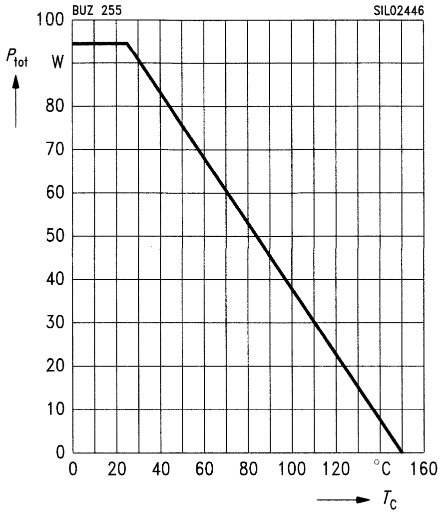
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	13.0	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	52	
Diode forward on-voltage I_S = 26 A, V_{GS} = 0 V	V_{SD}	–	1.3	1.6	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	180	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	1.2	–	µC

Characteristics at T_j = 25 ˚C, unless otherwise specified.

Total power dissipation

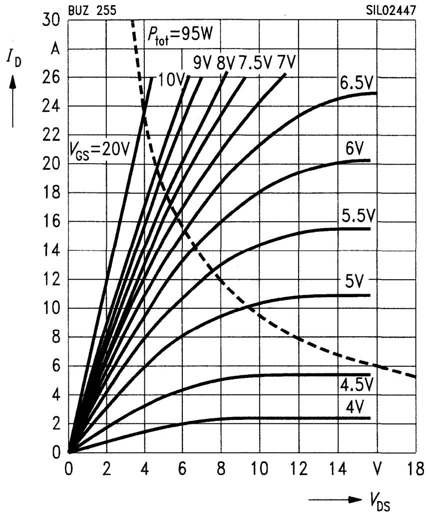
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

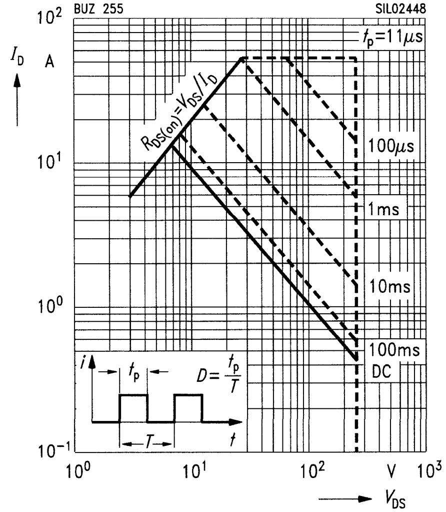
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

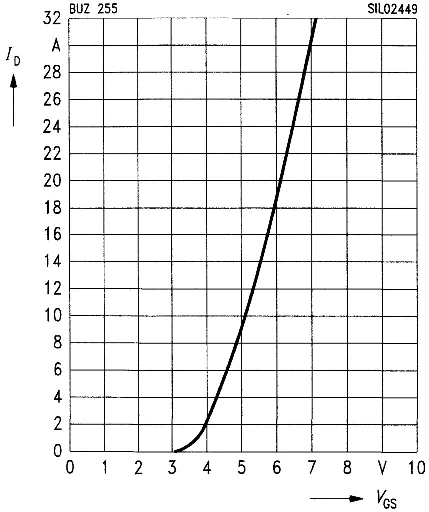
parameter: D = 0.01, T_C = 25 ˚C



Typ. transfer characteristics

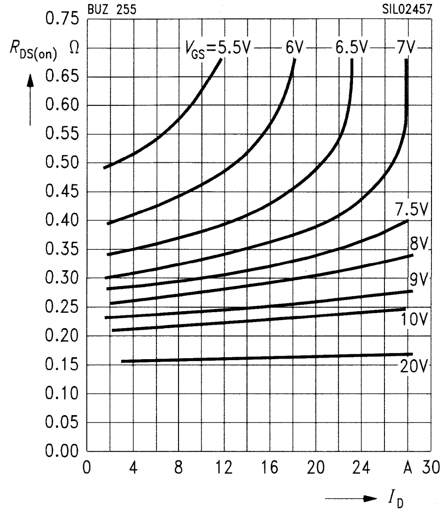
$I_D = f(V_{GS})$

parameter: t_p = 80 µs



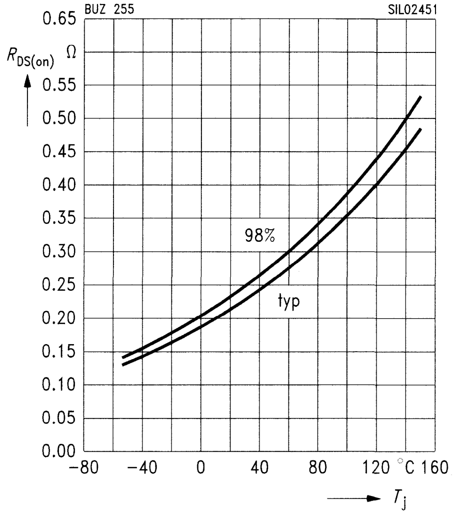
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



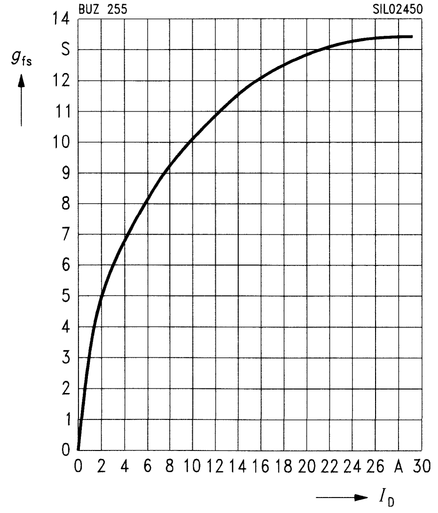
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 8.5 A, V_{GS} = 10 V, (spread)



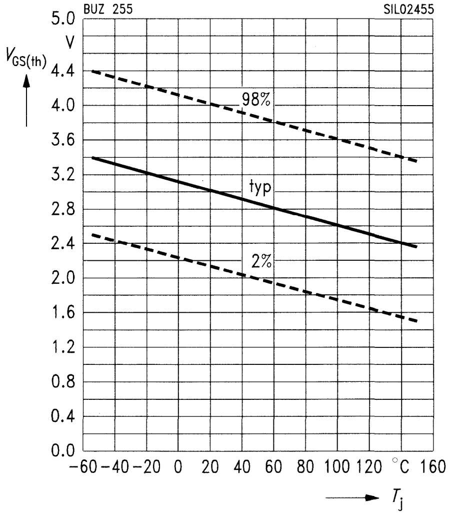
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

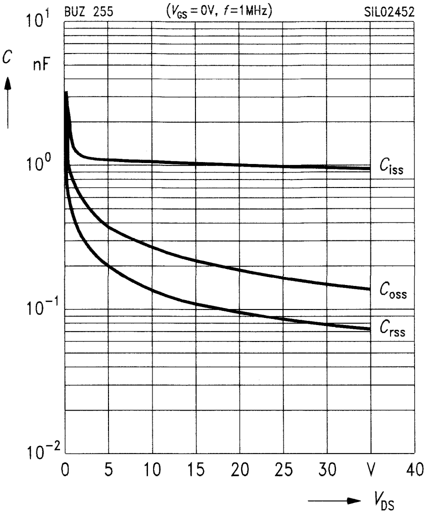
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

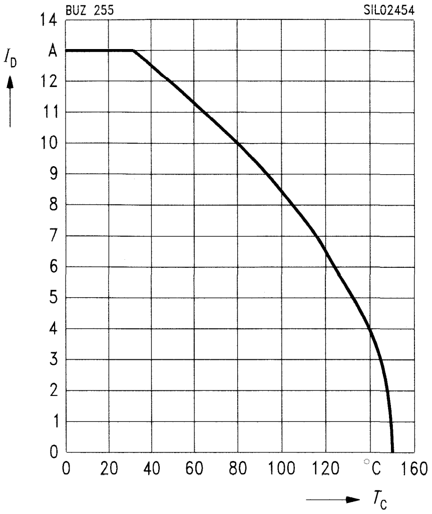
parameter: V_{GS} = 0 V, f = 1 MHz



Drain current

$I_D = f(T_C)$

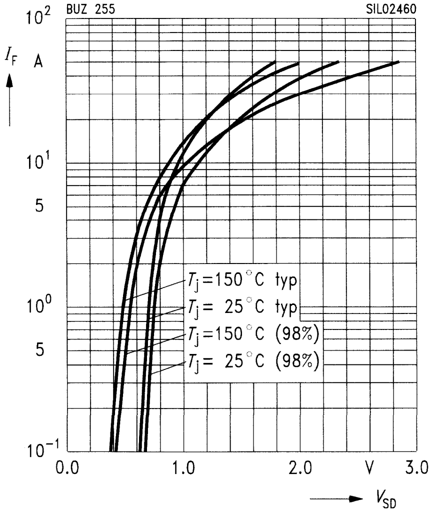
parameter: $V_{GS} \geq$ 10 V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

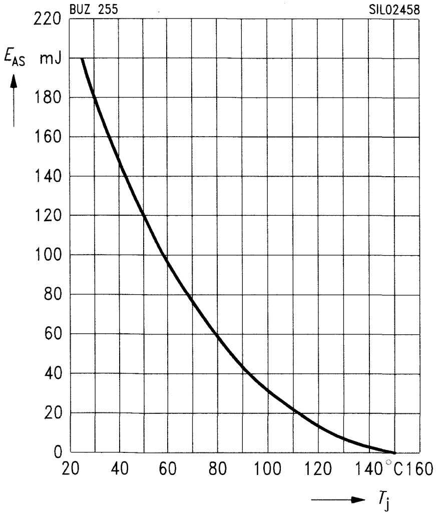
parameter: t_p = 80 µs, T_j



Avalanche energy $E_{AS} = f(T_j)$

parameter: I_D = 13 A, V_{DD} = 50 V

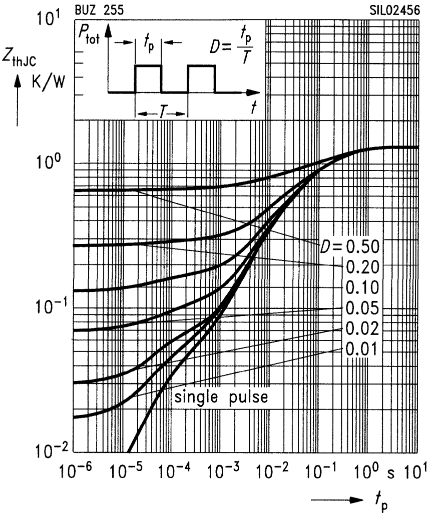
R_{GS} = 25 Ω, L = 1.89 mH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

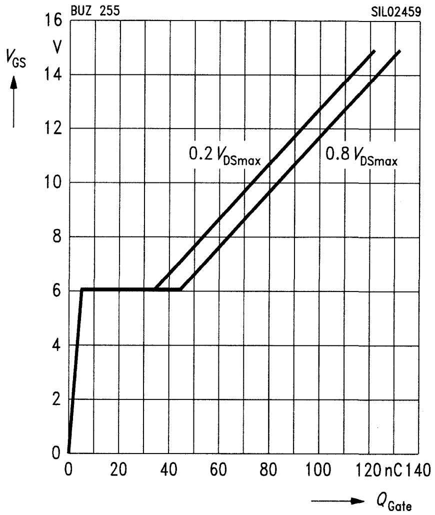
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{\text{Gate}})$

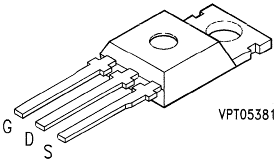
parameter: $I_{\text{D puls}} = 19.5$ A



SIEMENS

SIPMOS® Power Transistor **BUZ 271**

- P channel
- Enhancement mode
- Avalanche rated



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 271	– 50 V	– 22 A	0.15 Ω	TO-220 AB	C67078-S1453-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 26 °C	I_D	**– 22**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**– 88**	
Avalanche energy, single pulse I_D = – 22 A, V_{DD} = – 25 V, R_{GS} = 25 Ω L = 413 µH, T_j = 25 °C	E_{AS}	**200**	mJ
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

Static characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Drain-source breakdown voltage V_{GS} = 0 V, I_D = – 0.25 mA	$V_{(BR)\,DSS}$	– 50	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = – 1 mA	$V_{GS\,(th)}$	– 2.1	– 3.0	– 4.0	
Zero gate voltage drain current V_{DS} = – 50 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	– 0.1	– 1.0	
T_j = 125 °C		–	– 10	– 100	
Gate-source leakage current V_{GS} = – 20 V, V_{DS} = 0 V	I_{GSS}	–	– 10	– 100	nA
Drain-source on-resistance V_{GS} = – 10 V, I_D = – 14 A	$R_{DS\,(on)}$	–	0.12	0.15	Ω

Dynamic characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = – 14 A	g_{fs}	1.5	4.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{iss}	–	2000	2700	pF
Output capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{oss}	–	650	975	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{rss}	–	250	375	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = – 30 V, V_{GS} = – 10 V, I_D = – 2.95 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	30	45	ns
	t_r	–	120	180	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = – 30 V, V_{GS} = – 10 V, I_D = – 2.95 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	130	175	
	t_f	–	140	190	

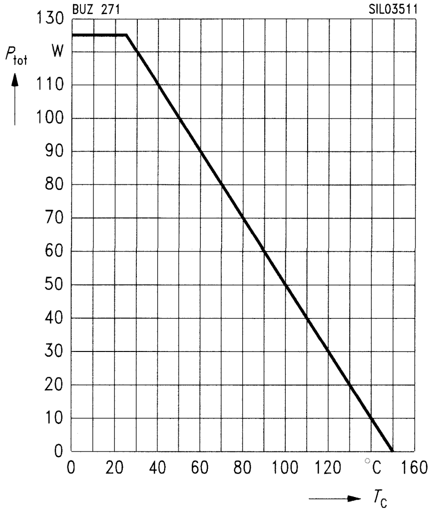
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	– 22	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	– 88	
Diode forward on-voltage I_S = – 44 A, V_{GS} = 0 V	V_{SD}	–	– 1.25	– 1.7	V
Reverse recovery time V_R = – 30 V, I_F = I_S , di_F / dt = – 100 A/µs	t_{rr}	–	90	–	ns
Reverse recovery charge V_R = – 30 V, I_F = I_S , di_F / dt = – 100 A/µs	Q_{rr}	–	0.23	–	µC

Characteristics at T_j = 25 ˚C, unless otherwise specified.

Total power dissipation

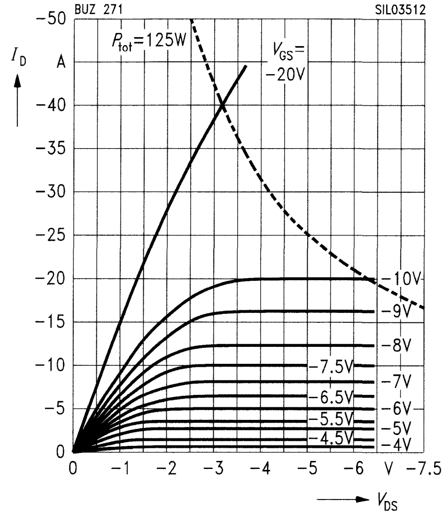
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

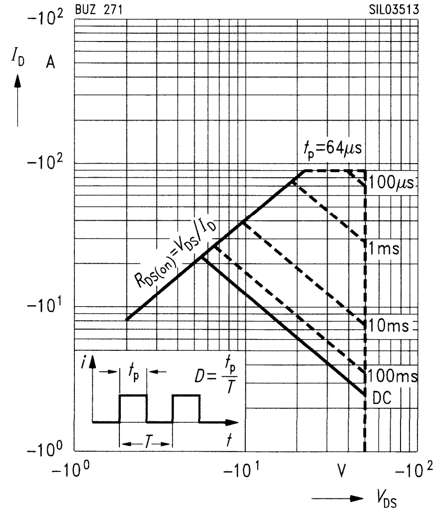
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

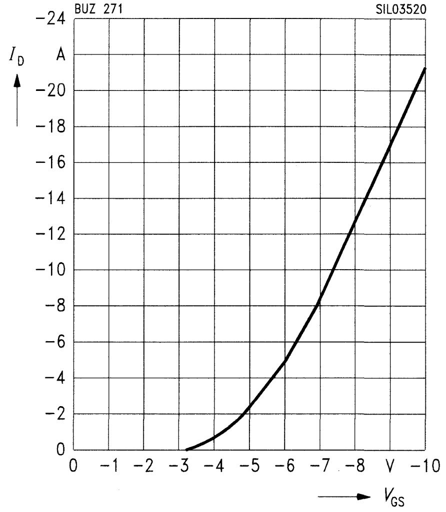
parameter: D = 0.01, T_C = 25 ˚C



Typ. transfer characteristics

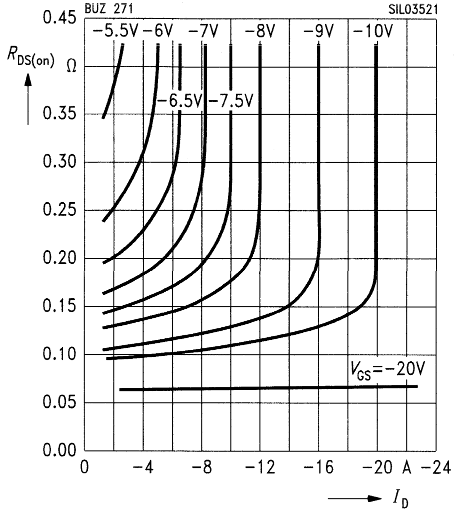
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = – 25 V



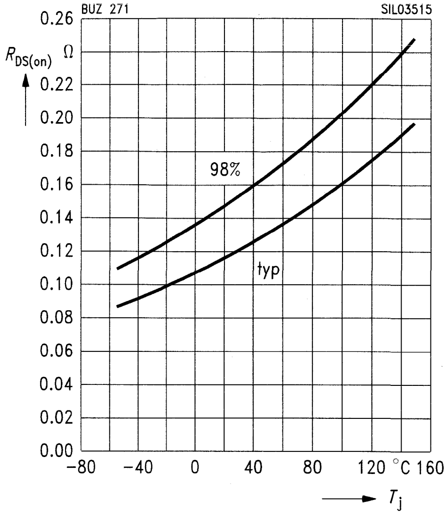
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



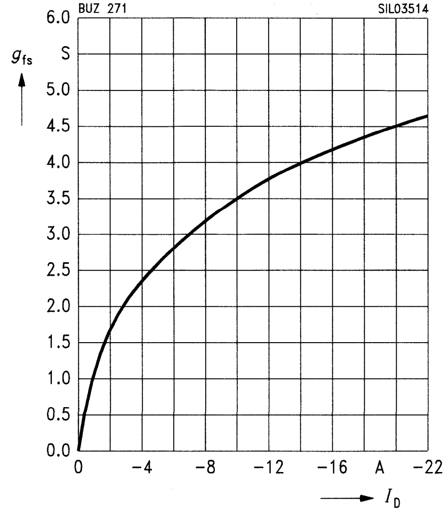
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 14 A, V_{GS} = – 10 V, (spread)



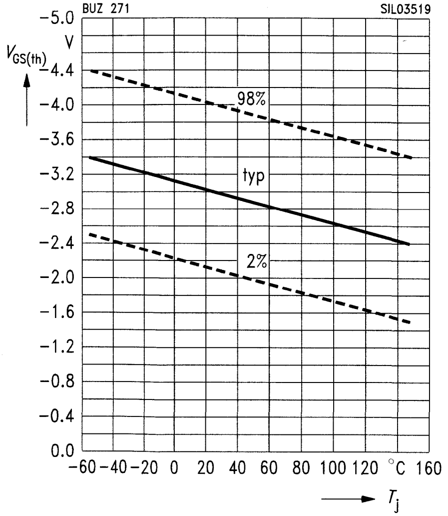
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

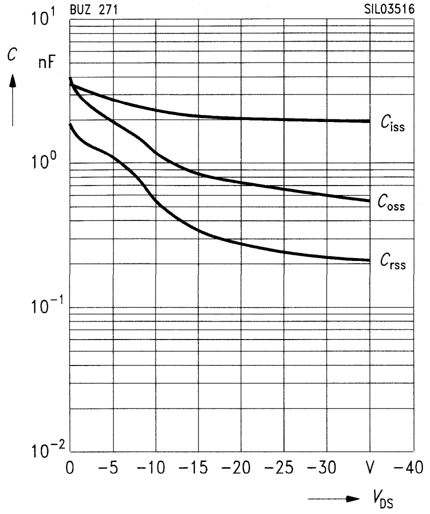
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = – 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

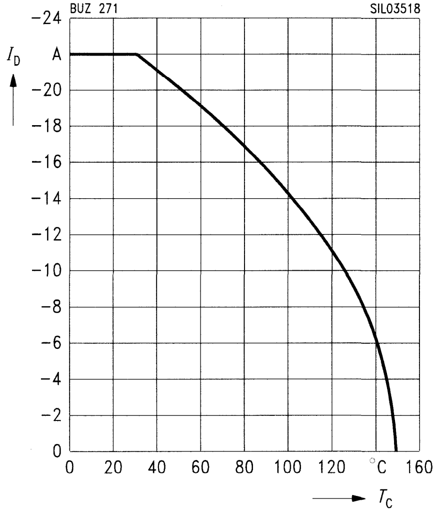
parameter: V_{GS} = 0 V, f = 1 MHz



Drain current

$I_D = f(T_C)$

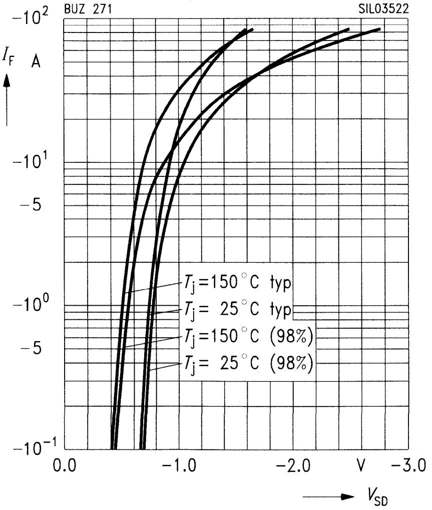
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

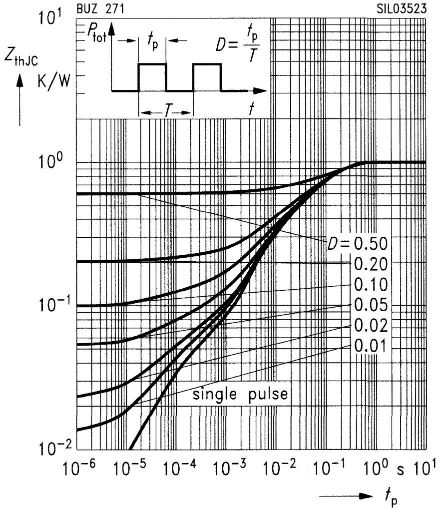
parameter: t_p = 80 µs, T_j



Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

parameter: $D = t_p / T$

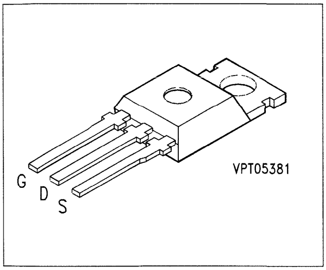


SIEMENS

SIPMOS® Power Transistor

BUZ 272

- P channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 272	– 100 V	– 15 A	0.3 Ω	TO-220 AB	C67078-S1454-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 25 °C	I_D	**– 15**	A
Pulsed drain current, T_C = 25 °C	$I_{D\ puls}$	**– 60**	
Avalanche energy, single pulse I_D = – 15 A, V_{DD} = – 25 V, R_{GS} = 25 Ω L = 1.93 mH, T_j = 25 °C	E_{AS}	**290**	mJ
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\ JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

Static characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Drain-source breakdown voltage V_{GS} = 0 V, I_D = – 0.25 mA	$V_{(BR)\,DSS}$	– 100	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = – 1 mA	$V_{GS\,(th)}$	– 2.1	– 3.0	– 4.0	
Zero gate voltage drain current V_{DS} = – 100 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 ˚C		–	– 0.1	– 1.0	
T_j = 125 ˚C		–	– 10	– 100	
Gate-source leakage current V_{GS} = – 20 V, V_{DS} = 0 V	I_{GSS}	–	– 10	– 100	nA
Drain-source on-resistance V_{GS} = – 10 V, I_D = – 9.5 A	$R_{DS\,(on)}$	–	– 0.2	0.3	Ω

Dynamic characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = – 9.5 A	g_{fs}	1.5	– 4.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{iss}	–	2000	2700	pF
Output capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{oss}	–	360	540	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = – 25 V, f = 1 MHz	C_{rss}	–	128	180	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = – 30 V, V_{GS} = – 10 V, I_D = – 2.9 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	30	45	ns
	t_r	–	120	180	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = – 30 V, V_{GS} = – 10 V, I_D = – 2.9 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	125	170	
	t_f	–	120	160	

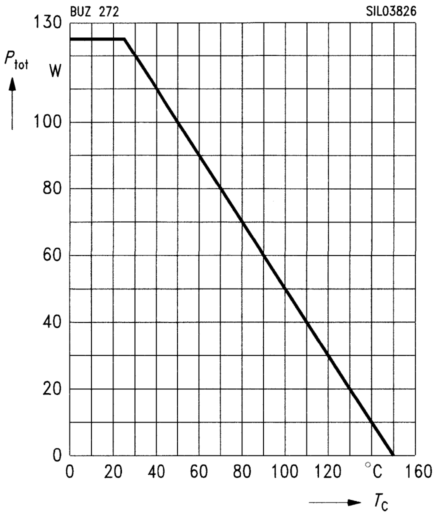
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	– 15	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	– 60	
Diode forward on-voltage I_S = – 30 A, V_{GS} = 0	V_{SD}	–	– 1.15	– 1.7	V
Reverse recovery time V_R = – 30 V, I_F = I_S , di_F / dt = – 100 A/µs	t_{rr}	–	–	–	ns
Reverse recovery charge V_R = – 30 V, I_F = I_S , di_F / dt = – 100 A/µs	Q_{rr}	–	–	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

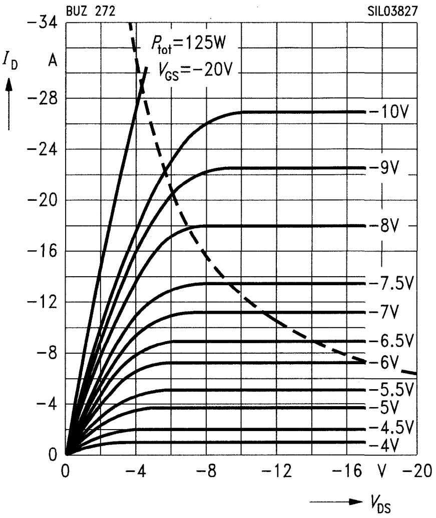
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

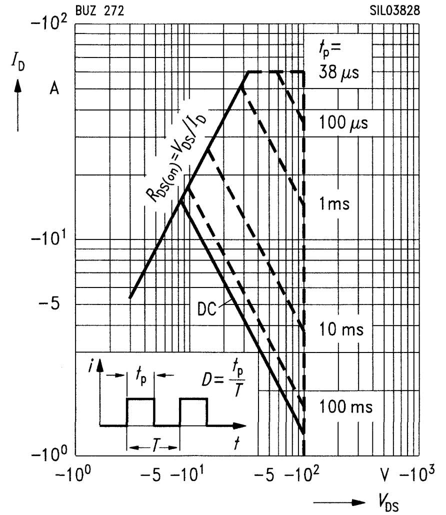
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

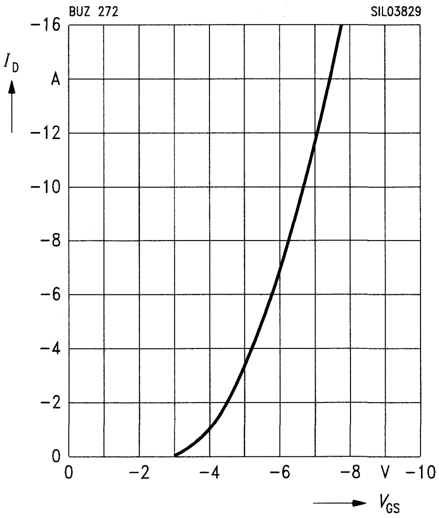
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

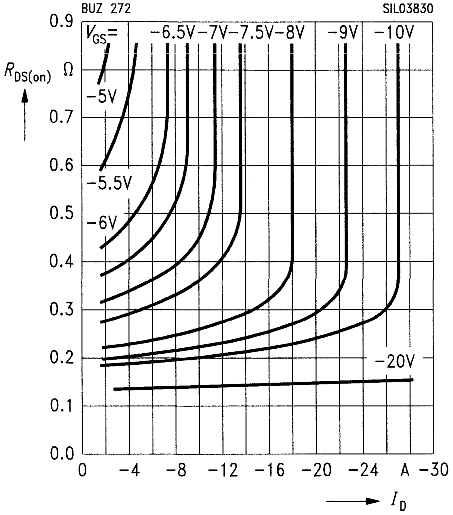
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = – 100 V



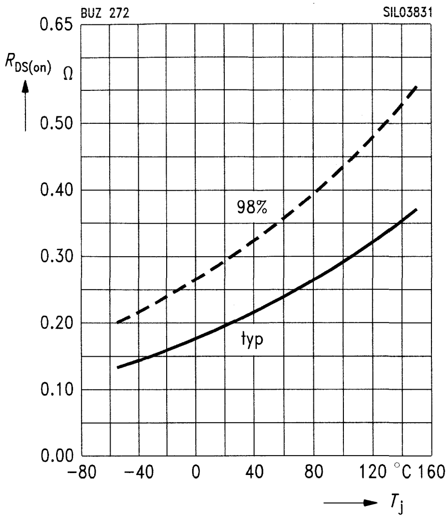
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



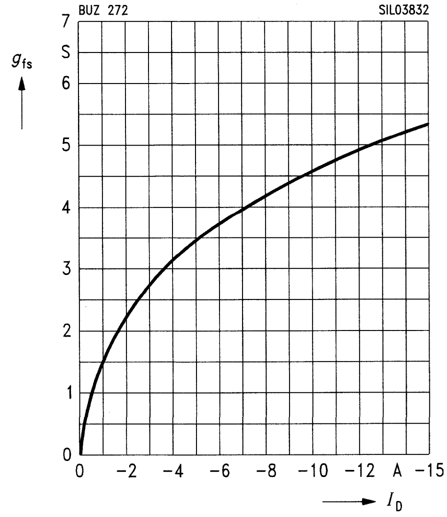
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: $I_D = -9.5$ A, $V_{GS} = -10$ V, (spread)



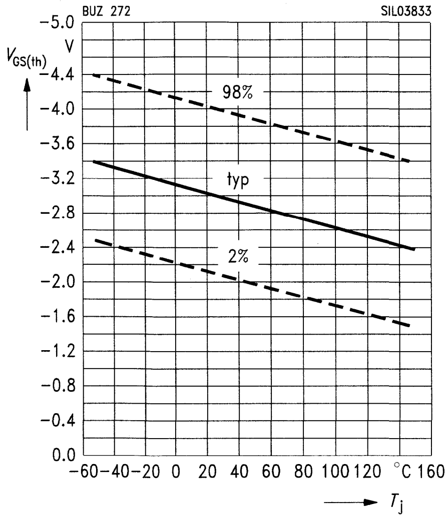
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

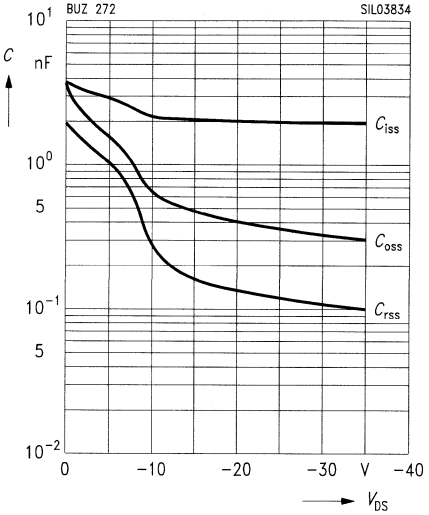
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, $I_D = -1$ mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

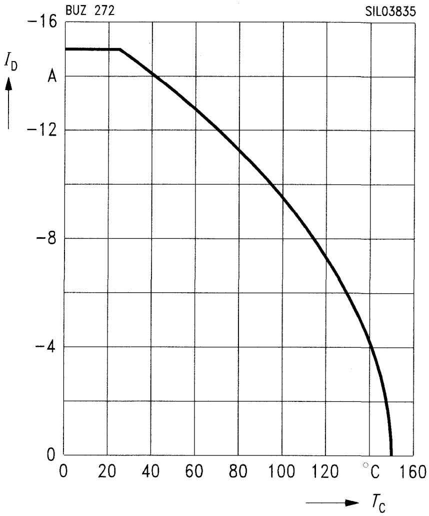
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

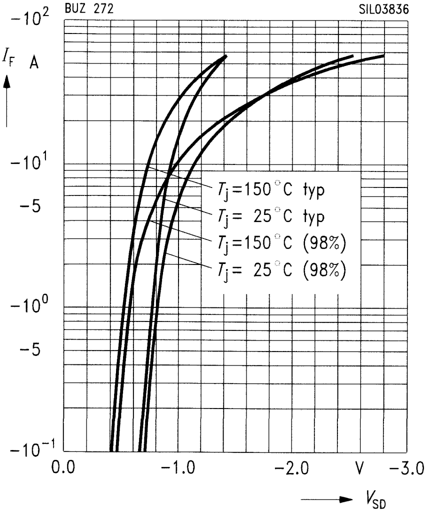
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

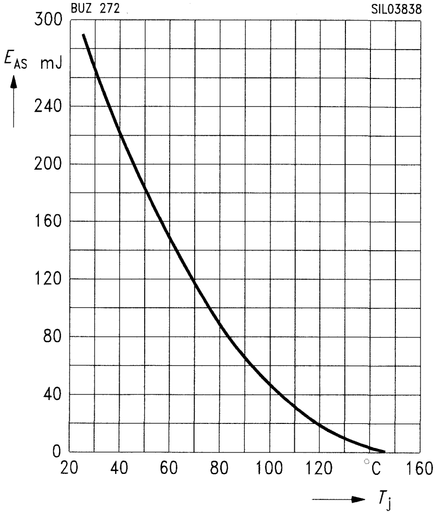
parameter: $t_p = 80$ µs, T_j



Avalanche energy $E_{AS} = f(T_j)$

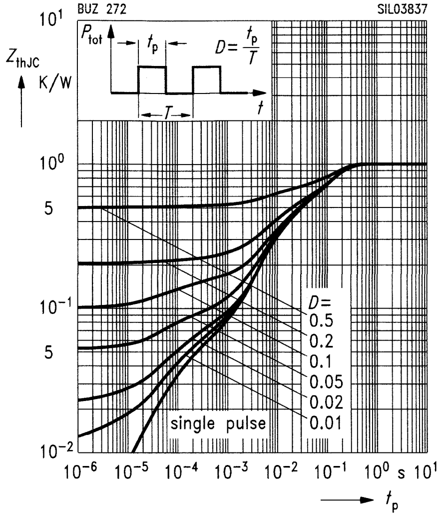
parameter: $I_D = -15$ A, $V_{DD} = -25$ V

$R_{GS} = 25\ \Omega$, $L = 1.93$ mH



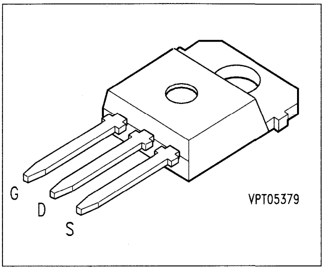
Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$



SIPMOS® Power Transistor **BUZ 305**

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS(on)}$	**Package** 1)	**Ordering Code**
BUZ 305	800 V	7.5 A	1.0 Ω	TO-218 AA	C67078-S3134-A2

Maximum Ratings

Parameter	**Symbol**	**Values**	**Unit**
Continuous drain current, $T_C = 31$ °C	I_D	**7.5**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**30**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**9.0**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**16**	mJ
Avalanche energy, single pulse $I_D = 7.5$ A, $V_{DD} = 50$ V, $R_{GS} = 25$ Ω $L = 27.7$ mH, $T_j = 25$ °C	E_{AS}	**830**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, $T_C = 25$ °C	P_{tot}	**150**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 0.83**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\ DSS}$	800	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\ (th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 800 V, V_{GS} = 0 V T_j = 25 °C T_j = 125 °C	I_{DSS}	 – –	 0.1 10	 1.0 100	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 5.0 A	$R_{DS\ (on)}$	–	–	1.0	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 5.0 A	g_{fs}	2.5	–	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1700	2200	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	170	300	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	80	140	
Turn-on time t_{on} , ($t_{on} = t_{d\ (on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d\ (on)}$	–	30	45	ns
	t_r	–	100	160	
Turn-off time t_{off} , ($t_{off} = t_{d\ (off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d\ (off)}$	–	400	520	
	t_f	–	130	170	

Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

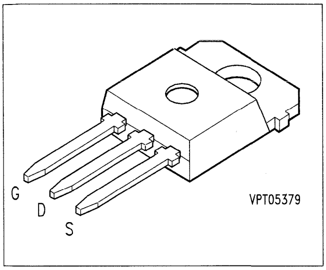
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	7.5	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	30	
Diode forward on-voltage I_S = 15 A, V_{GS} = 0 V	V_{SD}	–	–	1.4	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	–	–	µs
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	–	–	µC

SIEMENS

SIPMOS® Power Transistors

BUZ 307
BUZ 308

- N channel
- Enhancement mode



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 307	800 V	3.0 A	3.0 Ω	TO-218 AA	C67078-A3100-A2
BUZ 308	800 V	2.6 A	4.0 Ω	TO-218 AA	C67078-A3109-A2

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		307	308	
Continuous drain current, T_C = 50 °C	I_D	**3.0**	**2.6**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**10**		
Drain-source voltage	V_{DS}	**800**		V
Drain-gate voltage, R_{GS} = 20 kΩ	V_{DGR}	**800**		
Gate-source voltage	V_{GS}	**± 20**		
Power dissipation, T_C = 25 °C	P_{tot}	**75**		W
Operating and storage temperature range	T_j, T_{stg}	**– 55 ... + 150**		°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	800	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 800 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	20	250	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS\,(on)}$				Ω
V_{GS} = 10 V, I_D = 1.5 A BUZ 307		–	2.7	3.0	
BUZ 308		–	3.5	4.0	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 1.5 A	g_{fs}	1.0	1.8	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1600	2100	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	90	150	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	30	55	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	30	45	ns
	t_r	–	40	60	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	110	140	
	t_f	–	60	80	

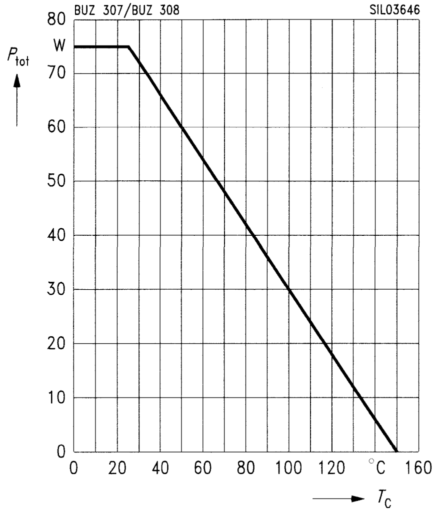
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter		**Symbol**	**Values**			**Unit**
			min.	**typ.**	**max.**	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 °C	BUZ 307		–	–	3.0	
	BUZ 308		–	–	2.6	
Pulsed reverse drain current		I_{SM}				
T_C = 25 °C	BUZ 307		–	–	12	
	BUZ 308		–	–	10	
Diode forward on-voltage I_S = 6.0 A, V_{GS} = 0 V		V_{SD}	–	1.05	1.3	V
Reverse recovery time V_R = 100 V, I_F = I_S , di_F / dt = 100 A/µs		t_{rr}	–	1.8	–	µs
Reverse recovery charge V_R = 100 V, I_F = I_S , di_F / dt = 100 A/µs		Q_{rr}	–	12	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Total power dissipation

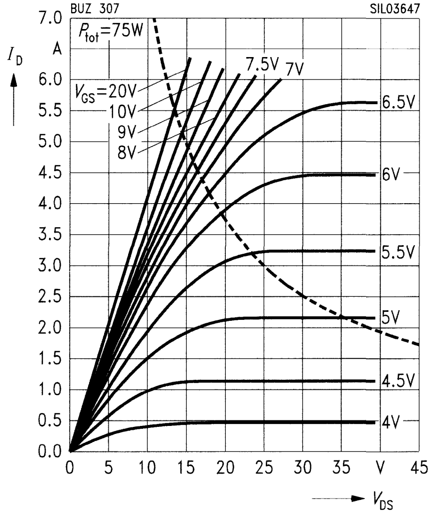
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 307**

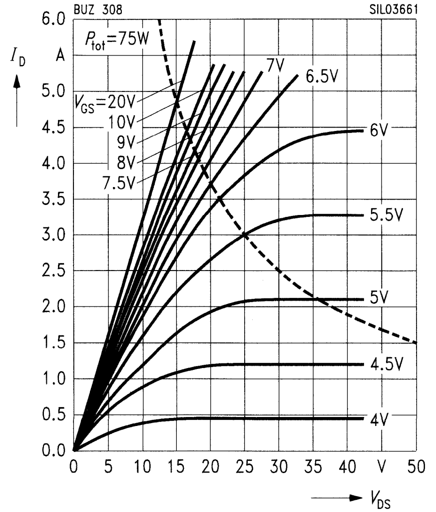
parameter: $t_p = 80$ µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 308**

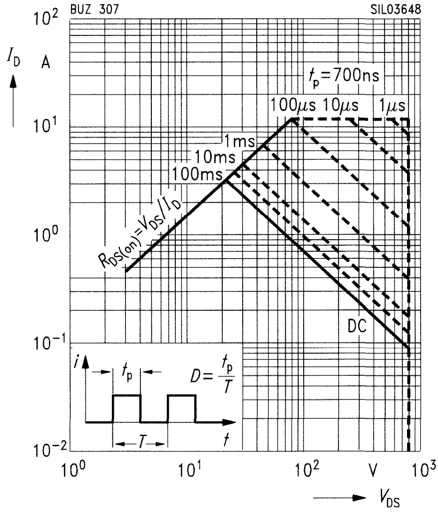
parameter: $t_p = 80$ µs



Safe operating area

$I_D = f(V_{DS})$ **BUZ 307**

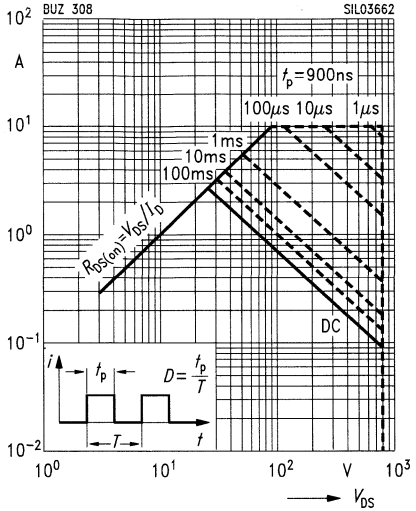
parameter: $D = 0.01$, $T_C = 25$ °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 308**

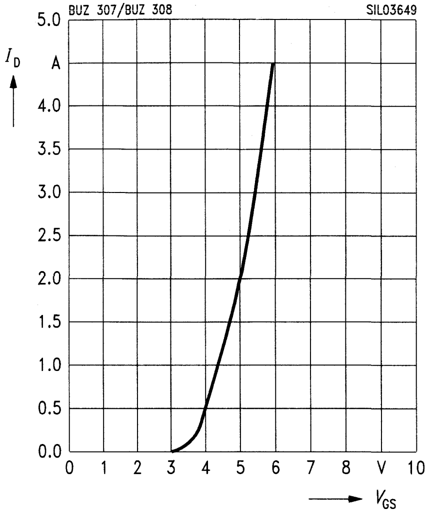
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

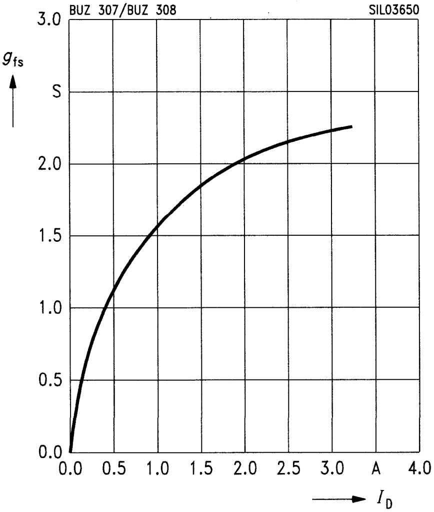
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



Typ.forward transconductance

$g_{fs} = f(I_D)$

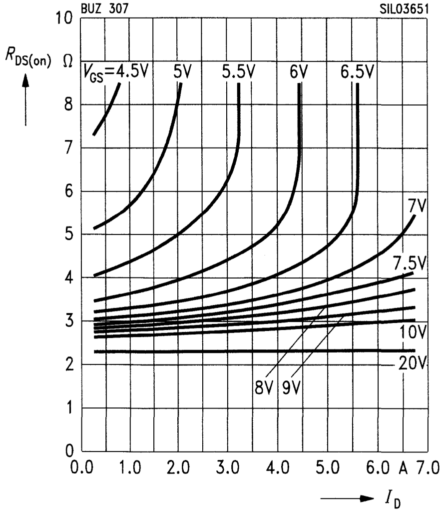
parameter: $t_p = 80$ µs



Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$ **BUZ 307**

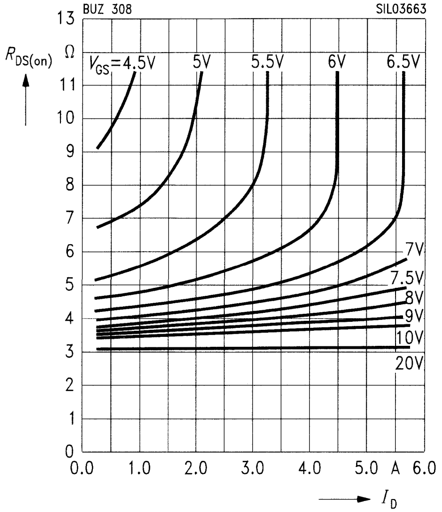
parameter: V_{GS}



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 308**

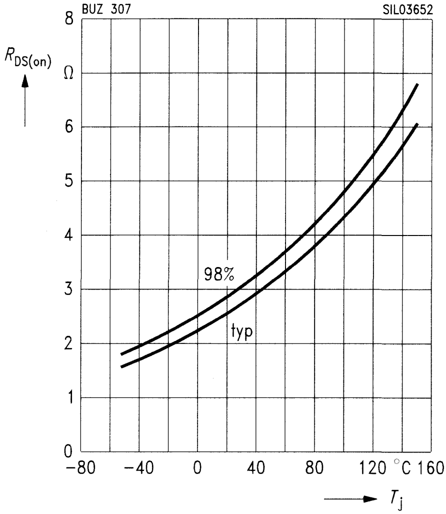
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 307**

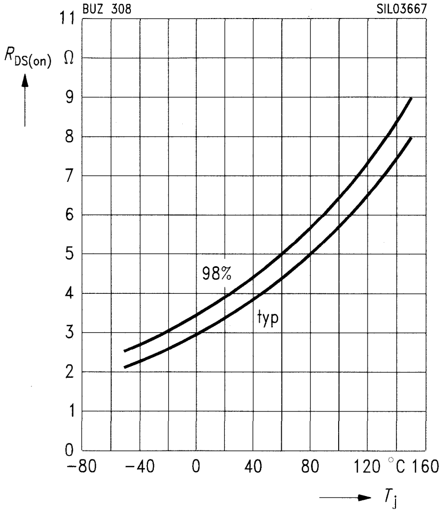
parameter: I_D = 1.7 A, V_{GS} = 10 V, (spread)



rain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 308**

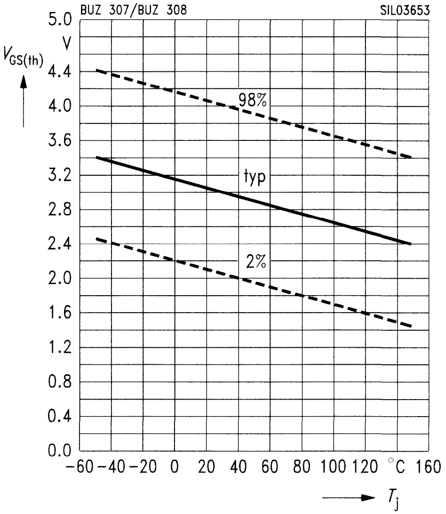
parameter: I_D = 1.7 A, V_{GS} = 10 V, (spread)



Gate threshold voltage

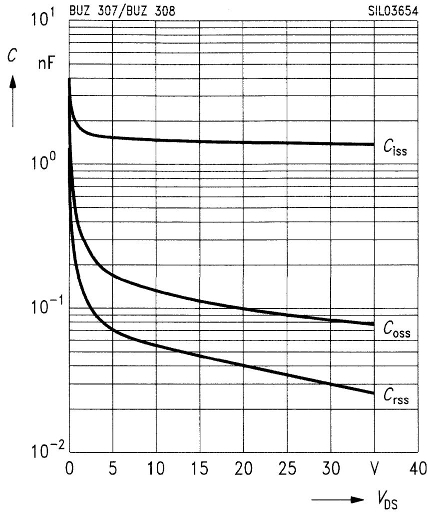
$V_{GS\,(th)} = f\,(T_j)$

parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



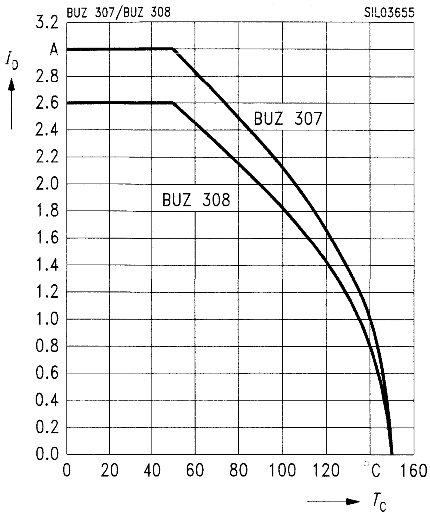
Typ. capacitances

$C = f(V_{DS})$
parameter: V_{GS} = 0 V, f = 1 MHz



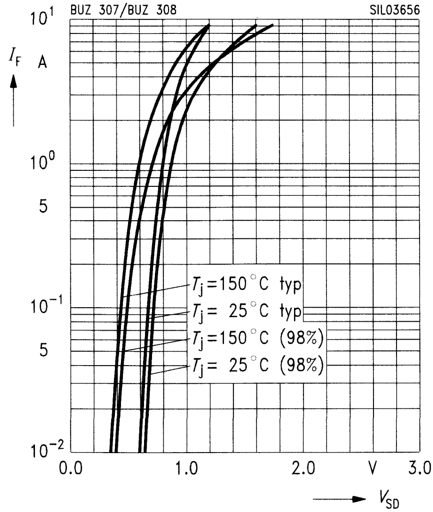
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq$ 10 V



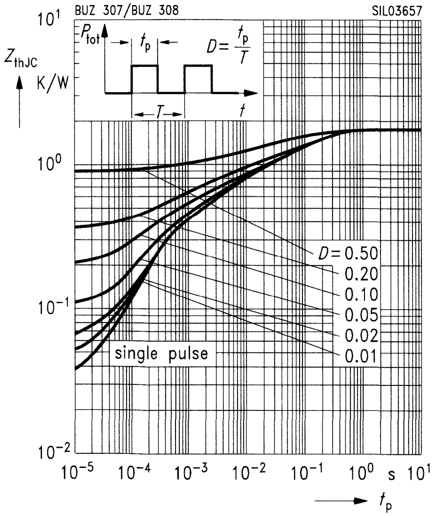
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: t_p = 80 µs, T_j

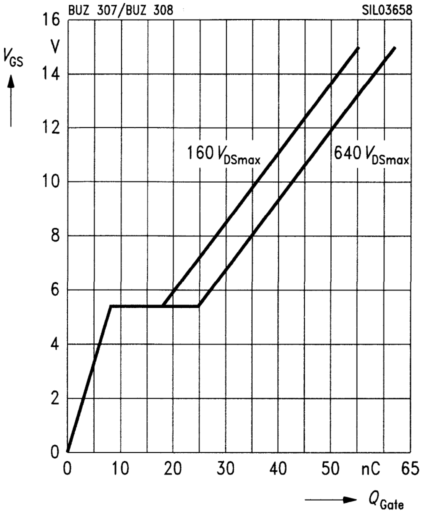


Transient thermal impedance

$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge
$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 5$ A

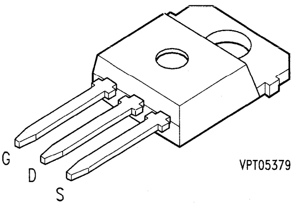


SIEMENS

SIPMOS® Power Transistors

BUZ 310
BUZ 311

- N channel
- Enhancement mode



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 310	1000 V	2.5 A	5.0 Ω	TO-218 AA	C67078-A3101-A2
BUZ 311	1000 V	2.3 A	6.0 Ω	TO-218 AA	C67078-A3102-A2

Maximum Ratings

Parameter	**Symbol**	**BUZ**		**Unit**
		310	**311**	
Continuous drain current T_C = 25 °C	I_D	**2.5**	**2.3**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**10.0**	**9.0**	
Drain-source voltage	V_{DS}	**1000**		V
Drain-gate voltage, R_{GS} = 20 kΩ	V_{DGR}	**1000**		
Gate-source voltage	V_{GS}	**± 20**		
Power dissipation, T_C = 25 °C	P_{tot}	**75**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.67**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	1000	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} =1000 V, V_{GS} = 0 V T_j = 25 °C T_j = 125 °C	I_{DSS}	 – –	 20 100	 250 1000	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 1.6 A BUZ 310 I_D = 1.6 A BUZ 311	$R_{DS(on)}$	 – –	 4.5 5.0	 5.0 6.0	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D =1.5 A	g_{fs}	0.7	1.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1600	2100	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	70	120	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	30	55	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	30	45	ns
	t_r	–	40	60	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	110	140	
	t_f	–	60	80	

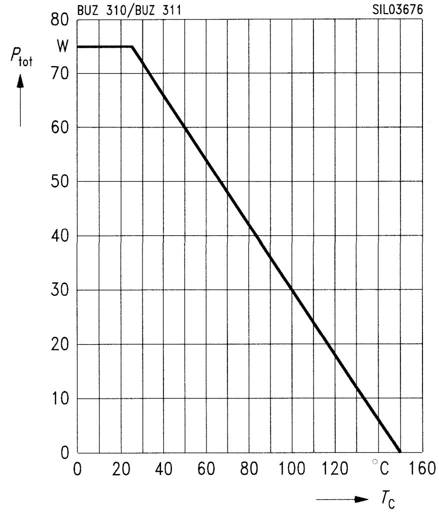
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter		**Symbol**	**Values**			**Unit**
			min.	**typ.**	**max.**	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 ˚C	BUZ 310		–	–	2.5	
	BUZ 311		–	–	2.3	
Pulsed reverse drain current		I_{SM}				A
T_C = 25 ˚C	BUZ 310		–	–	10.0	
	BUZ 311		–	–	9.0	
Diode forward on-voltage I_S = 6 A, V_{GS} = 0 V		V_{SD}	–	1.05	1.3	V
Reverse recovery time V_R = 100 V, I_F = I_S, di_F / dt = 100 A/µs		t_{rr}	–	2.0	–	ns
Reverse recovery charge V_R = 100 V, I_F = I_S, di_F / dt = 100 A/µs		Q_{rr}	–	15	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

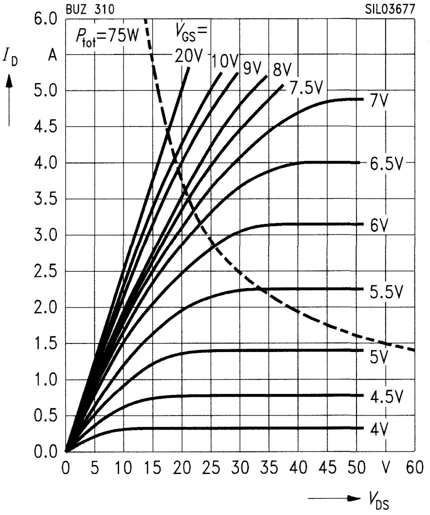
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 310**

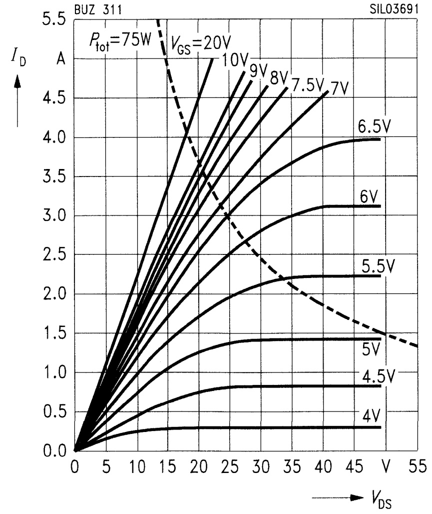
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 311**

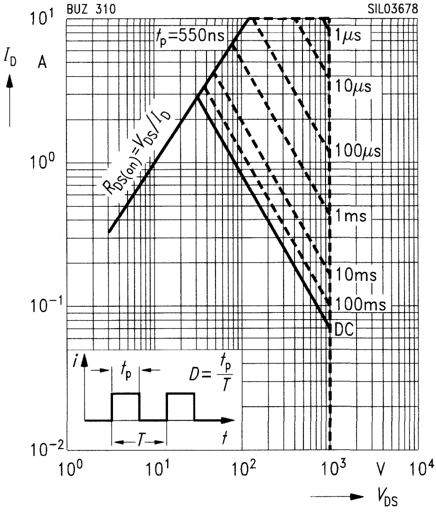
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$ **BUZ 310**

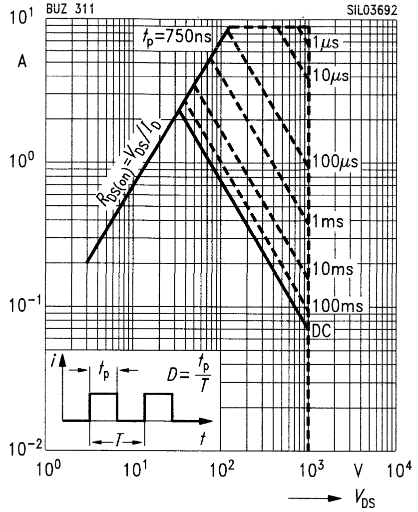
parameter: D = 0.01, T_C = 25 °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 311**

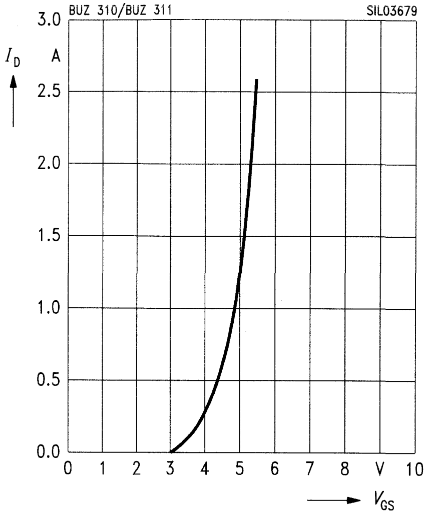
parameter: $D = 0.01$, $T_C = 25\ ^\circ C$



Typ. transfer characteristics

$I_D = f(V_{GS})$

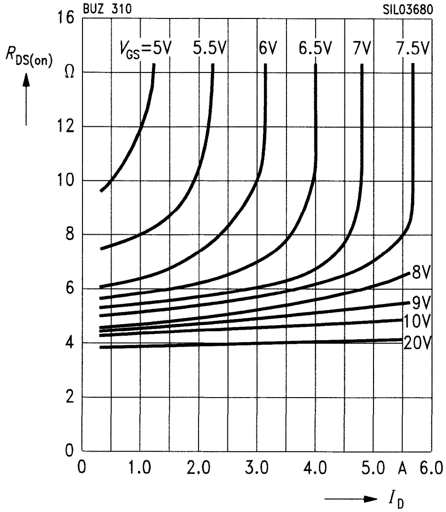
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 310**

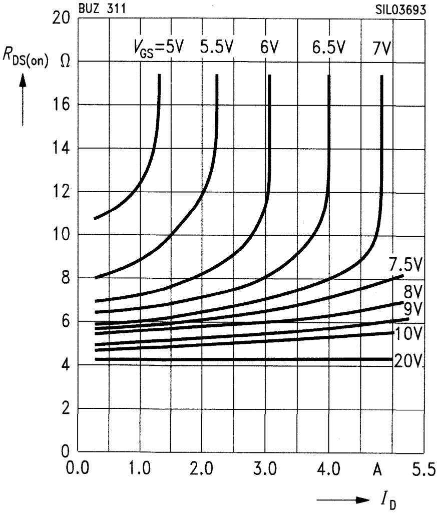
parameter: V_{GS}



Typ. drain-source on-resistance

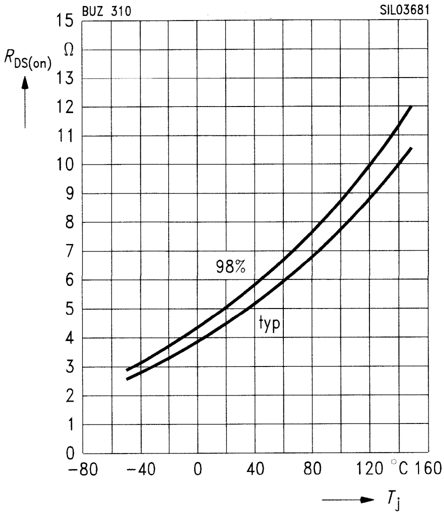
$R_{DS(on)} = f(I_D)$ **BUZ 311**

parameter: V_{GS}



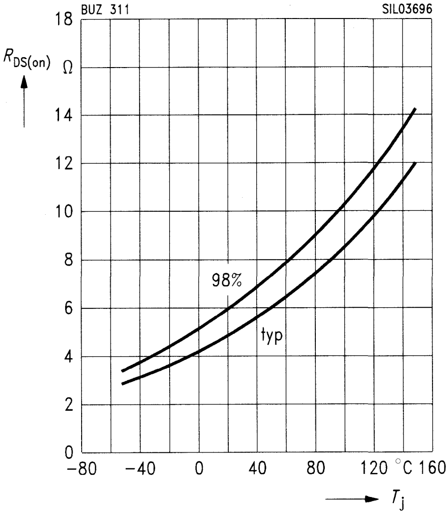
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 310**
parameter: V_{GS} = 10 V, I_D = 1.6 A



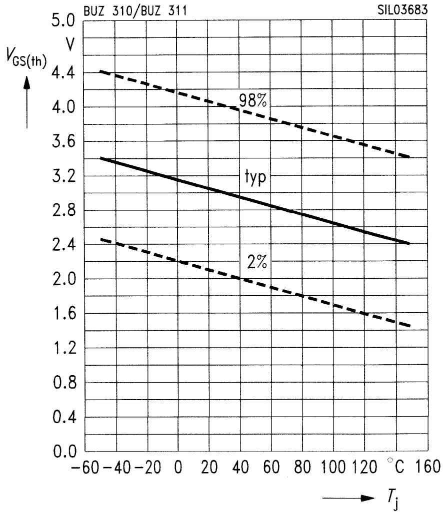
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 311**
parameter: V_{GS} = 10 V, I_D = 1.6 A



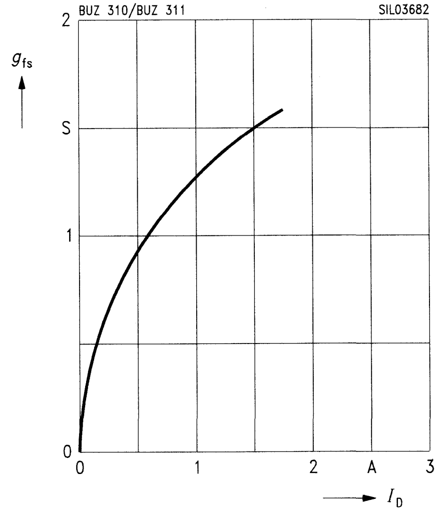
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



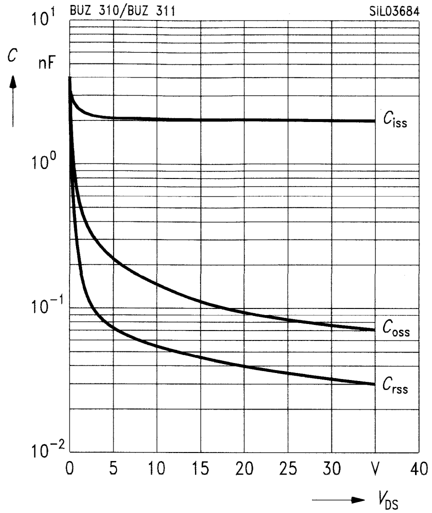
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



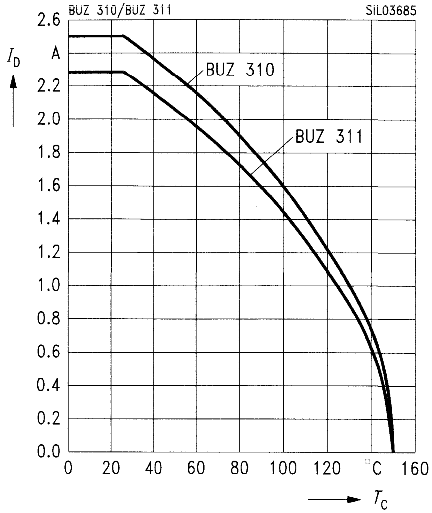
Typ. capacitances

$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



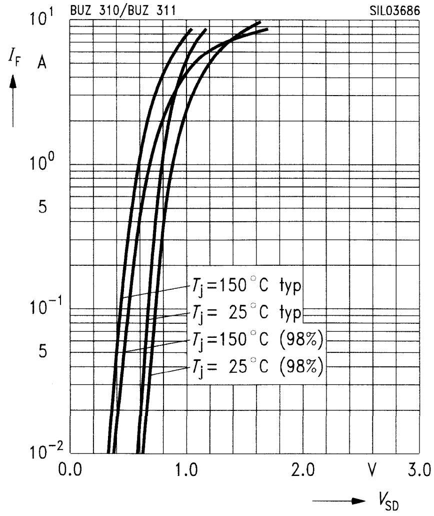
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



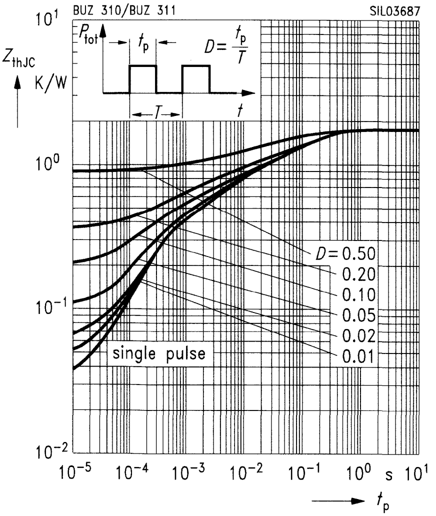
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs, (spread)

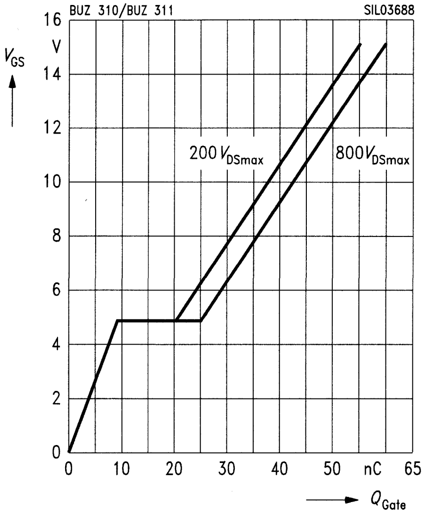


Transient thermal impedance

$Z_{thJC} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge
$V_{GS} = f\,(Q_{Gate})$
parameter: $I_{D\,puls} = 3.75$ A

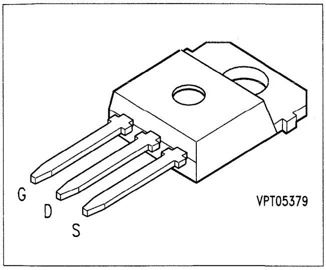


SIEMENS

SIPMOS® Power Transistor

BUZ 312

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 312	1000 V	6.0 A	1.5 Ω	TO-218 AA	C67078-S3129-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 33 ˚C	I_D	**6.0**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**24**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**6.0**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**17**	mJ
Avalanche energy, single pulse I_D = 6.0 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 43.8 mH, T_j = 25 ˚C	E_{AS}	**830**	
Gate-source voltage	V_{GS}	± **20**	V
Power dissipation, T_C = 25 ˚C	P_{tot}	**150**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\,JC}$	≤ **0.83**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	1000	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 1000 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 4.0 A	$R_{DS\,(on)}$	–	1.3	1.5	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 4.0 A	g_{fs}	2.5	6.8	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1950	2600	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	190	285	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	110	170	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.6 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	25	40	ns
	t_r	–	125	190	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.6 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	480	640	
	t_f	–	155	210	

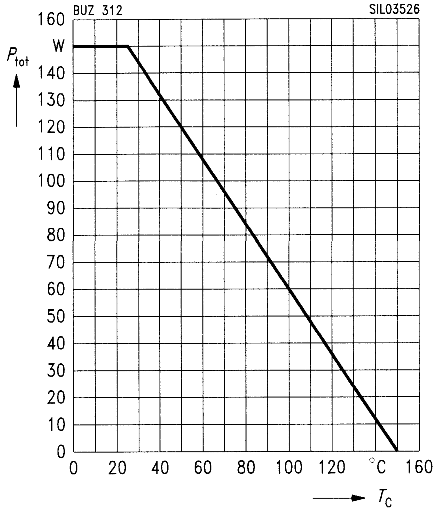
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	6.0	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	24	
Diode forward on-voltage I_S = 12 A, V_{GS} = 0 V	V_{SD}	–	0.9	1.4	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	–	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	–	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Total power dissipation

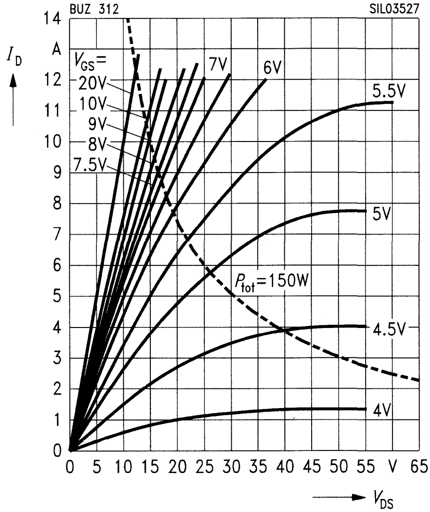
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

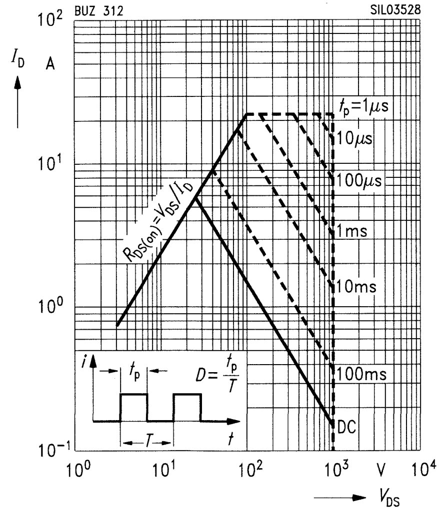
parameter: $t_p = 80$ µs



Safe operating area

$I_D = f(V_{DS})$

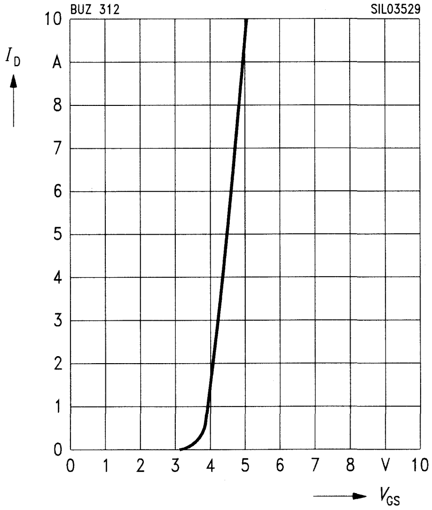
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

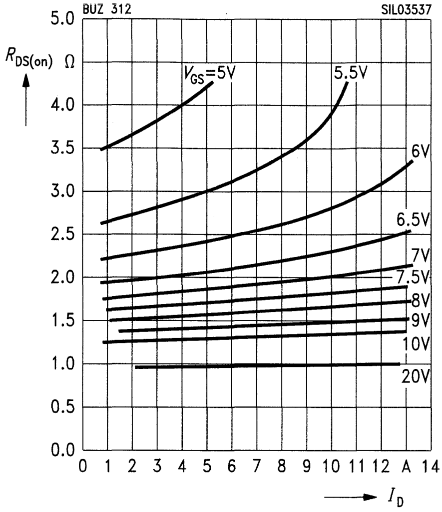
$I_D = f(V_{GS})$

parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



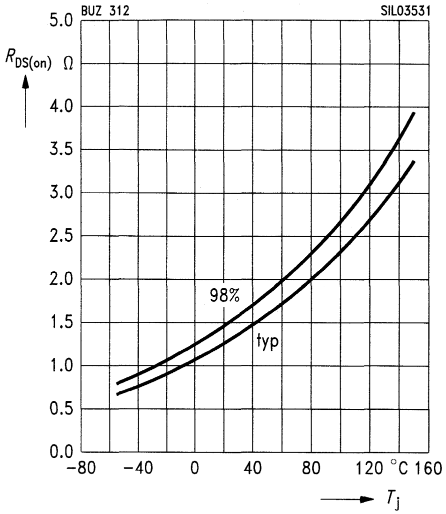
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



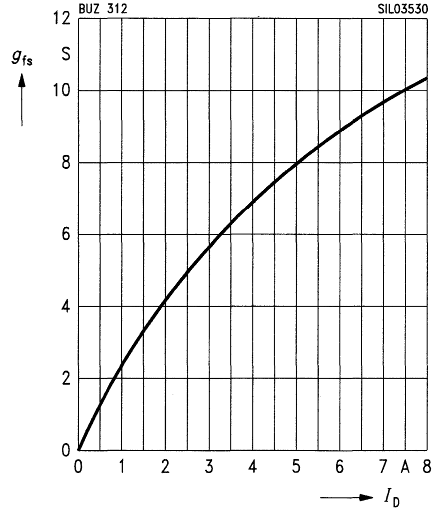
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 4 A, V_{GS} = 10 V, (spread)



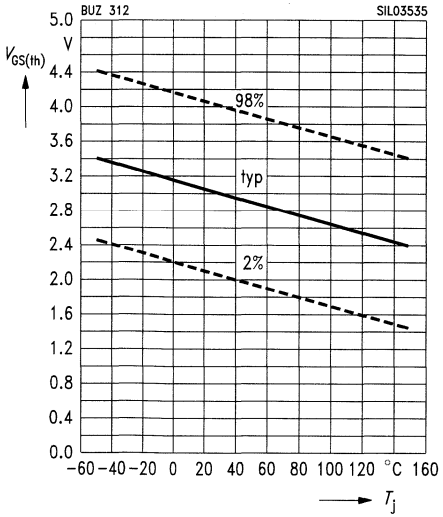
Typ.forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

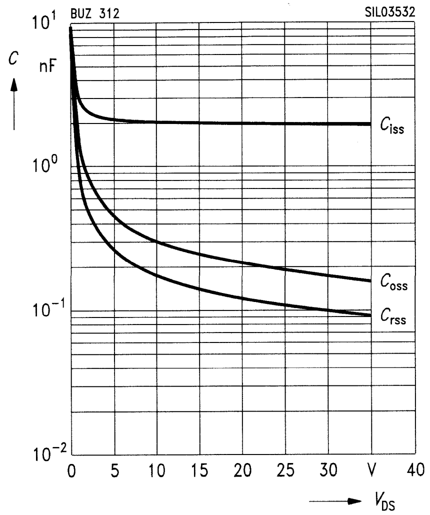
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

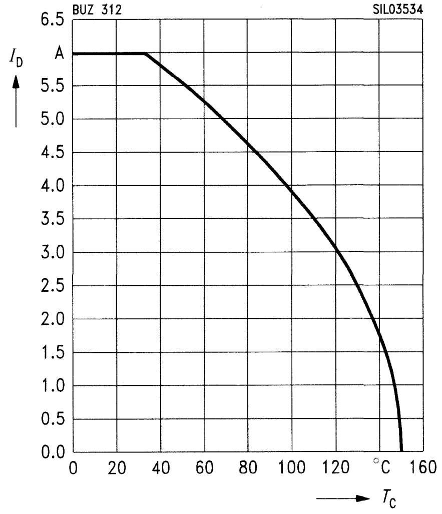
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

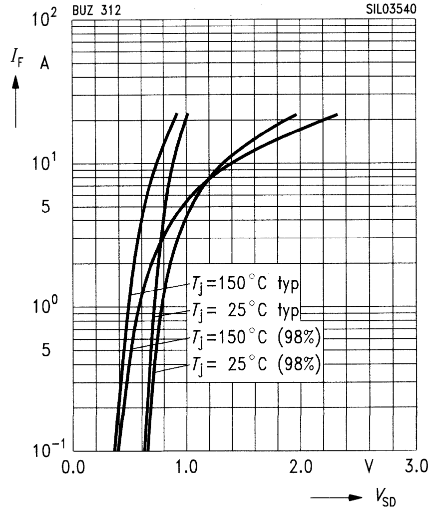
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

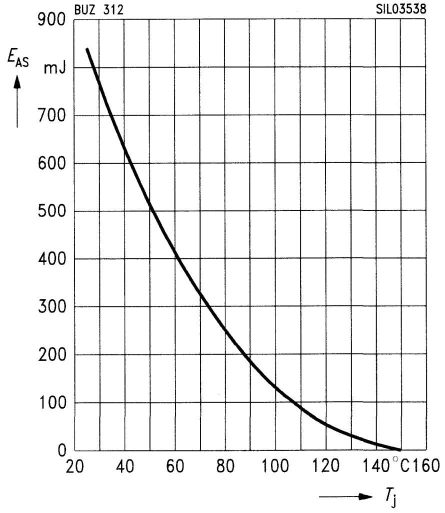
parameter: $t_p = 80$ µs, T_j



Avalanche energy $E_{AS} = f(T_j)$

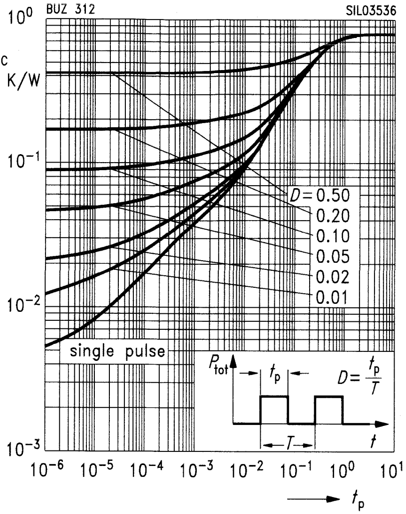
parameter: $I_D = 6$ A, $V_{DD} = 50$ V

$R_{GS} = 25\ \Omega$, $L = 43.8$ mH



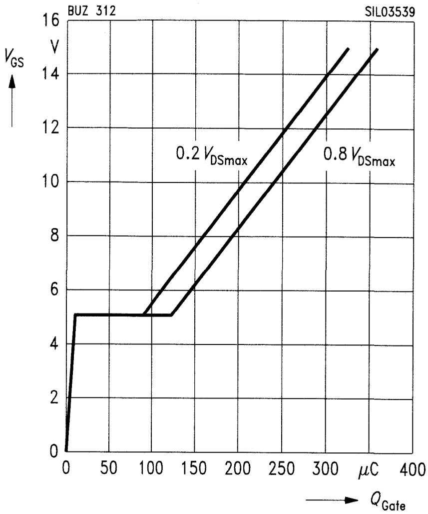
Transient thermal impedance

$Z_{\mathrm{th\,JC}} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{\mathrm{Gate}})$
parameter: $I_{\mathrm{D\,puls}}$ = 9 A

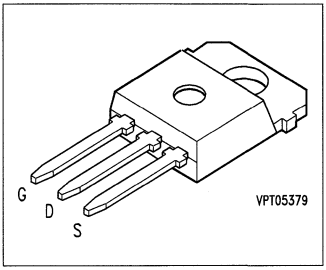


SIEMENS

SIPMOS® Power Transistor

BUZ 323

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 323	400 V	15.0 A	0.3 Ω	TO-218 AA	C67078-S3127-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 25 ˚C	I_D	**15**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**60**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**15**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**18**	mJ
Avalanche energy, single pulse I_D = 15 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 6.14 mH, T_j = 25 ˚C	E_{AS}	**790**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 ˚C	P_{tot}	**170**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 0.74**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	400	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 400 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 9.5 A	$R_{DS\,(on)}$	–	0.25	0.30	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 9.5 A	g_{fs}	8	14.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	2300	3000	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	320	480	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	120	180	
Turn-on time t_{on}, ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	40	65	ns
	t_r	–	75	115	
Turn-off time t_{off}, ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	270	350	
	t_f	–	130	170	

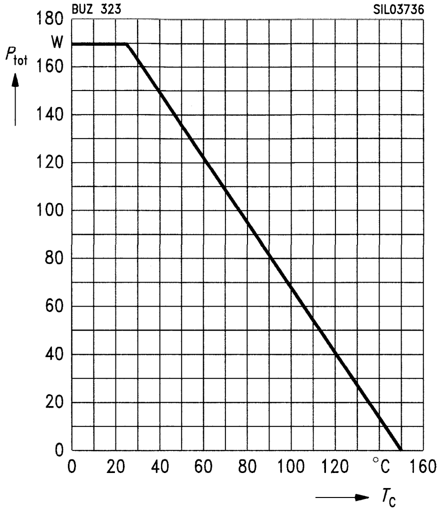
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	15	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	60	
Diode forward on-voltage I_S = 30 A, V_{GS} = 0 V	V_{SD}	–	1.1	1.5	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	120	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.25	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

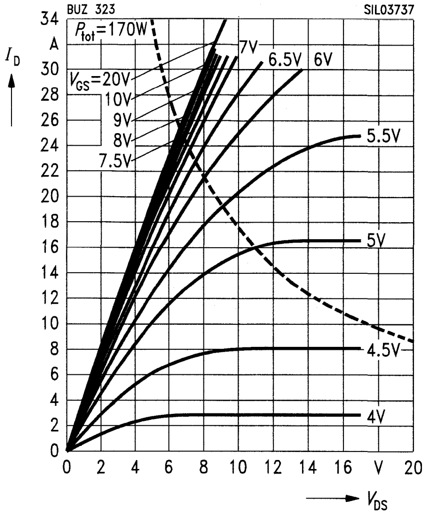
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

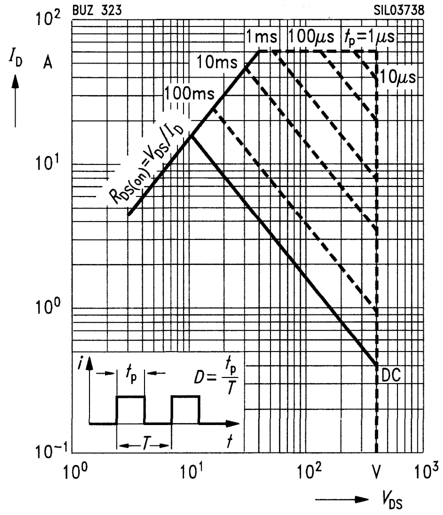
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

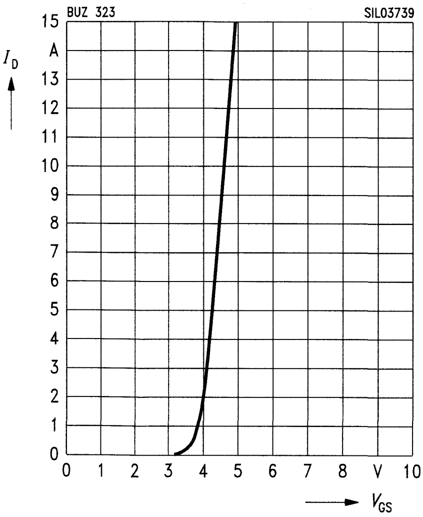
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

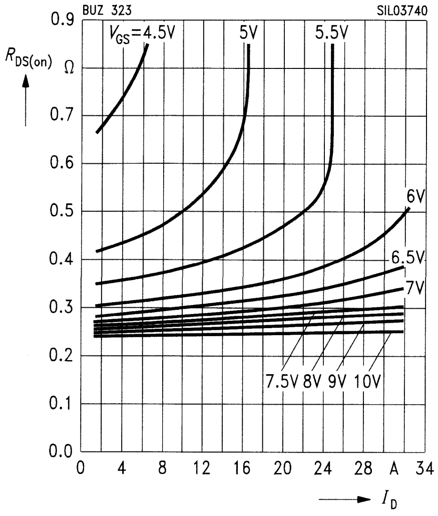
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



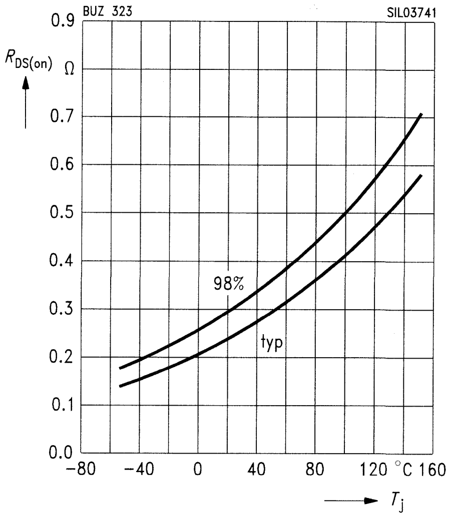
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



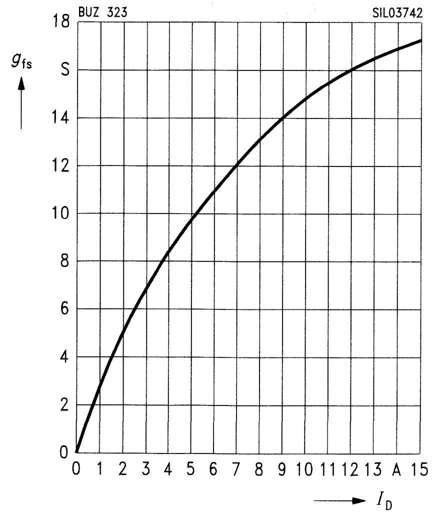
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 9.5 A, V_{GS} = 10 V, (spread)



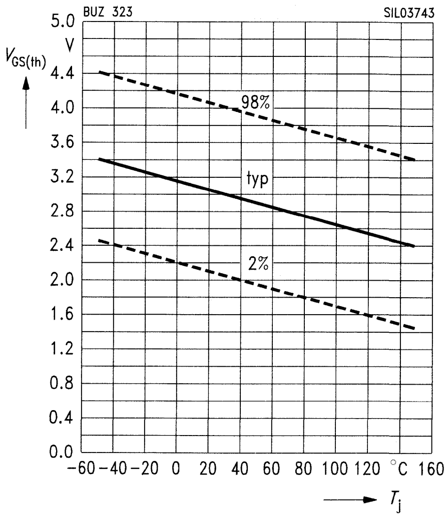
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

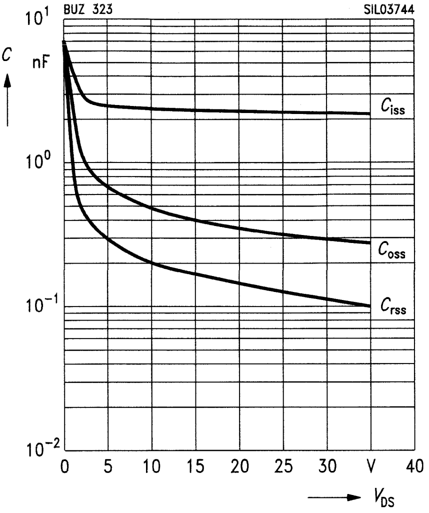
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

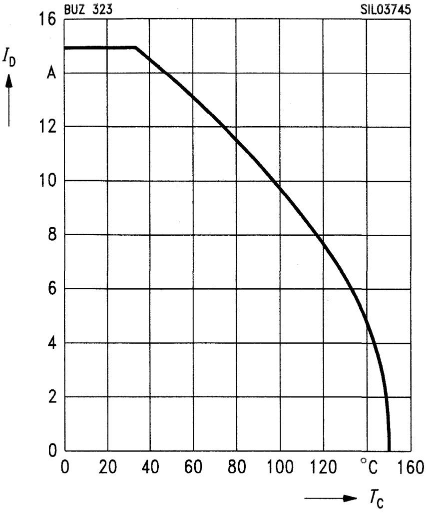
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

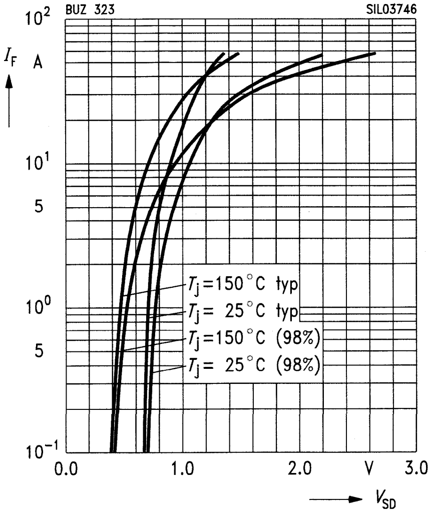
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

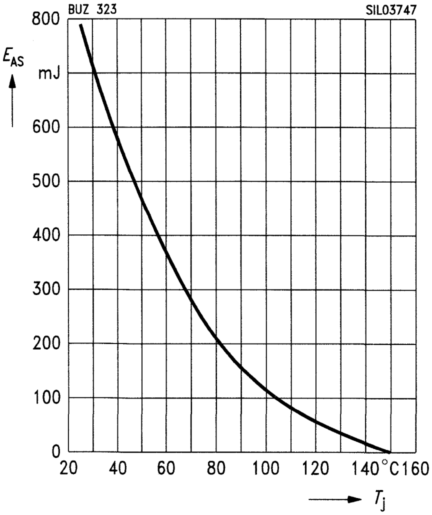
parameter: $t_p = 80$ µs, T_j



Avalanche energy $E_{AS} = f(T_j)$

parameter: $I_D = 15$ A, $V_{DD} = 50$ V

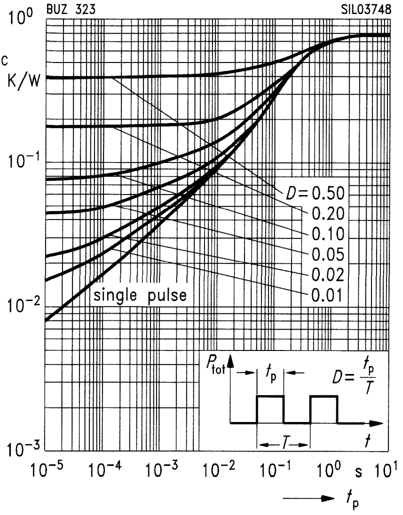
$R_{GS} = 25\ \Omega$, $L = 6.14$ mH



Transient thermal impedance

$Z_{\text{th JC}} = f\,(t_p)$

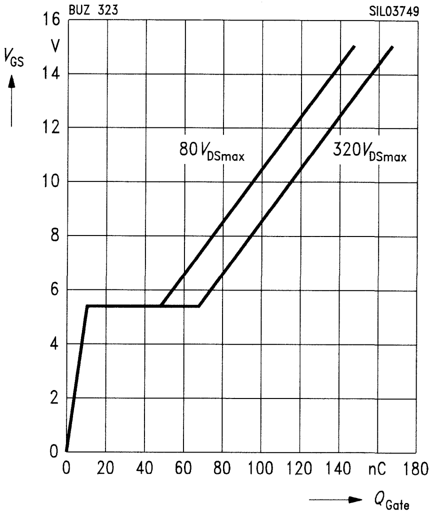
parameter: $D = t_p\,/\,T$



Typ. gate charge

$V_{\text{GS}} = f\,(Q_{\text{Gate}})$

parameter: $I_{\text{D puls}} = 22.5$ A

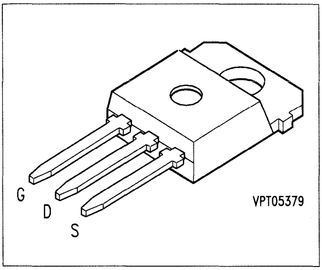


SIEMENS

SIPMOS® Power Transistor

BUZ 325

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 325	400 V	12.5 A	0.35 Ω	TO-218 AA	C67078-S3118-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 27 ˚C	I_D	**12.5**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**50**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**12.5**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**14**	mJ
Avalanche energy, single pulse I_D = 12.5 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 7.50 mH, T_j = 25 ˚C	E_{AS}	**670**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 ˚C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	**typ.**	**max.**	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	400	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 400 V, V_{GS} = 0 V T_j = 25 °C T_j = 125 °C	I_{DSS}	 – –	 0.1 10	 1.0 100	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 8.0 A	$R_{DS(on)}$	–	0.28	0.35	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 8.0 A	g_{fs}	8.0	9.8	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1900	2500	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	260	400	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	110	170	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	30	45	ns
	t_r	–	90	135	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	350	465	
	t_f	–	100	135	

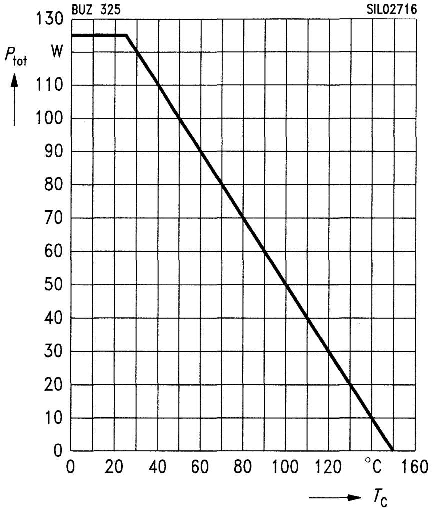
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	12.5	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	50	
Diode forward on-voltage I_S = 25 A, V_{GS} = 0 V	V_{SD}	–	1.0	1.5	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	450	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	6.8	–	µC

Characteristics at $T_j = 25\ ^\circ\text{C}$, unless otherwise specified.

Total power dissipation

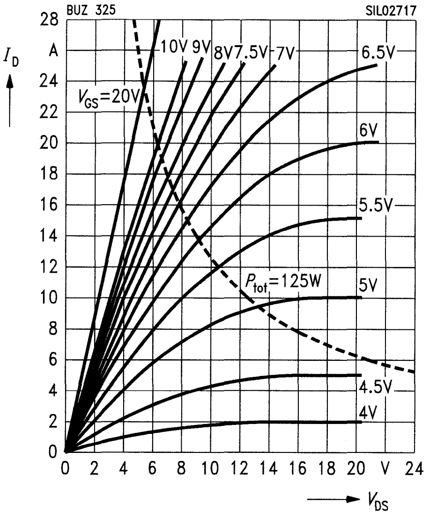
$P_{tot} = f\,(T_C)$



Typ. output characteristics

$I_D = f\,(V_{DS})$

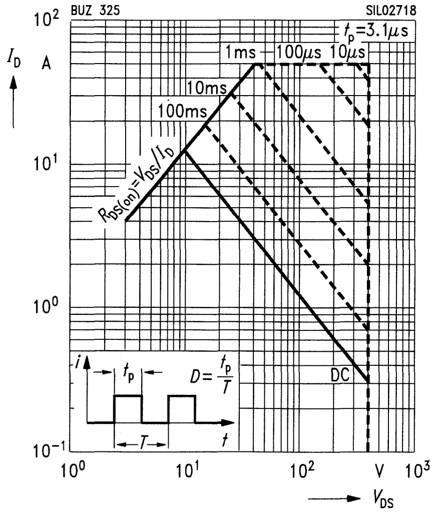
parameter: t_p = 80 µs



Safe operating area

$I_D = f\,(V_{DS})$

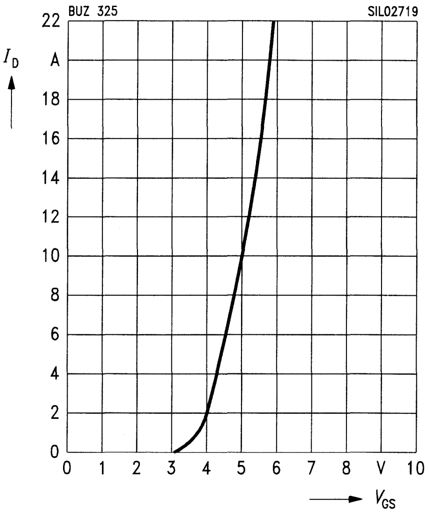
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

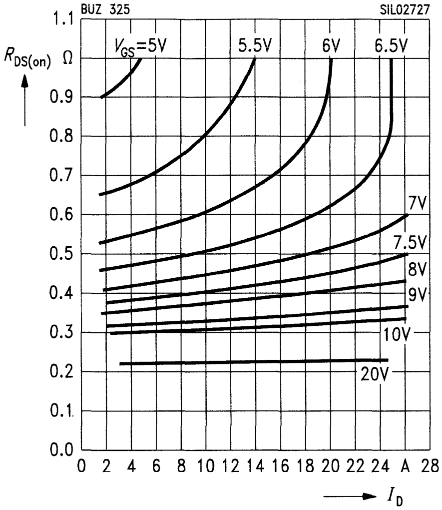
$I_D = f\,(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



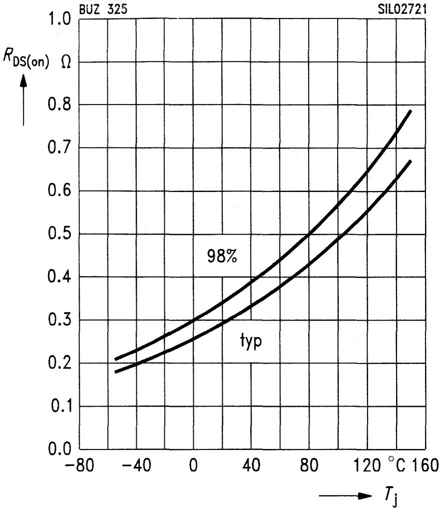
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



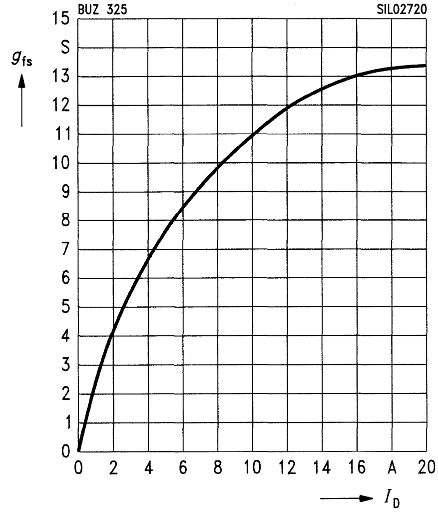
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 8.0 A, V_{GS} = 10 V, (spread)



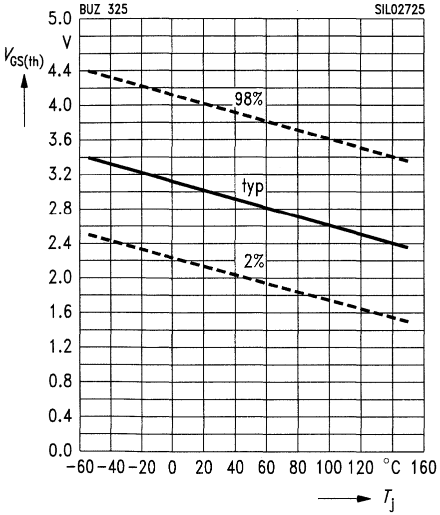
Typ.forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

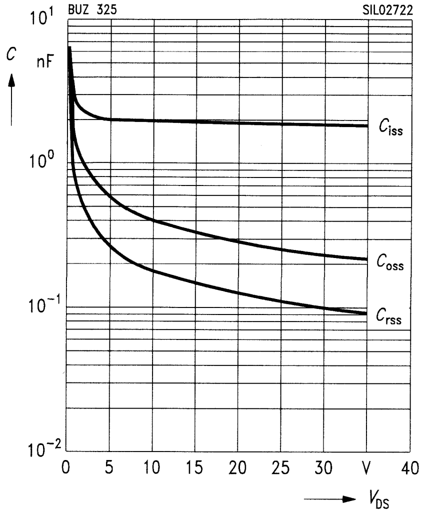
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f\,(V_{DS})$

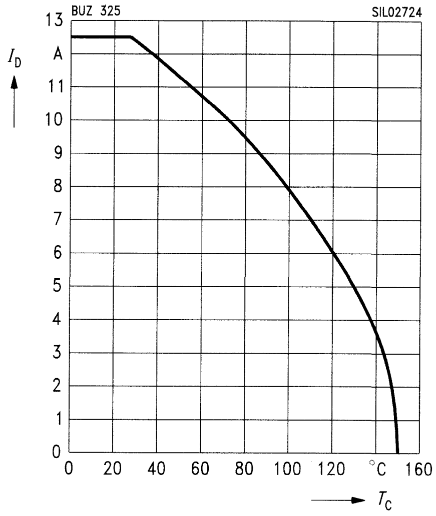
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f\,(T_C)$

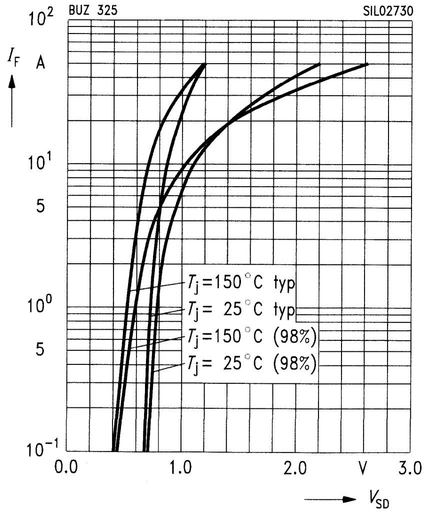
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f\,(V_{SD})$

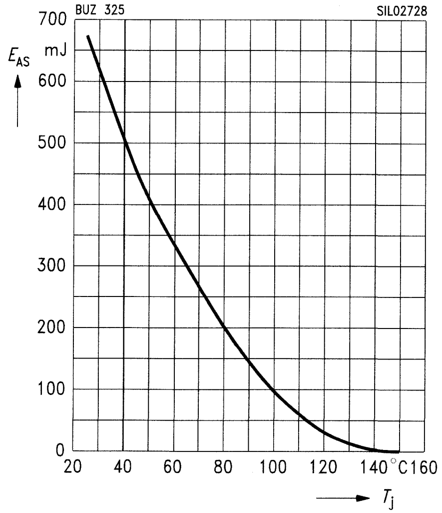
parameter: T_j , $t_p = 80$ µs



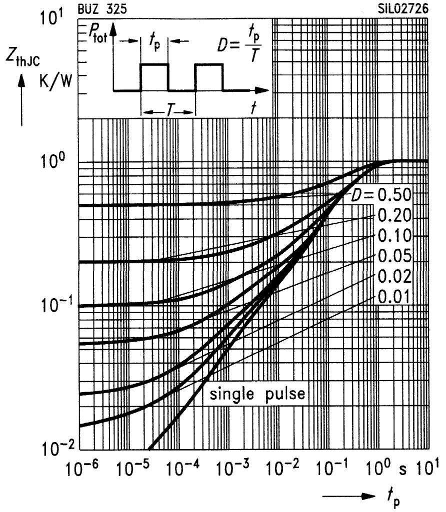
Avalanche energy $E_{AS} = f\,(T_j)$

parameter: $I_D = 12.5$ A, $V_{DD} = 50$ V

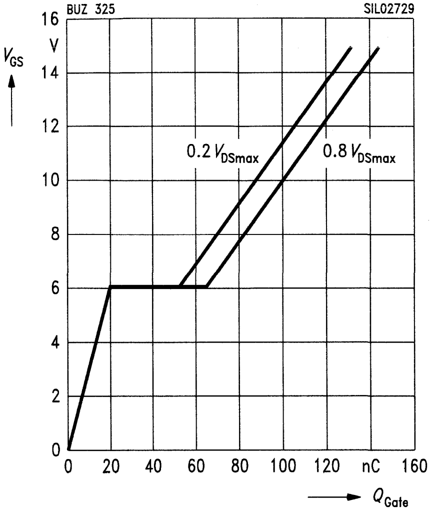
$R_{GS} = 25\ \Omega$, $L = 7.50$ mH



Transient thermal impedance
$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge
$V_{GS} = f(Q_{\text{Gate}})$
parameter: $I_{\text{D puls}}$ = 21.0 A

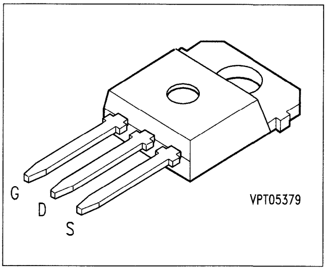


SIEMENS

SIPMOS® Power Transistor

BUZ 326

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 326	400 V	10.5 A	0.5 Ω	TO-218 AA	C67078-S3112-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 27 ˚C	I_D	**10.5**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**42**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**10.5**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**13**	mJ
Avalanche energy, single pulse I_D = 10.5 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 9.05 mH, T_j = 25 ˚C	E_{AS}	**570**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 ˚C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	400	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 400 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 6.5 A	$R_{DS\,(on)}$	–	0.35	0.5	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$ I_D = 6.5 A	g_{fs}	5.0	10.2	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1500	2250	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	210	315	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	75	110	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD}= 30 V, V_{GS} = 10 V, I_D =3.0 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	20	30	ns
	t_r	–	65	100	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	260	340	
	t_f	–	75	100	

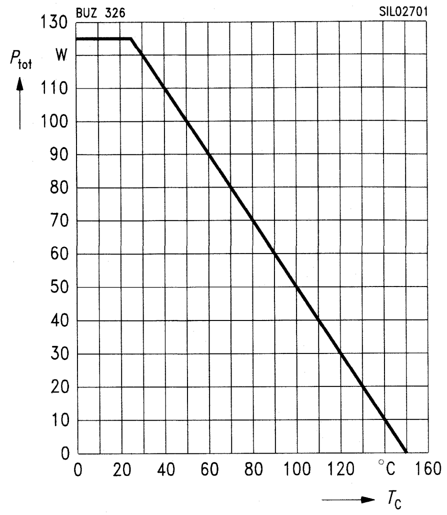
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	10.5	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	42	
Diode forward on-voltage I_S = 22 A, V_{GS} = 0	V_{SD}	–	1.0	1.4	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	280	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	3	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

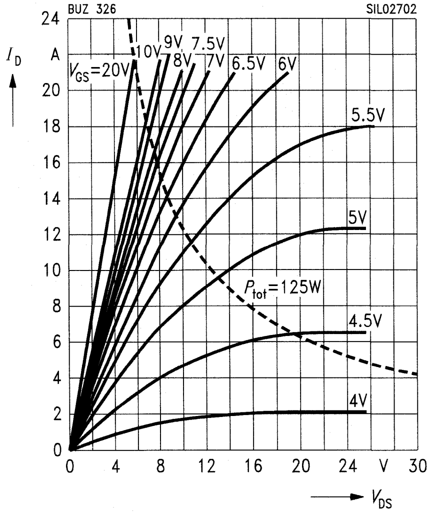
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

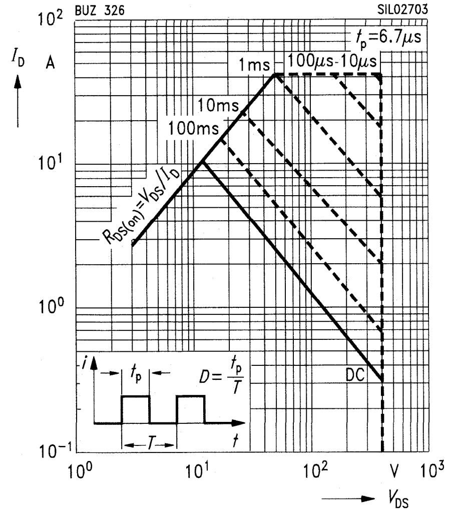
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

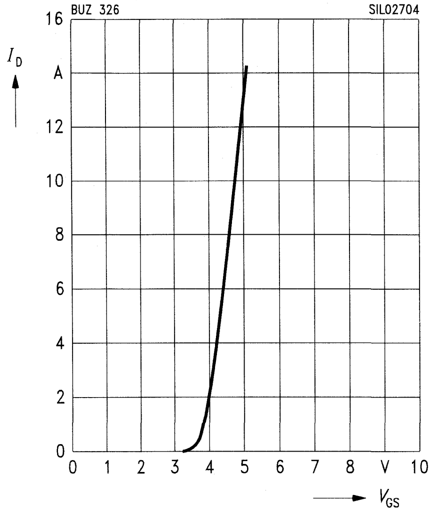
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

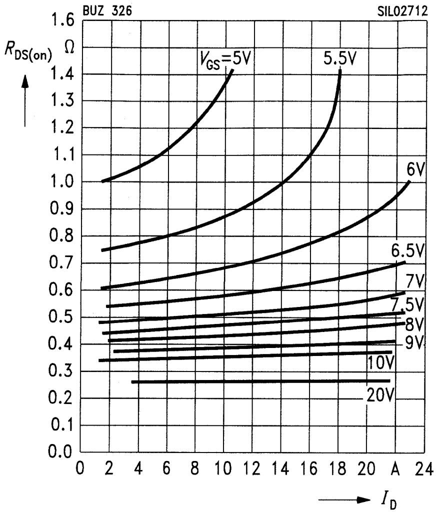
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

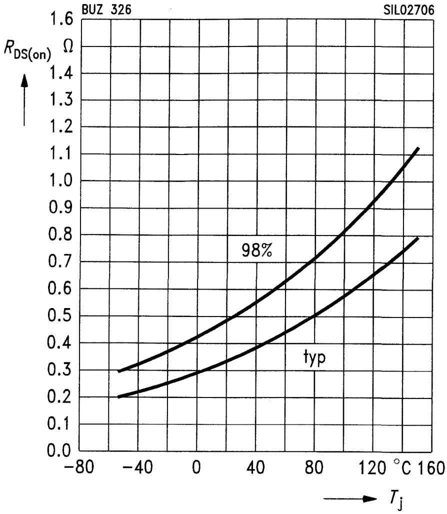
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

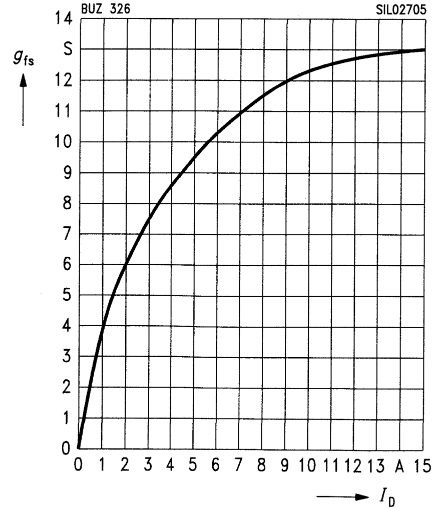
parameter: I_D = 6.5 A, V_{GS} = 10 V, (spread)



Typ. forward transconductance

$g_{fs} = f\,(I_D)$

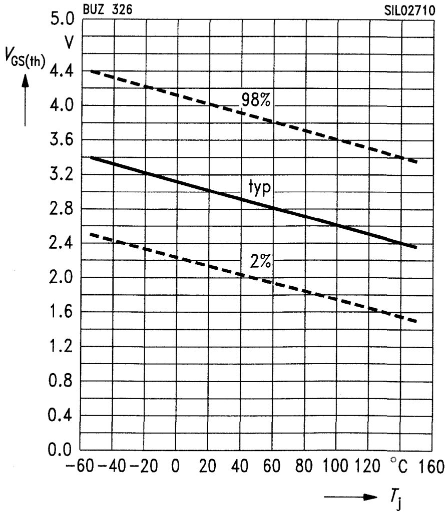
parameter: t_p = 80 µs



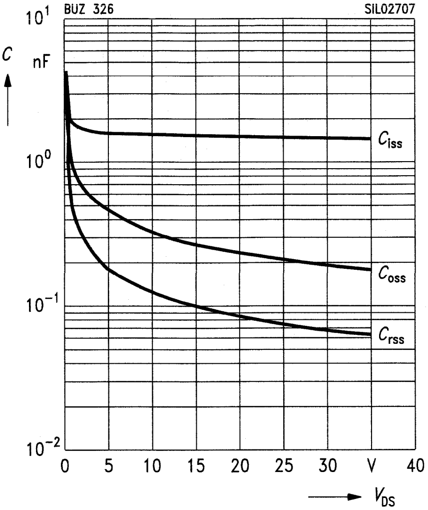
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

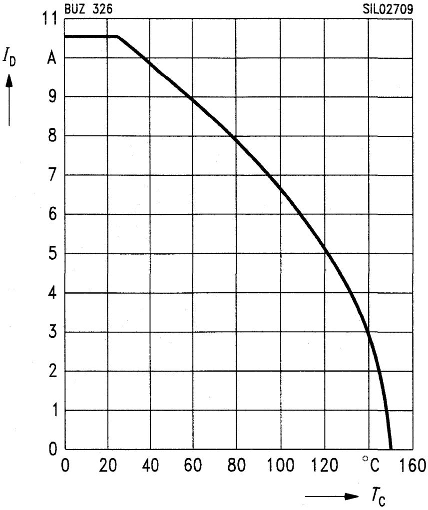
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



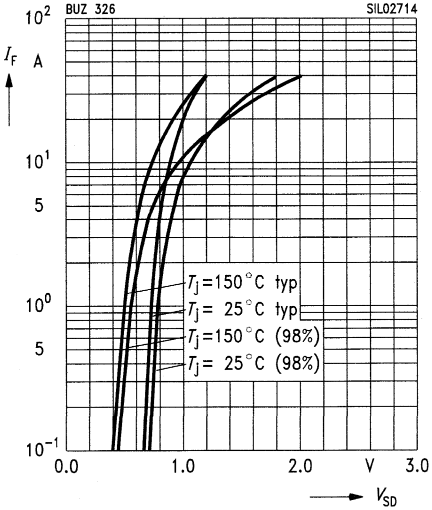
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



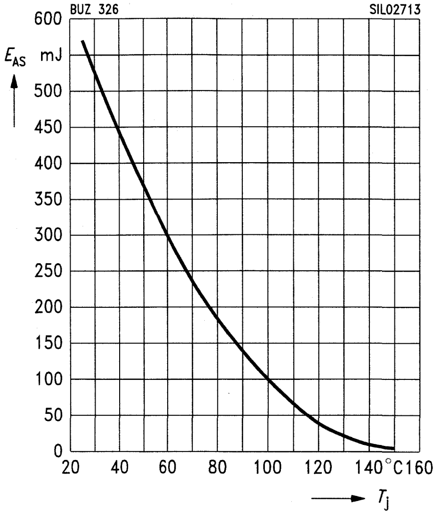
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j , $t_p = 80$ µs, (spread)



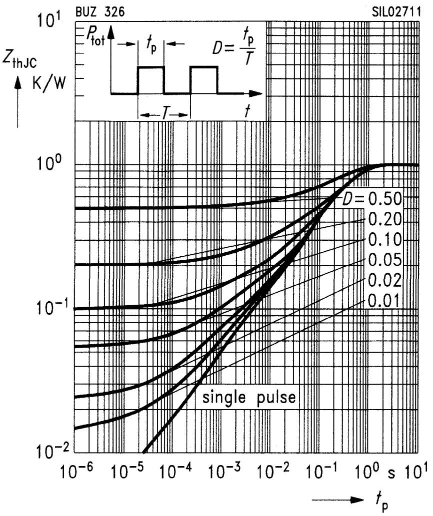
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 10.5$ A, $V_{DD} = 50$ V
$R_{GS} = 25\ \Omega$, $L = 9.05$ mH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

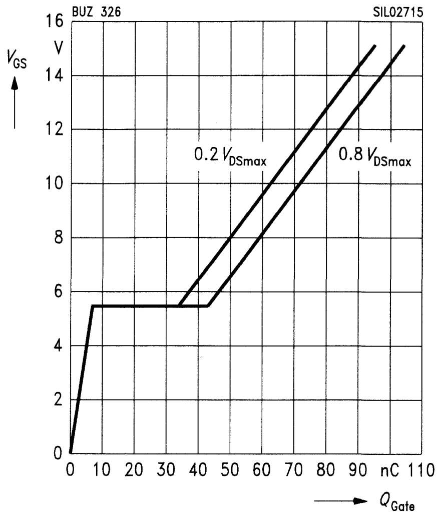
parameter: $D = t_p / T$



Typ. gate charge

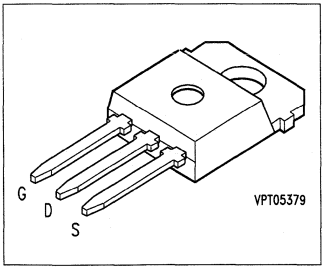
$V_{GS} = f(Q_{\text{Gate}})$

parameter: $I_{\text{D puls}} = 15.0$ A



SIPMOS® Power Transistor **BUZ 330**

- N channel
- Enhancement mode
- Avalanche rated



Type	V_{DS}	I_D	T_C	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 330	500 V	9.5 A	28 °C	0.6 Ω	TO-218 AA	C67078-S3105-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current	I_D	**9.5**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**38**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**9.5**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**13**	mJ
Avalanche energy, single pulse $I_D = 9.5$ A, $V_{DD} = 50$ V, $R_{GS} = 25\ \Omega$ $L = 13.4$ mH, $T_j = 25$ °C	E_{AS}	**670**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, $T_C = 25$ °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j, T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

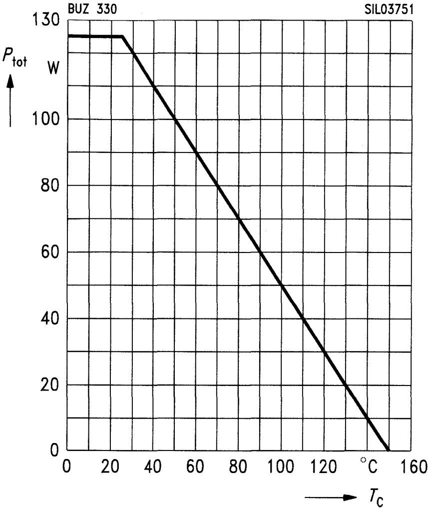
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	500	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 500 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 6.0 A	$R_{DS(on)}$	–	0.45	0.6	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 6.0 A	g_{fs}	5.0	9.3	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1700	2300	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	220	330	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	95	140	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	23	35	ns
	t_r	–	95	145	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	340	450	
	t_f	–	110	150	

Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

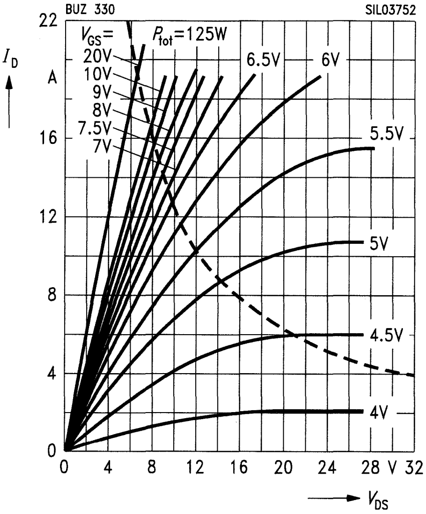
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	9.5	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	38	
Diode forward on-voltage I_S = 19 A, V_{GS} = 0 V	V_{SD}	–	1.0	1.4	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	400	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	6.0	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

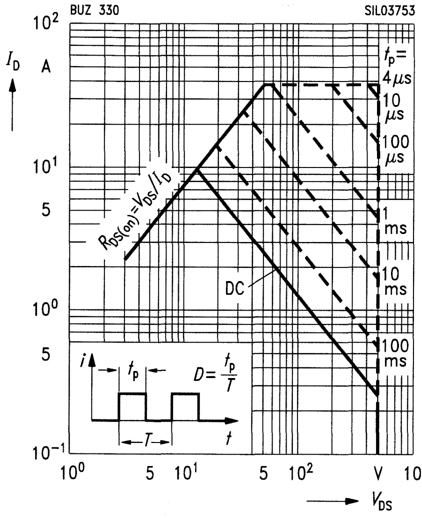
Total power dissipation
$P_{tot} = f(T_C)$



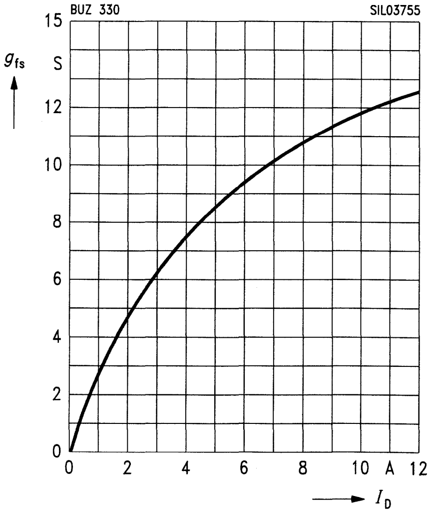
Typ. output characteristics
$I_D = f(V_{DS})$
parameter: $t_p = 80$ µs



Safe operating area
$I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25$ °C



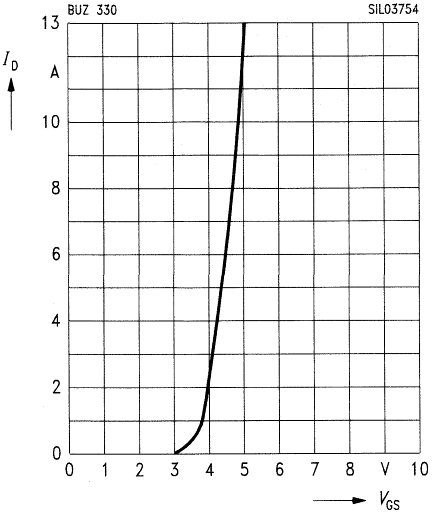
Typ. forward transconductance
$g_{fs} = f(I_D)$
parameter: $t_p = 80$ µs



Typ. transfer characteristics

$I_D = f(V_{GS})$

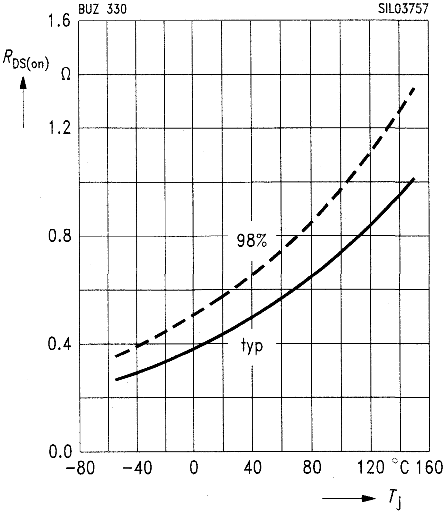
parameter: t_p = 80 µs, V_{DS} = 25 V



Drain-source on-resistance

$R_{DS\,(on)} = f(T_j)$

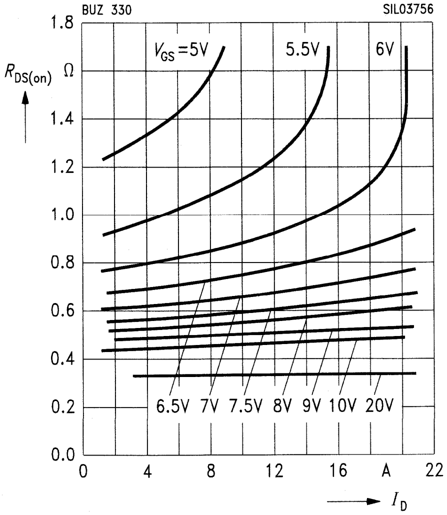
parameter: I_D = 6 A, V_{GS} = 10 V, (spread)



Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$

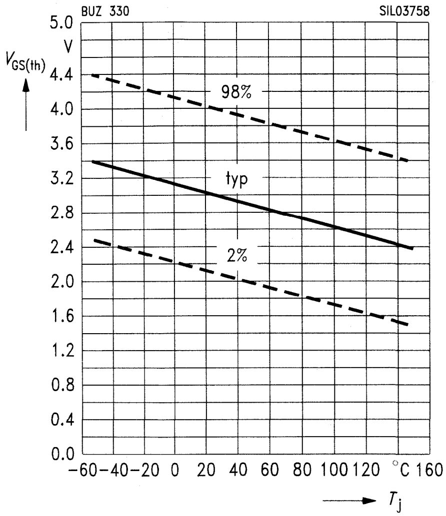
parameter: V_{GS}



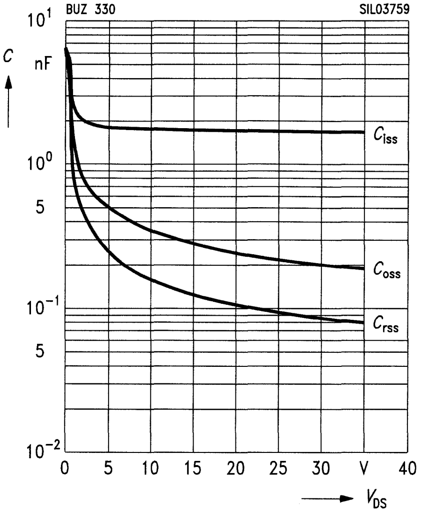
Gate threshold voltage

$V_{GS\,(th)} = f(T_j)$

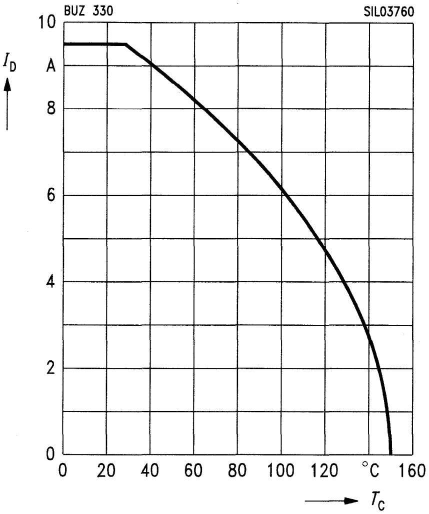
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



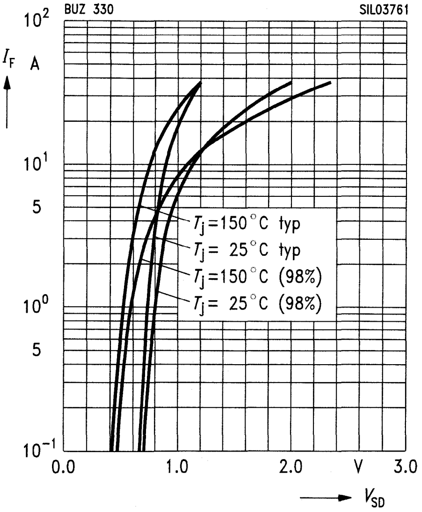
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



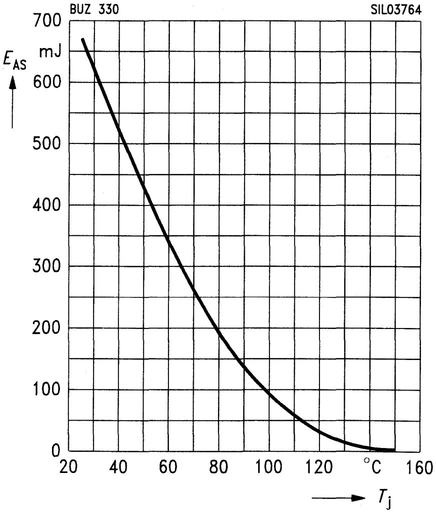
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: $t_p = 80$ µs, T_j



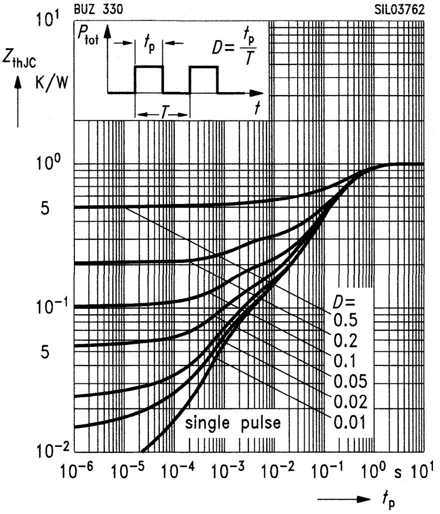
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 9.5$ A, $V_{DD} = 50$ V
$R_{GS} = 25\ \Omega$, $L =$ **13.4** mH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

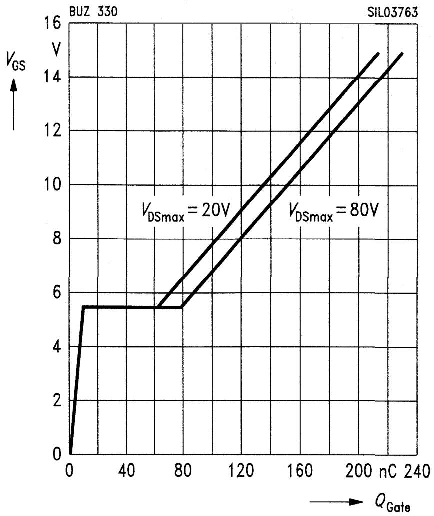
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{\text{Gate}})$

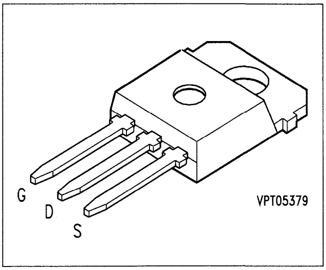
parameter: $I_{\text{D puls}} = 14.25$ A



SIPMOS® Power Transistor

BUZ 331

- N channel
- Enhancement mode
- Avalanche rated



Type	V_{DS}	I_D	T_C	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 331	500 V	8.0 A	35 ˚C	0.8 Ω	TO-218 AA	C67078-S3114-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current	I_D	**8.0**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**32**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**8.0**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**13**	mJ
Avalanche energy, single pulse I_D = 8.0 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 16 mH, T_j = 25 ˚C	E_{AS}	**570**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 ˚C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	500	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 500 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 5.5 A	$R_{DS\,(on)}$	–	0.6	0.8	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 5.5 A	g_{fs}	5.0	8.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1500	2300	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	18	270	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	65	100	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	20	30	ns
	t_r	–	70	110	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	260	340	
	t_f	–	80	150	

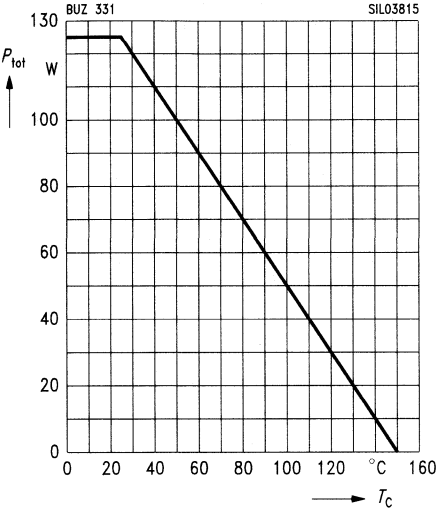
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	5.0	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	20	
Diode forward on-voltage I_S = 10 A, V_{GS} = 0 V	V_{SD}	–	1.1	1.2	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	380	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	4.0	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

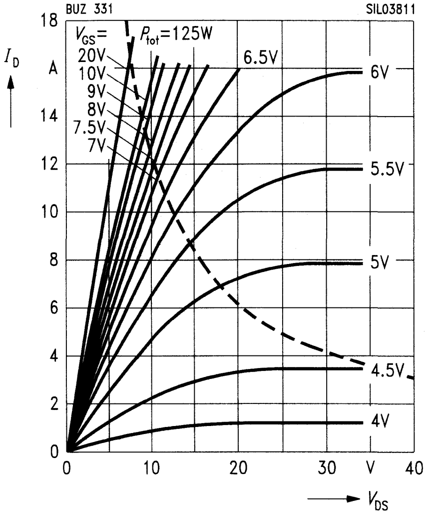
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

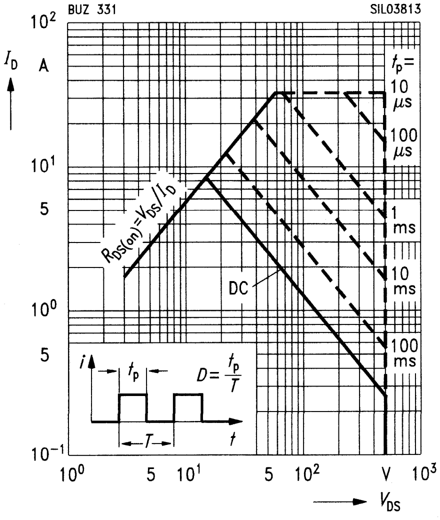
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

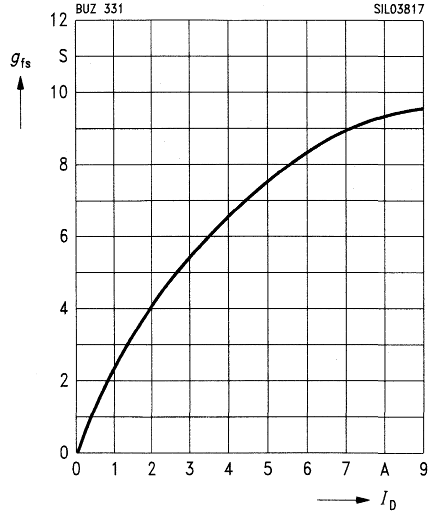
parameter: D = 0.01, T_C = 25 °C



Typ. forward transconductance

$g_{fs} = f(I_D)$

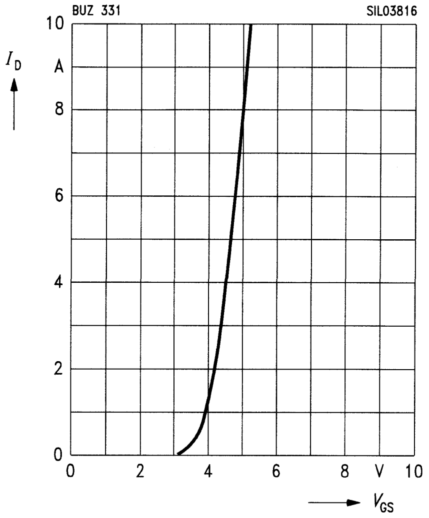
parameter: t_p = 80 µs



Typ. transfer characteristics

$I_D = f(V_{GS})$

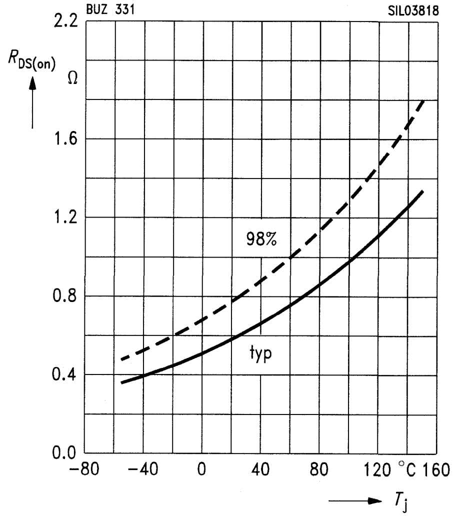
parameter: $t_p = 80\ \mu s$, $V_{DS} = 25\ V$



Drain-source on-resistance

$R_{DS\,(on)} = f(T_j)$

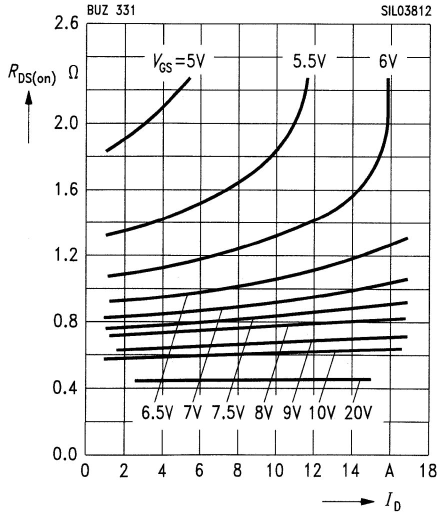
parameter: $I_D = 5.5$ A, $V_{GS} = 10$ V, (spread)



Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$

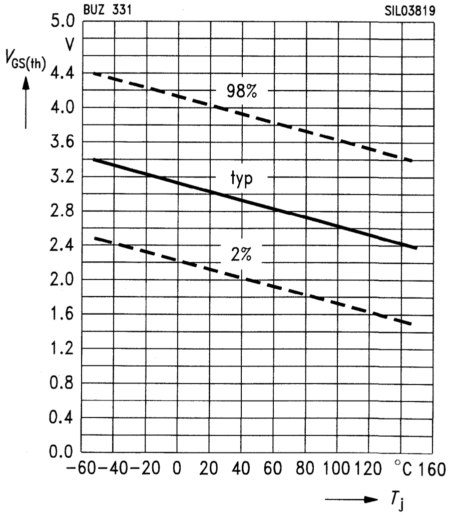
parameter: V_{GS}



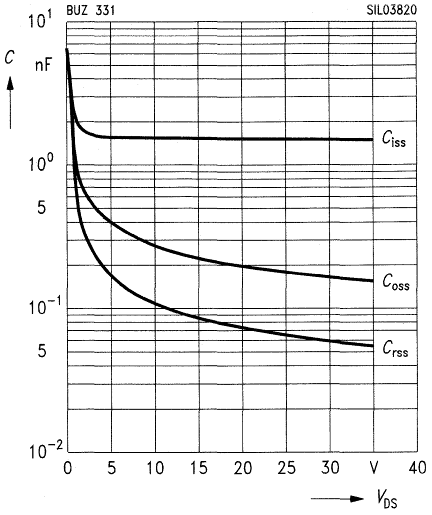
Gate threshold voltage

$V_{GS\,(th)} = f(T_j)$

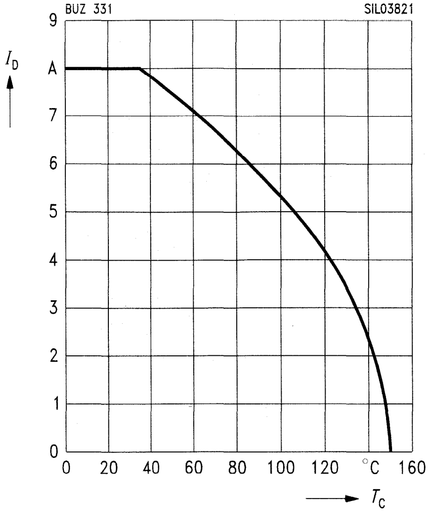
parameter: $V_{GS} = V_{DS}$, $I_D = 1$ mA, (spread)



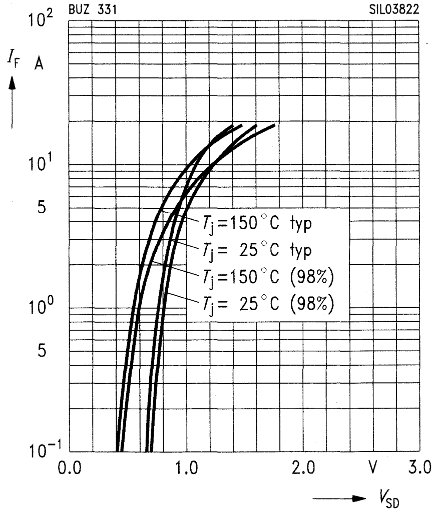
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



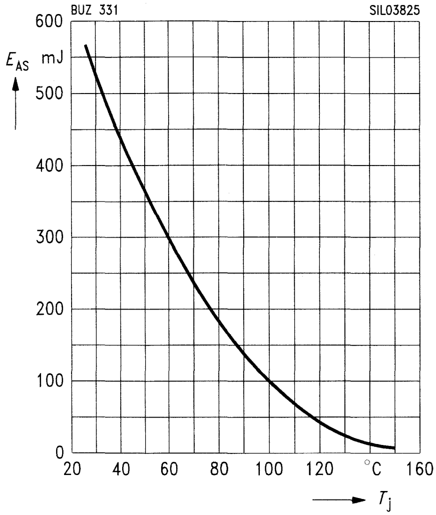
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: $t_p = 80$ µs, T_j



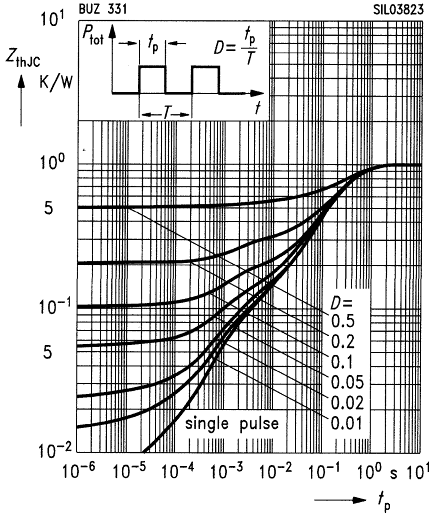
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 8$ A, $V_{DD} = 50$ V
$R_{GS} = 25\ \Omega$, $L = 16$ mH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

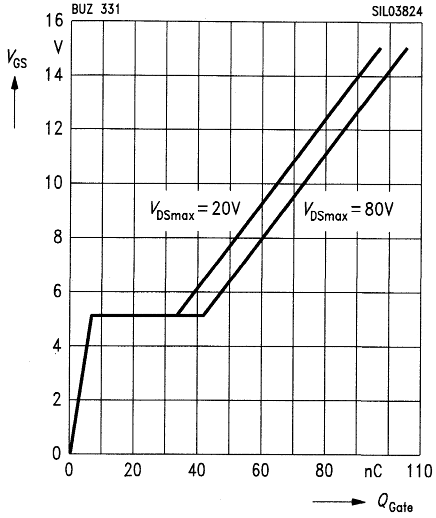
parameter: $D = t_p / T$



Typ. gate charge

$V_{\text{GS}} = f(Q_{\text{Gate}})$

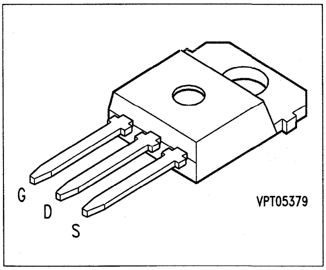
parameter: $I_{\text{D puls}} = 12$ A



SIPMOS® Power Transistors

BUZ 332
BUZ 332 A

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	T_C	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 332	600 V	8.5 A	33 °C	0.8 Ω	TO-218 AA	C67078-S3123-A2
BUZ 332 A	600 V	8.0 A	33 °C	0.9 Ω	TO-218 AA	C67078-S3123-A4

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		332	332 A	
Continuous drain current	I_D	**8.5**	**8.0**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**34.0**	**32**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**8.0**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**13**		mJ
Avalanche energy, single pulse $I_D = 8$ A, $V_{DD} = 50$ V, $R_{GS} = 25\ \Omega$ $L = 16.3$ mH, $T_j = 25$ °C	E_{AS}	**570**		
Gate-source voltage	V_{GS}	**± 20**		V
Power dissipation, $T_C = 25$ °C	P_{tot}	**150**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 0.83**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

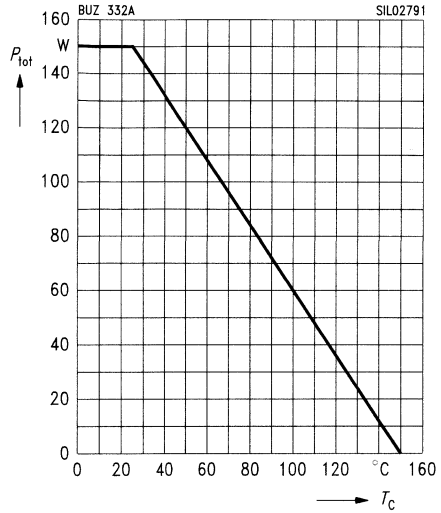
Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	600	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 600 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	µA
Drain-source on-resistance V_{GS} = 10 V, I_D = 5.0 A	$R_{DS(on)}$				Ω
BUZ 332		–	0.7	0.8	
BUZ 332 A		–	0.8	0.9	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 5.0 A	g_{fs}	5.0	8.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1400	2100	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	180	270	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	65	100	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{CC} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	20	30	ns
	t_r	–	70	110	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{CC} = 30 V, V_{GS} = 10 V, I_D = 3.07 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	250	330	
	t_f	–	80	100	

Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

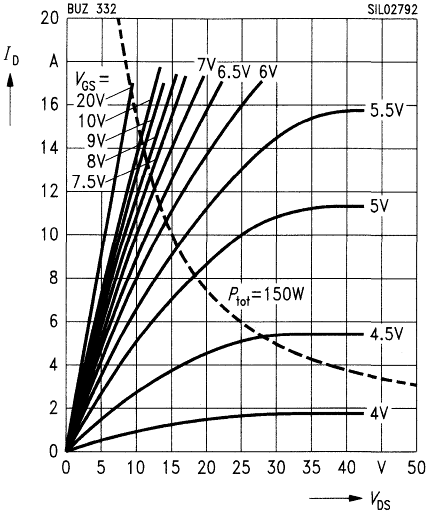
Parameter		Symbol	Values			Unit
			min.	typ.	max.	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 ˚C	BUZ 332		–	–	8.5	
	BUZ 332 A		–	–	8.0	
Pulsed reverse drain current		I_{SM}	–			
T_C = 25 ˚C	BUZ 332			–	34	
	BUZ 332 A			–	32	
Diode forward on-voltage I_S = 16 A, V_{GS} = 0 V		V_{SD}	–	1.1	1.2	V
Reverse recovery time V_R = 100 V, I_F = I_S , di_F / dt = 100 A/µs		t_{rr}	–	480	–	ns
Reverse recovery charge V_R = 100 V, I_F = I_S , di_F / dt = 100 A/µs		Q_{rr}	–	6.5	–	µC

Characteristics at T_j = 25 ˚C, unless otherwise specified.

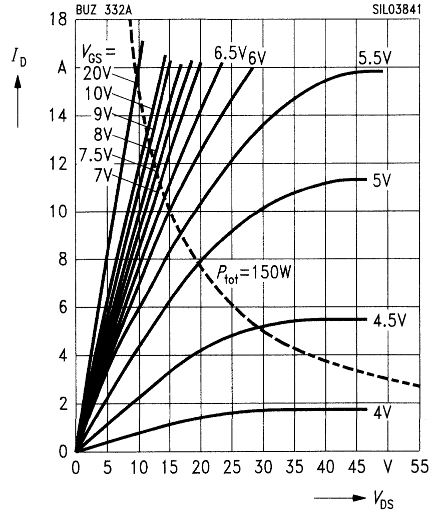
Total power dissipation
$P_{tot} = f(T_C)$



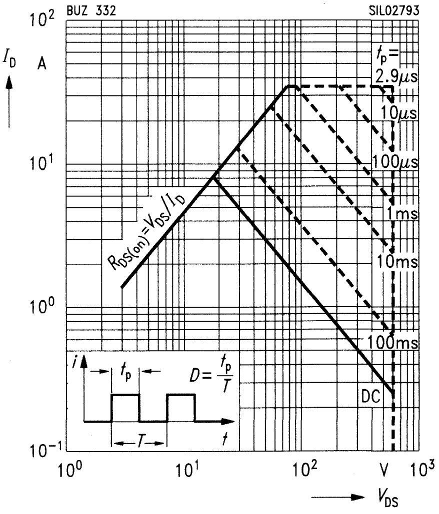
Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 332**
parameter: t_p = 80 µs



Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 332 A**
parameter: t_p = 80 µs

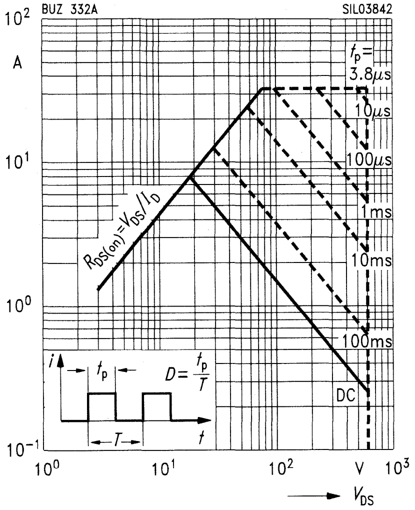


Safe operating area
$I_D = f(V_{DS})$ **BUZ 332**
parameter: D = 0.01, T_C = 25 ˚C



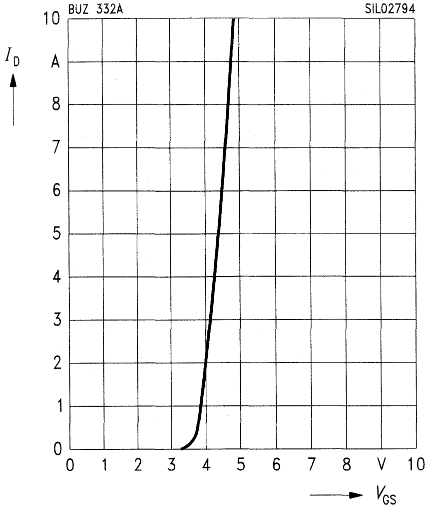
Safe operating area

$I_D = f(V_{DS})$ **BUZ 332 A**
parameter: $D = 0.01$, $T_C = 25\ ^\circ C$



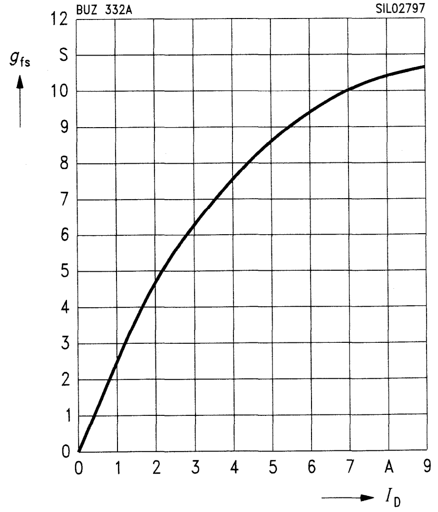
Typ. transfer characteristics

$I_D = f(V_{GS})$
parameter: t_p = 80 µs, V_{DS} = 25 V



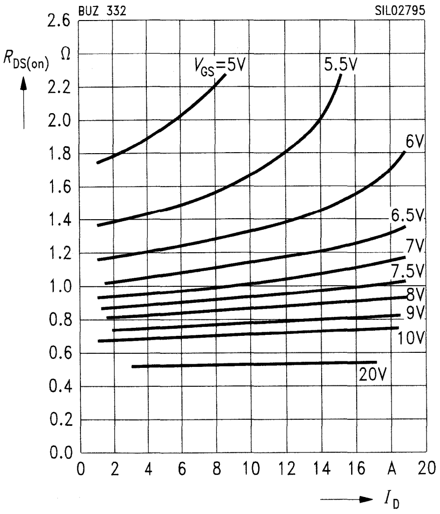
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: t_p = 80 µs



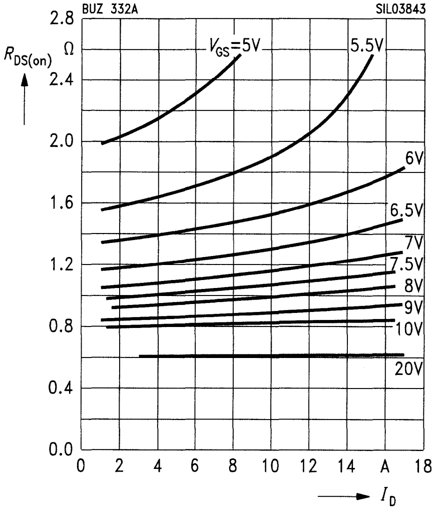
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$ **BUZ 332**
parameter: V_{GS}



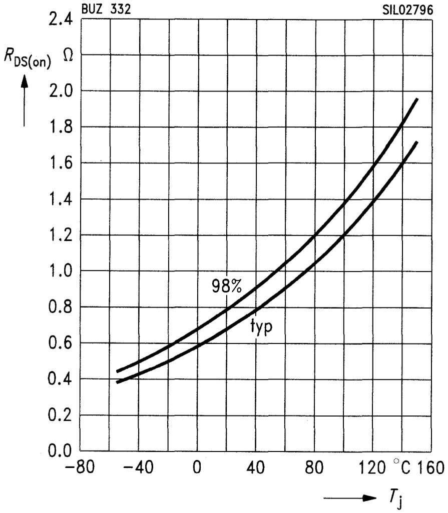
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 332 A**
parameter: V_{GS}



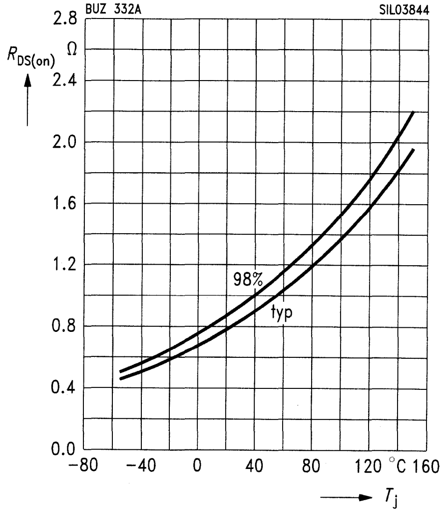
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 332**
parameter: I_D = 5 A, V_{GS} = 10 V, (spread)



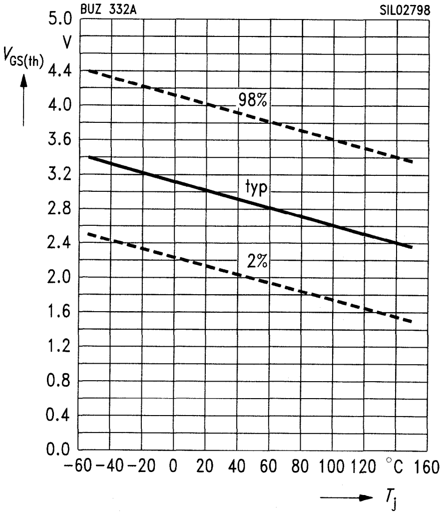
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 332 A**
parameter: I_D = 5 A, V_{GS} = 10 V, (spread)



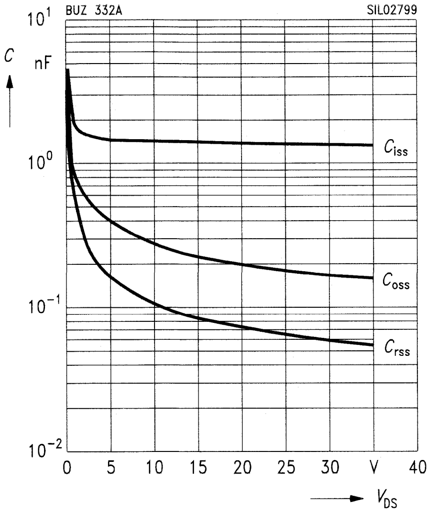
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



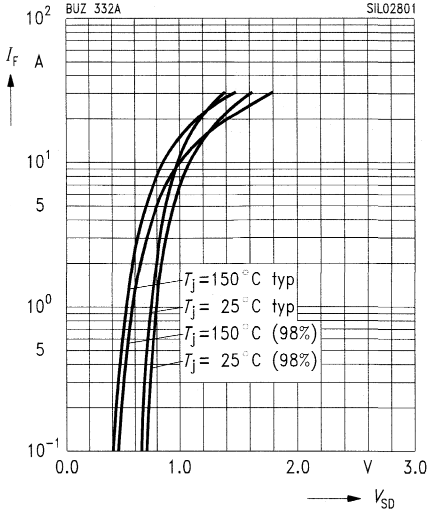
Typ. capacitances

$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Forward characteristics of reverse diode

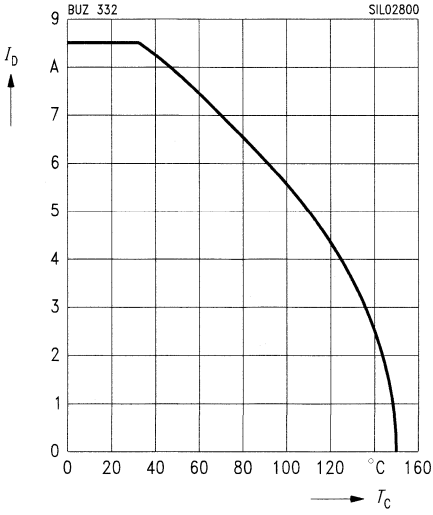
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs, (spread)



Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V

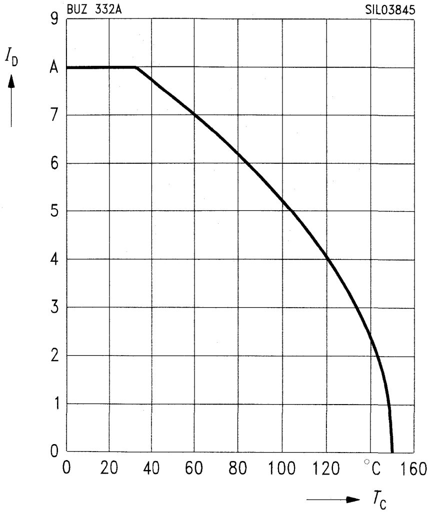
BUZ 332



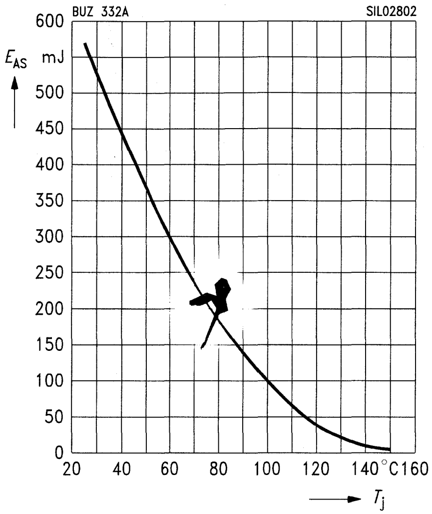
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V

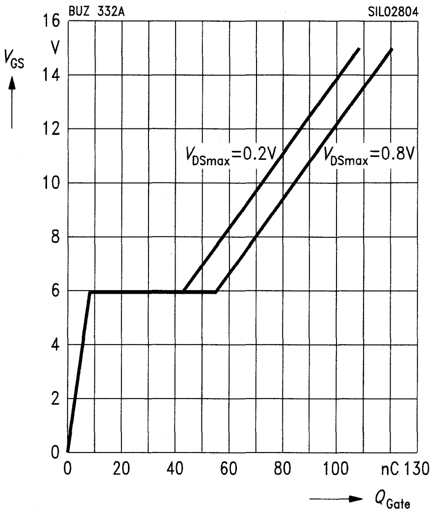
BUZ 332 A



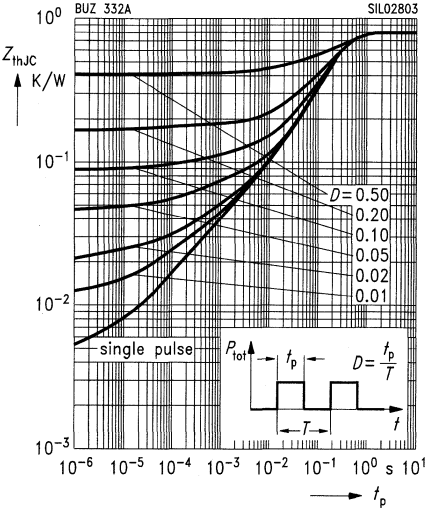
Avalanche energy $E_{AS} = f(T_j)$
parameter: I_D = 8 A, V_{DD} = 50 V
R_{GS} = 25 Ω, L = 16.3 mH



Typ. gate charge
$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls}$ = 33.0 A



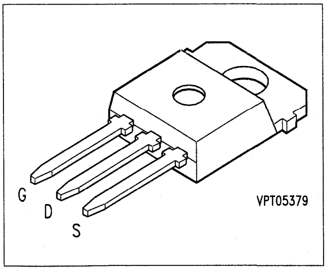
Transient thermal impedance
$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



SIPMOS® Power Transistor

BUZ 334

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 334	600 V	12 A	0.5 Ω	TO-218 AA	C67078-S3130-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, $T_C = 26\ ^\circ C$	I_D	**12**	A
Pulsed drain current, $T_C = 25\ ^\circ C$	$I_{D\ puls}$	**48**	
Avalanche current, limited by $T_{j\ max}$	I_{AR}	**12**	
Avalanche energy, periodic limited by $T_{j\ (max)}$	E_{AR}	**18**	mJ
Avalanche energy, single pulse $I_D = 12$ A, $V_{DD} = 50$ V, $R_{GS} = 25\ \Omega$ $L = 11.8$ mH, $T_j = 25\ ^\circ C$	E_{AS}	**930**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, $T_C = 25\ ^\circ C$	P_{tot}	**180**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\ JC}$	**≤ 0.7**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	600	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 600 V, V_{GS} = 0 V T_j = 25 ˚C T_j = 125 ˚C	I_{DSS}	 – –	 0.1 100	 1.0 1000	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 7.5 A	$R_{DS(on)}$	–	0.45	0.5	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 7.5 A	g_{fs}	8.0	13.5	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	2500	3350	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	300	450	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	100	150	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	40	60	ns
	t_r	–	100	150	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	450	600	
	t_f	–	120	160	

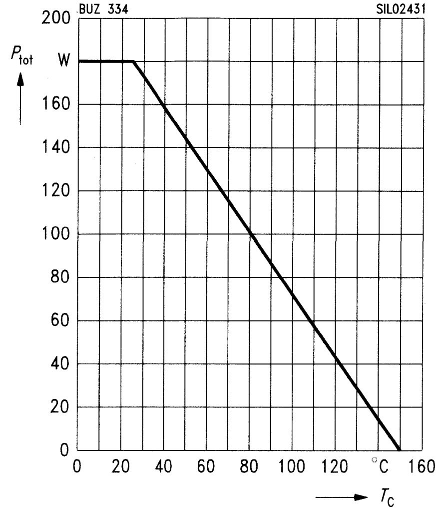
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	12	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	48	
Diode forward on-voltage I_S = 24 A, V_{GS} = 0 V	V_{SD}	–	1.0	1.6	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	140	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.5	–	µC

Characteristics at T_j = 25 ˚C, unless otherwise specified.

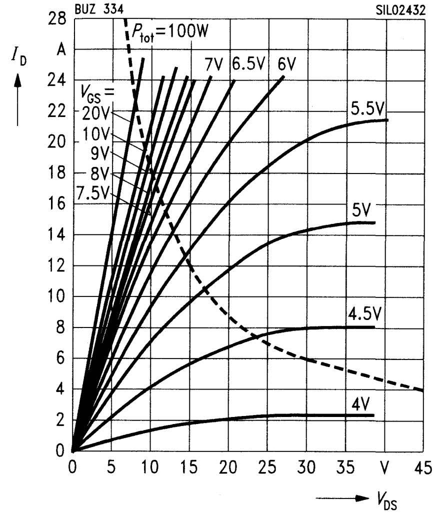
Total power dissipation

$P_{tot} = f(T_C)$



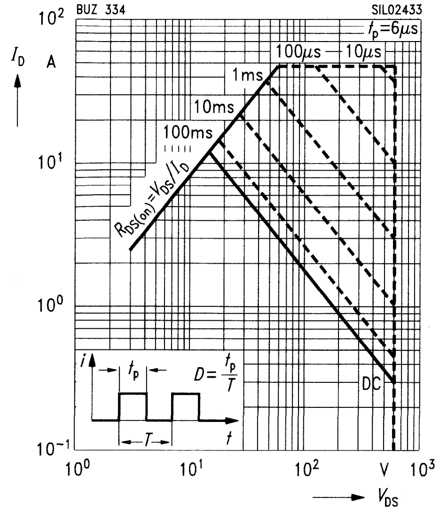
Typ. output characteristics

$I_D = f(V_{DS})$
parameter: t_p = 80 µs



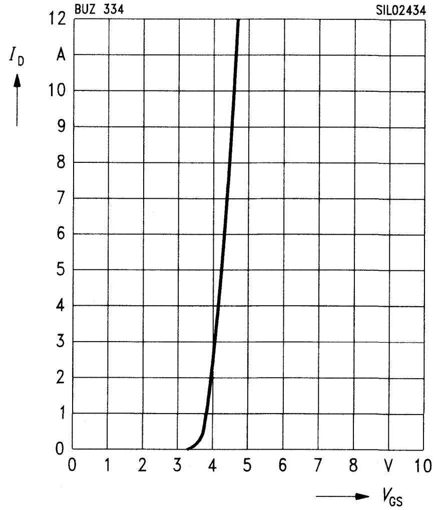
Safe operating area

$I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 ˚C



Typ. transfer characteristics

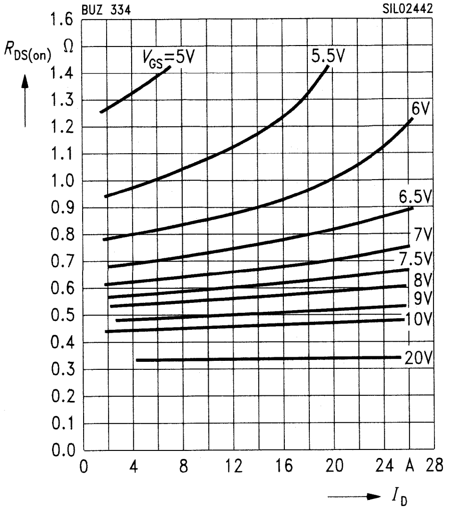
$I_D = f(V_{GS})$
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

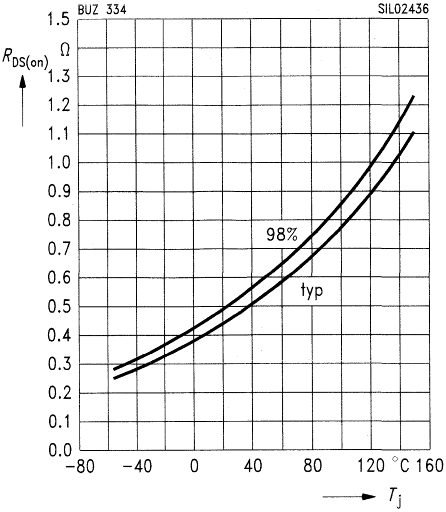
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

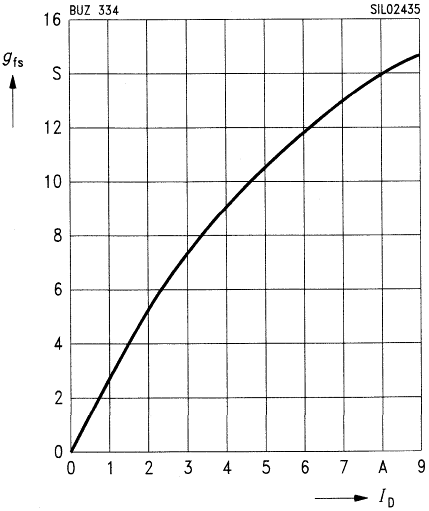
parameter: I_D = 7.5 A, V_{GS} = 10 V, (spread)



Typ.forward transconductance

$g_{fs} = f\,(I_D)$

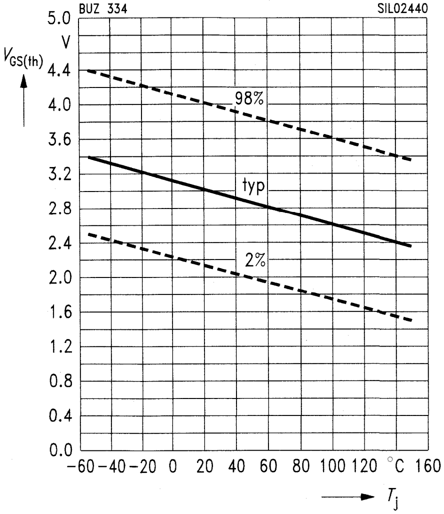
parameter: t_p = 80 µs



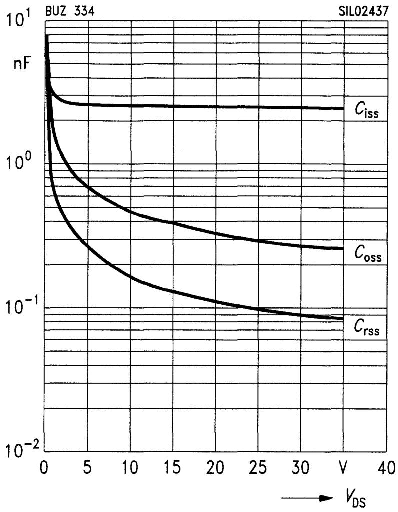
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

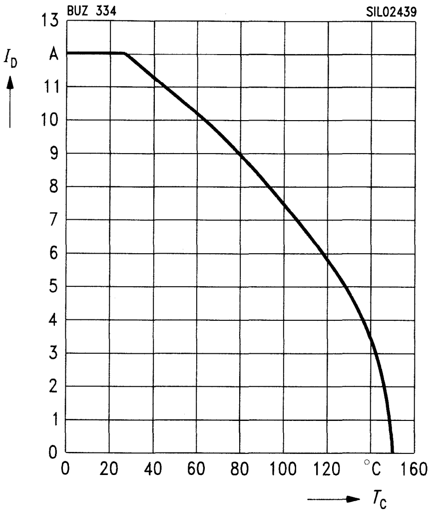
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



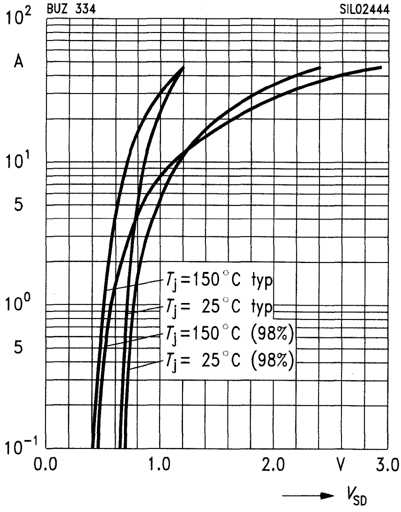
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



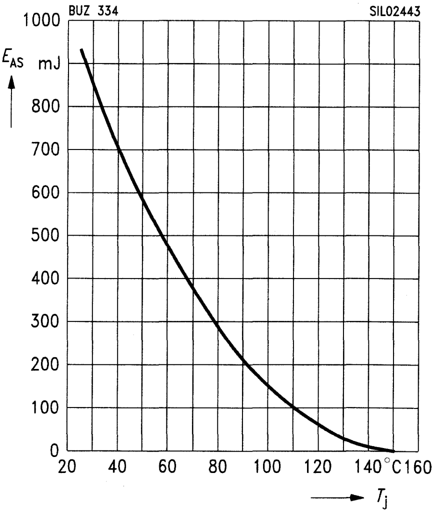
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j , $t_p = 80$ µs



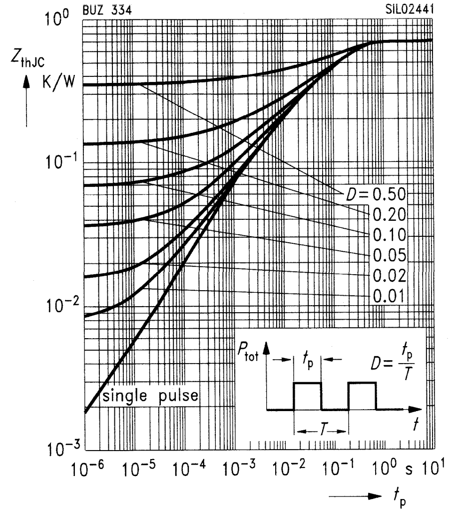
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 12$ A, $V_{DD} = 50$ V
$R_{GS} = 25\ \Omega$, $L = 11.8$ mH



Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

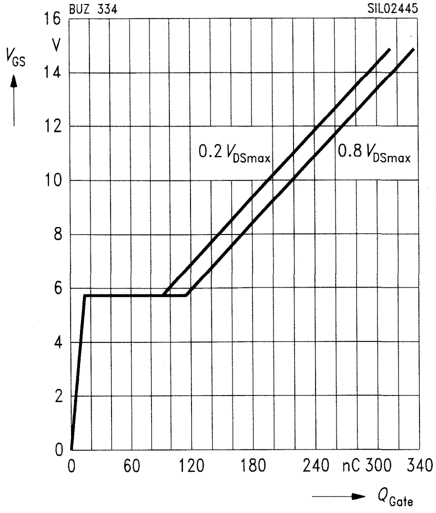
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{Gate})$

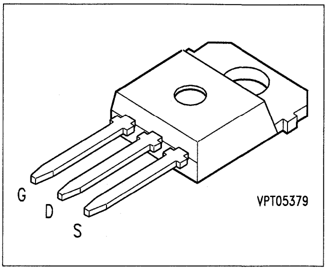
parameter: $I_{D\,puls} = 18.0$ A



SIPMOS® Power Transistor

BUZ 338

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 338	500 V	13.5 A	0.4 Ω	TO-218 AA	C67078-S3126-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 28 °C	I_D	**13.5**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**54**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**13.5**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**18**	mJ
Avalanche energy, single pulse I_D = 13.5 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 9.09 mH, T_j = 25 °C	E_{AS}	**920**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**180**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 0.7**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\ DSS}$	500	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\ (th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 500 V, V_{GS} = 0 V T_j = 25 ˚C T_j = 125 ˚C	I_{DSS}	 – –	 0.1 100	 1.0 1000	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 8.5 A	$R_{DS\ (on)}$	–	0.3	0.4	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 8.5 A	g_{fs}	8.0	15	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	2500	3325	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	320	480	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	120	180	
Turn-on time t_{on} , ($t_{on} = t_{d\ (on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_{GS} = 50 Ω	$t_{d\ (on)}$	–	40	60	ns
	t_r	–	100	150	
Turn-off time t_{off} , ($t_{off} = t_{d\ (off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_{GS} = 50 Ω	$t_{d\ (off)}$	–	450	600	
	t_f	–	120	160	

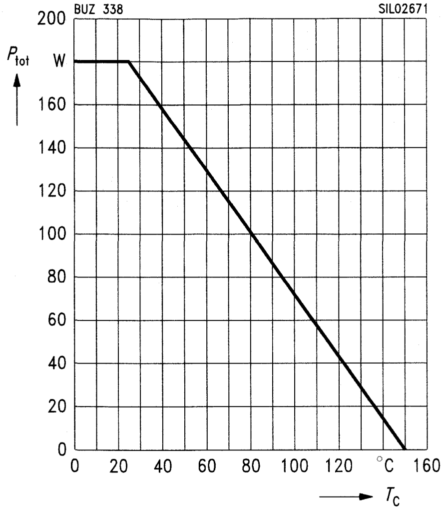
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	13.5	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	54	
Diode forward on-voltage I_S = 27 A, V_{GS} = 0 V	V_{SD}	–	1.1	1.6	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	400	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	6.2	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

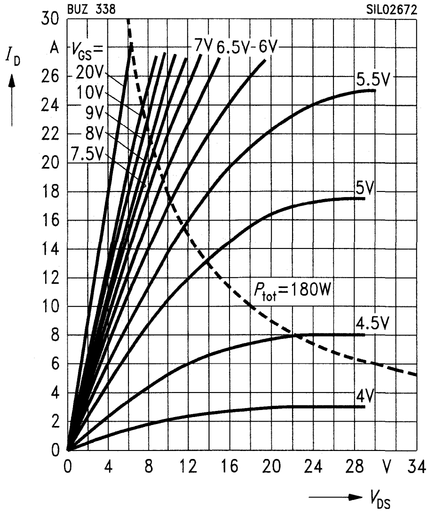
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

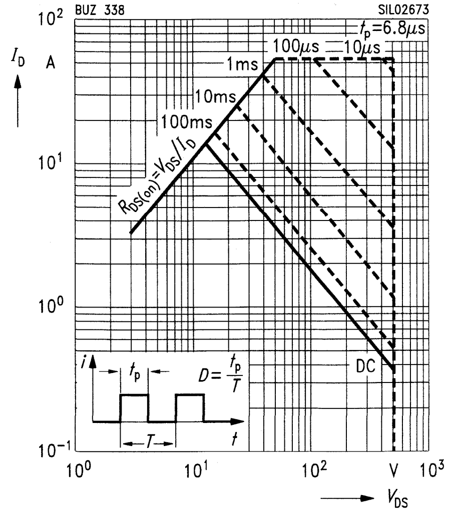
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

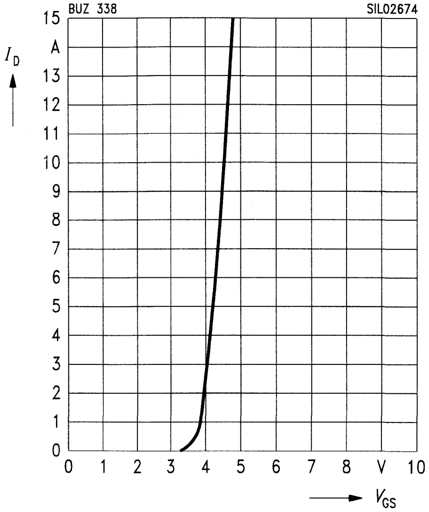
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

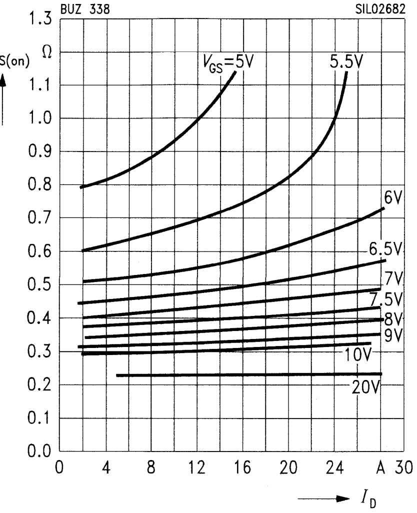
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

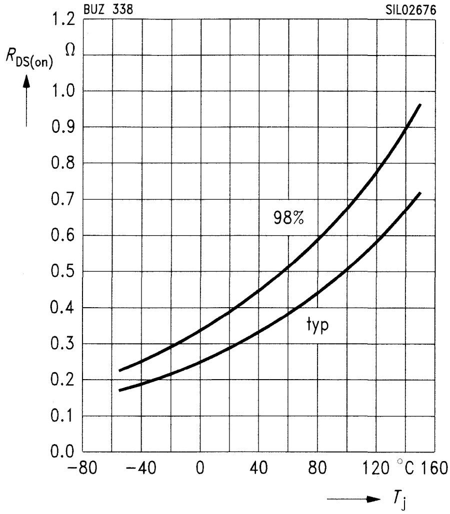
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

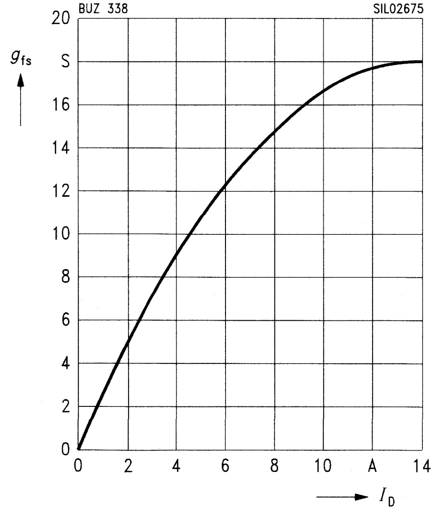
parameter: I_D = 8.5 A, V_{GS} = 10 V, (spread)



Typ.forward transconductance

$g_{fs} = f\,(I_D)$

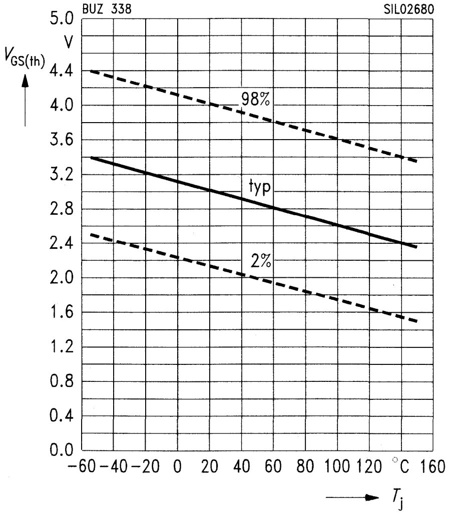
parameter: t_p = 80 µs



Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

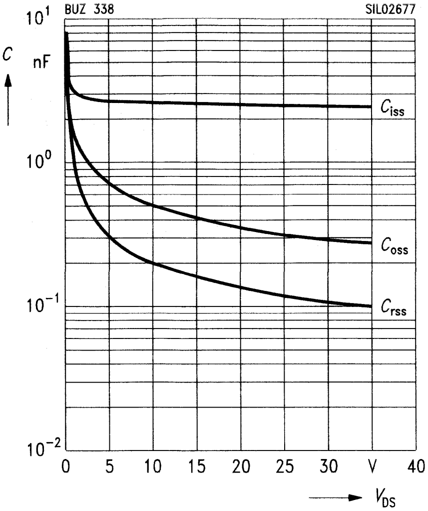
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

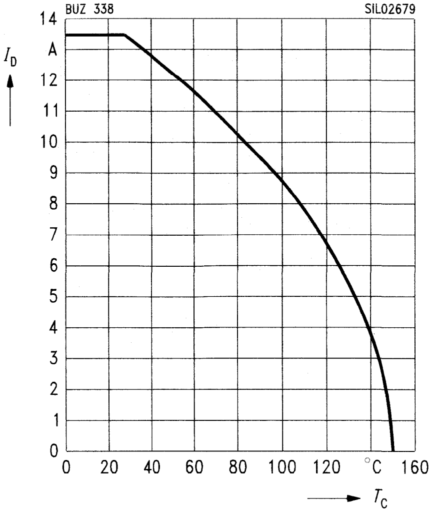
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$)

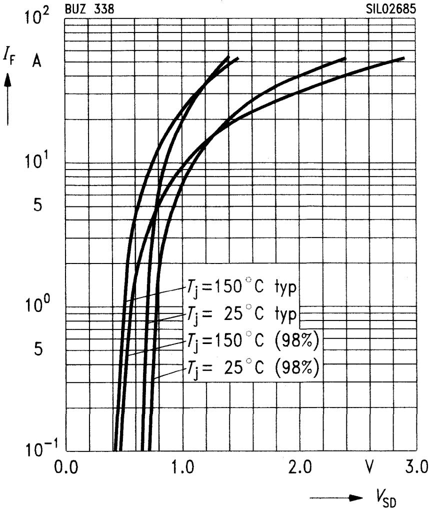
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

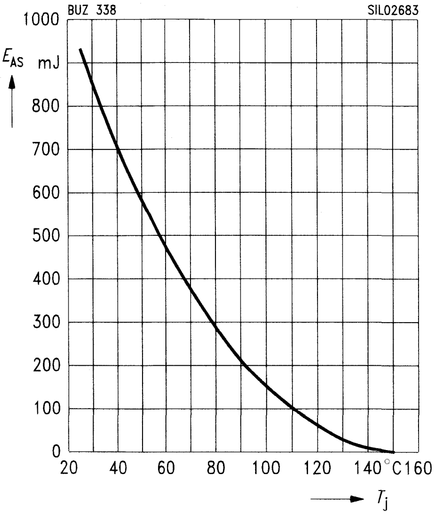
parameter: T_j , $t_p = 80$ µs



Avalanche energy $E_{AS} = f(T_j)$

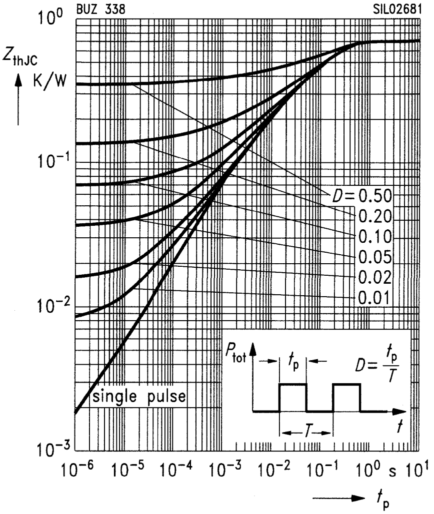
parameter: $I_D = 13.5$ A, $V_{DD} = 50$ V

$R_{GS} = 25$ Ω, $L = 9.09$ mH



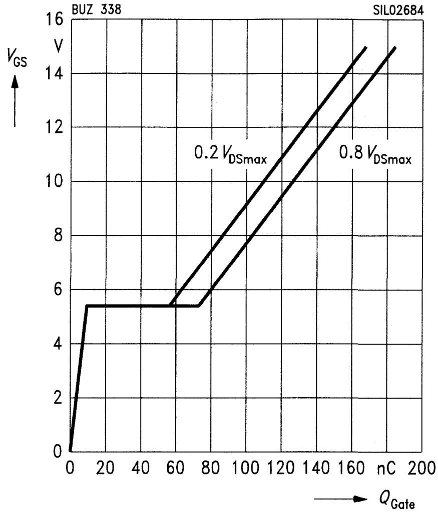
Transient thermal impedance

$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls}$ = 20.3 A

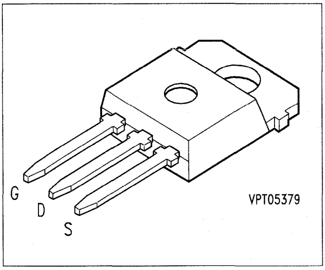


SIEMENS

SIPMOS® Power Transistor

BUZ 339

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	**Package** [1]	**Ordering Code**
BUZ 339	500 V	11.5 A	0.5 Ω	TO-218 AA	C67078-S3133-A2

Maximum Ratings

Parameter	**Symbol**	**Values**	**Unit**
Continuous drain current, T_C = 33 ˚C	I_D	**11.5**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**46**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**11.5**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**16**	mJ
Avalanche energy, single pulse I_D = 11.5 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 10.8 mH, T_j = 25 ˚C	E_{AS}	**790**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 ˚C	P_{tot}	**170**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 0.74**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	500	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 500 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 ˚C		–	0.1	1.0	
T_j = 125 ˚C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 7.5 A	$R_{DS\,(on)}$	–	0.4	0.5	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 7.5 A	g_{fs}	8	14	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	2200	3000	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	260	400	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	100	150	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	35	50	ns
	t_r	–	70	100	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	450	680	
	t_f	–	110	160	

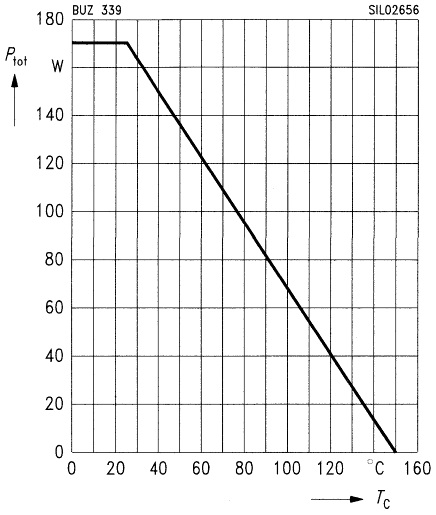
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	11.5	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	46	
Diode forward on-voltage I_S = 23 A, V_{GS} = 0 V	V_{SD}	–	1.1	1.5	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	450	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	7.6	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Total power dissipation

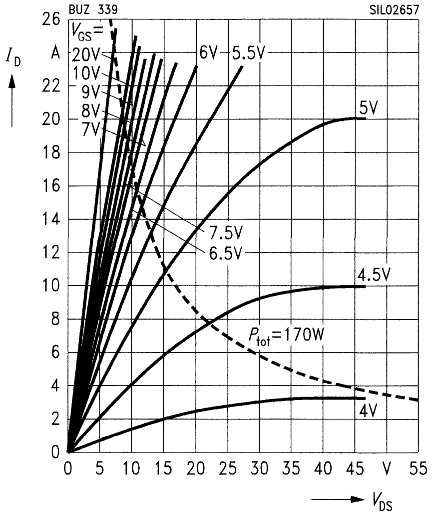
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

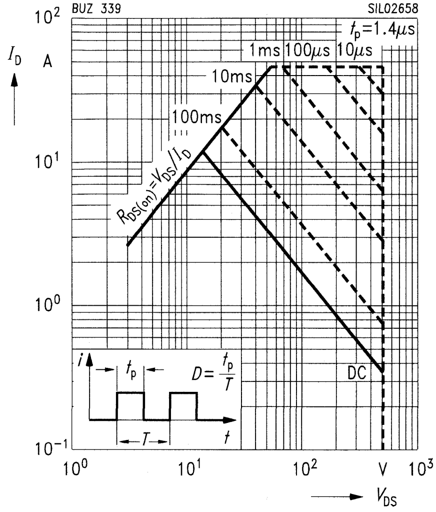
parameter: $t_p = 80$ µs



Safe operating area

$I_D = f(V_{DS})$

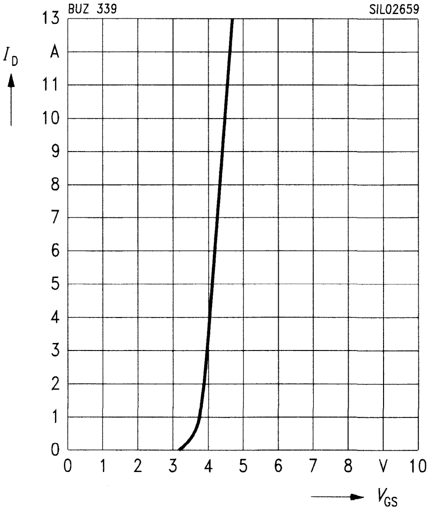
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

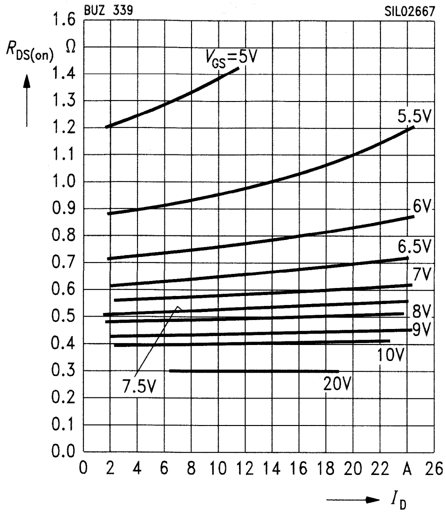
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

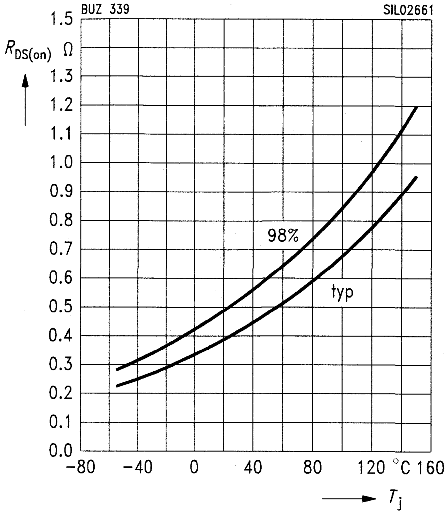
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

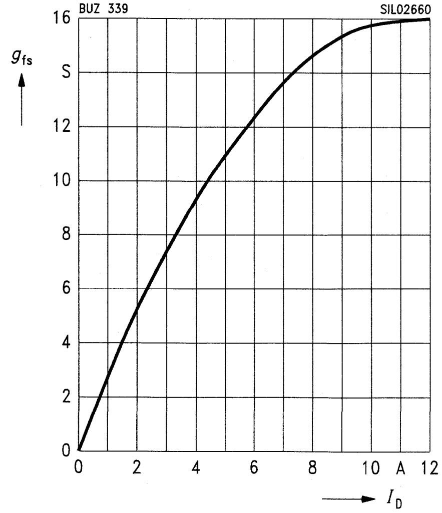
parameter: I_D = 7.5 A, V_{GS} = 10 V, (spread)



Typ.forward transconductance

$g_{fs} = f\,(I_D)$

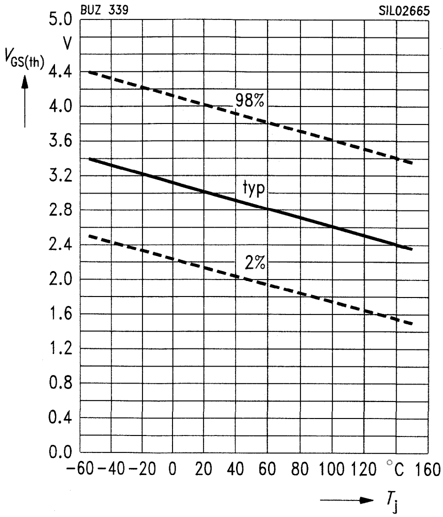
parameter: t_p = 80 µs



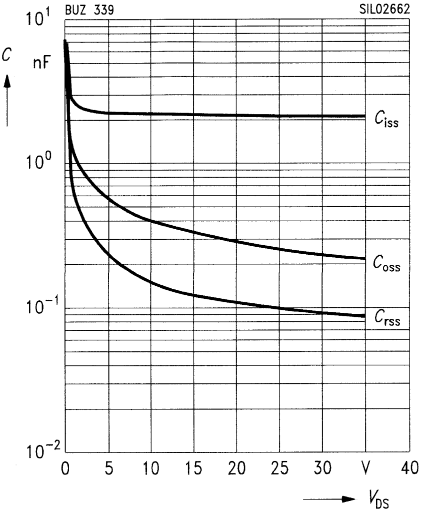
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

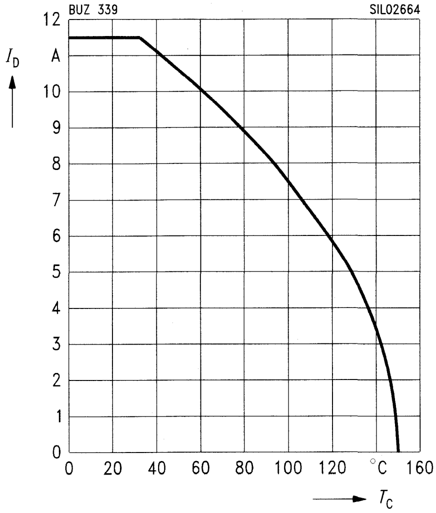
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



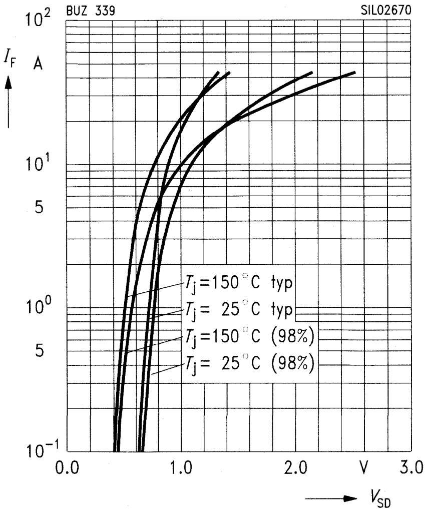
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



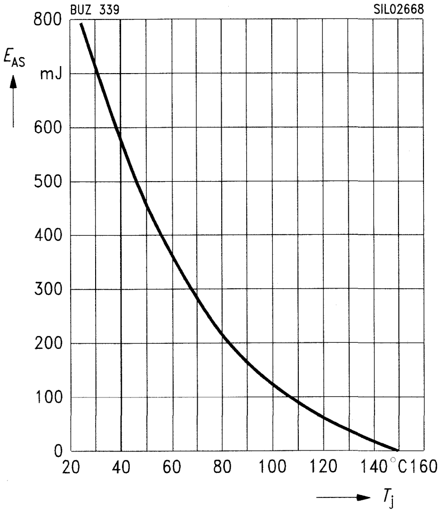
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs



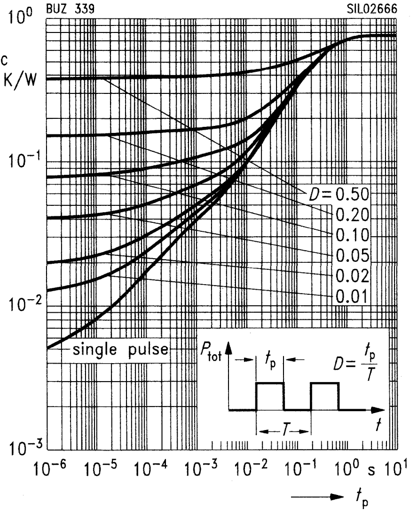
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 11.5$ A, $V_{DD} = 50$ V
$R_{GS} = 25\ \Omega$, $L = 10.8$ mH



Transient thermal impedance

$Z_{\text{th JC}} = f\,(t_p)$

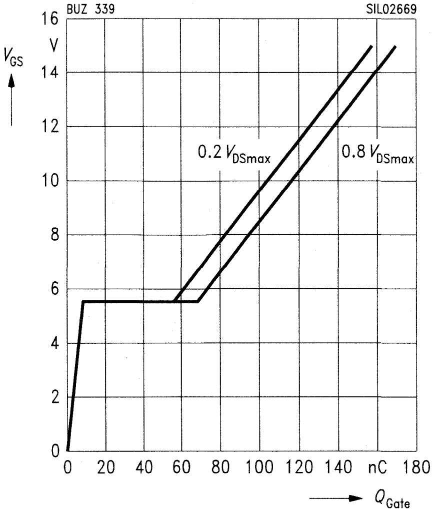
parameter: $D = t_p / T$



Typ. gate charge

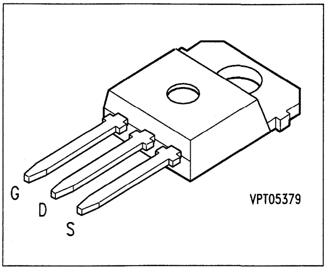
$V_{GS} = f\,(Q_{\text{Gate}})$

parameter: $I_{\text{D puls}} = 17.3$ A



SIPMOS® Power Transistor **BUZ 341**

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package[1]	Ordering Code
BUZ 341	200 V	33 A	0.07 Ω	TO-218 AA	C67078-S3128-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 28 °C	I_D	**33**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**132**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**33**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**16**	mJ
Avalanche energy, single pulse I_D = 33 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 1.09 mH, T_j = 25 °C	E_{AS}	**790**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**170**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 0.74**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	200	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 200 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 21 A	$R_{DS\,(on)}$	–	0.06	0.07	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 21 A	g_{fs}	15	23	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	2600	3900	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	500	750	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	230	350	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	40	60	ns
	t_r	–	110	170	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	450	680	
	t_f	–	160	240	

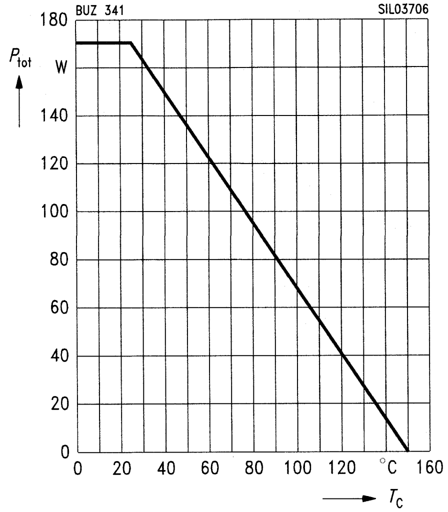
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	**typ.**	**max.**	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	33	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	132	
Diode forward on-voltage I_S = 66 A, V_{GS} = 0 V	V_{SD}	–	1.3	1.6	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	230	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	1.8	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

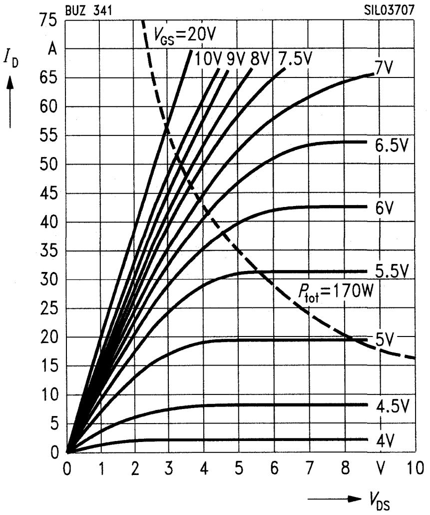
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

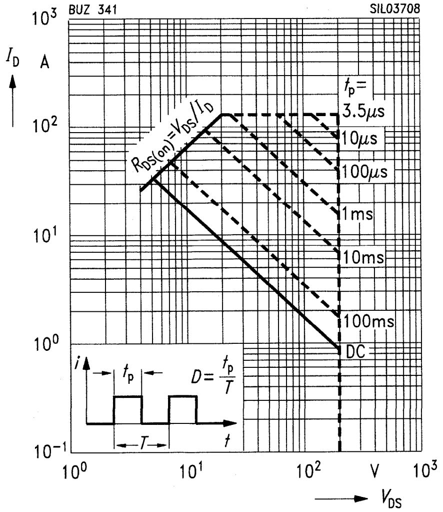
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

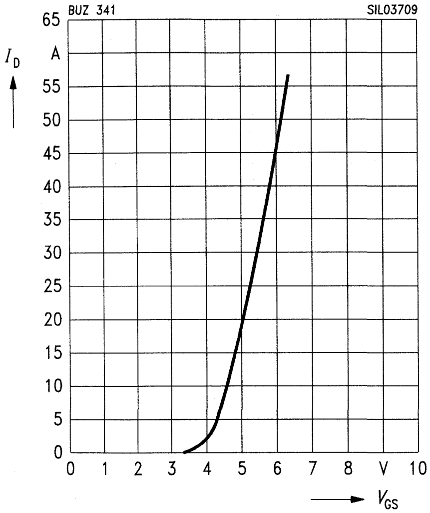
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

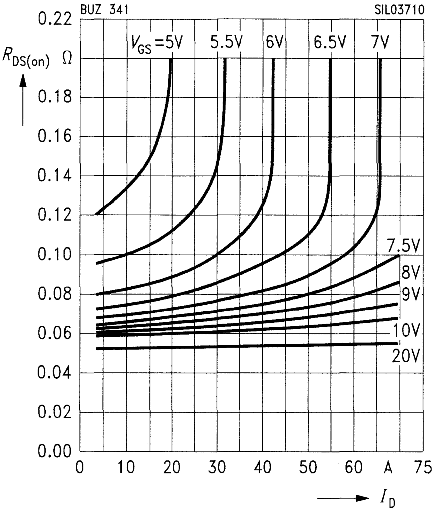
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

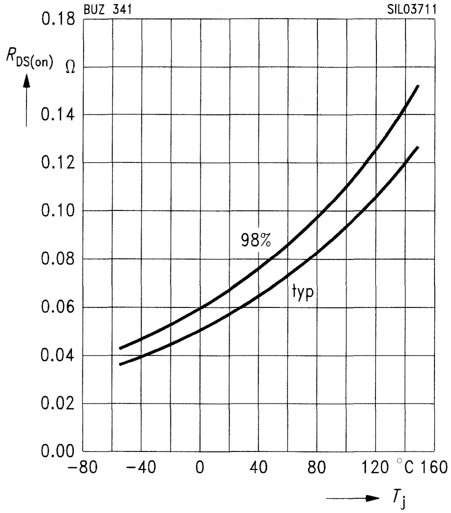
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

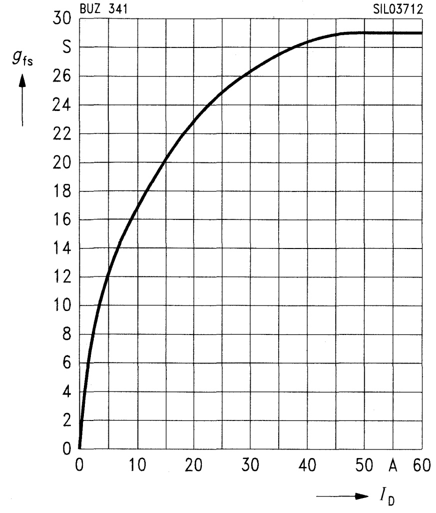
parameter: I_D = 21 A, V_{GS} = 10 V, (spread)



Typ.forward transconductance

$g_{fs} = f\,(I_D)$

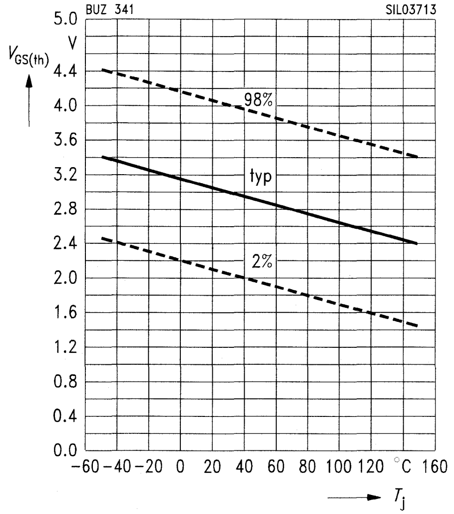
parameter: t_p = 80 µs



Gate threshold voltage

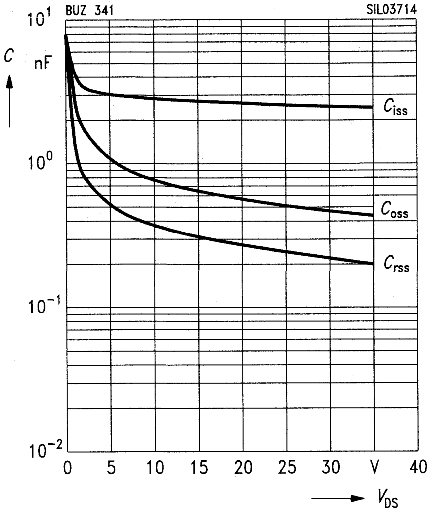
$V_{GS\,(th)} = f\,(T_j)$

parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



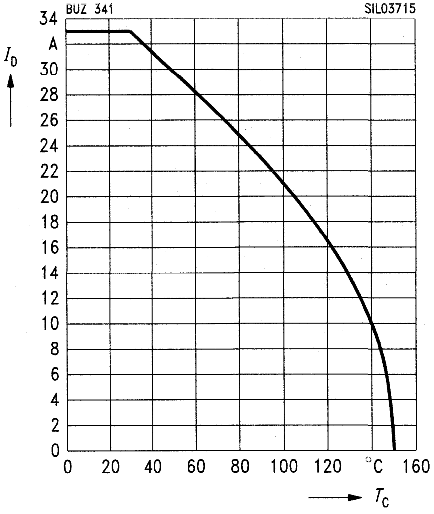
Typ. capacitances

$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



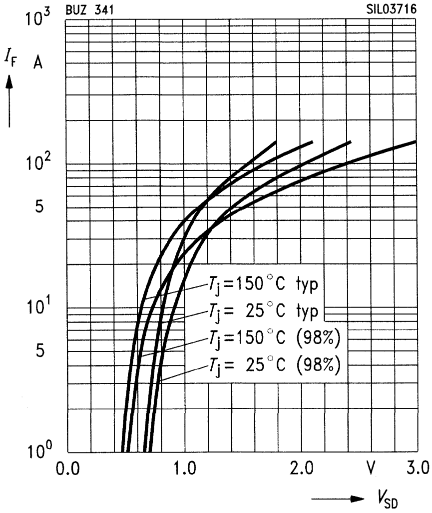
Drain current

$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



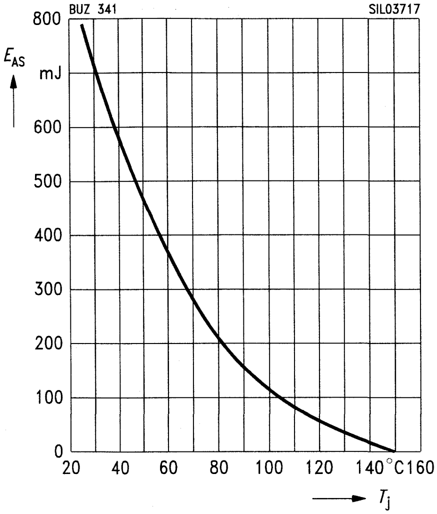
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: $t_p = 80$ µs, T_j



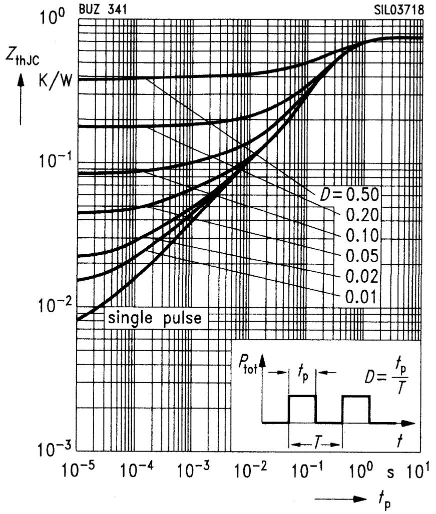
Avalanche energy $E_{AS} = f(T_j)$

parameter: $I_D = 33$ A, $V_{DD} = 50$ V
$R_{GS} = 25\ \Omega$, $L = 1.09$ mH



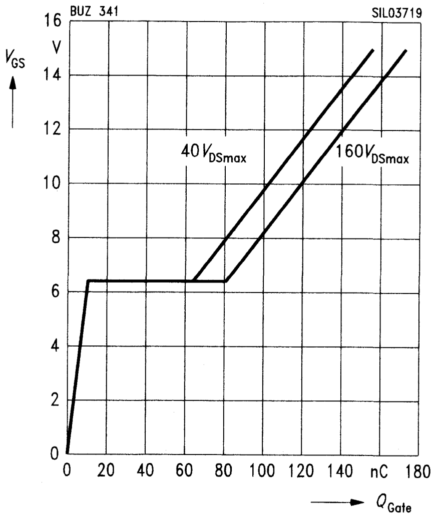
Transient thermal impedance

$Z_{\mathrm{th\,JC}} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

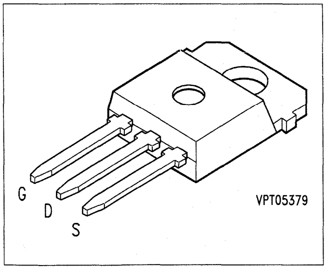
$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 49.5$ A



SIPMOS® Power Transistor

BUZ 344

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1)]	Ordering Code
BUZ 344	100 V	50 A	0.035 Ω	TO-218 AA	C67078-S3132-A2

Maximum Ratings

Parameter	Symbol	Value	Unit
Continuous drain current, T_C = 25 °C	I_D	**50**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**200**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**50**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**18.5**	mJ
Avalanche energy, single pulse I_D = 50 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 240 µH, T_j = 25 °C	E_{AS}	**400**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**170**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 0.74**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	100	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 100 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 32 A	$R_{DS(on)}$	–	0.03	0.035	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 32 A	g_{fs}	15	28	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	2400	3200	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	730	1100	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	430	650	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	33	50	ns
	t_r	–	140	210	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	500	670	
	t_f	–	230	310	

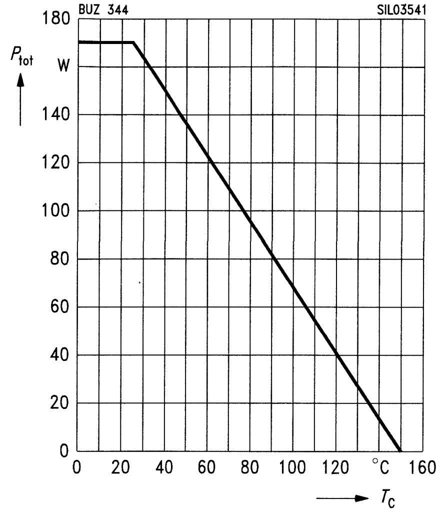
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	50	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	200	
Diode forward on-voltage I_S = 100 A, V_{GS} = 0 V	V_{SD}	–	1.6	1.8	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	170	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.9	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Total power dissipation

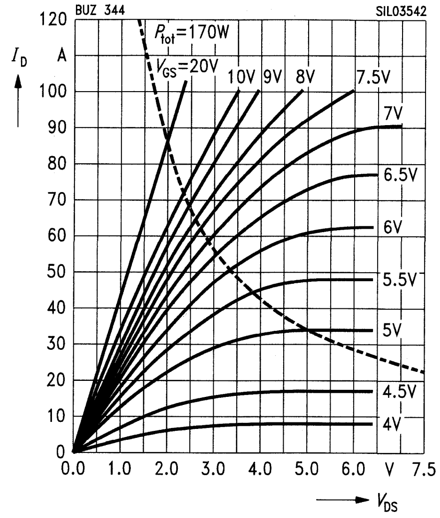
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

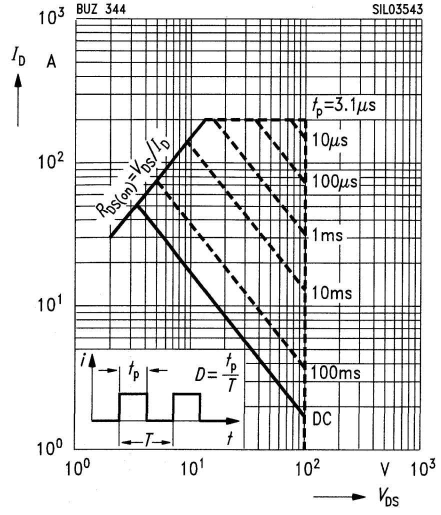
parameter: $t_p = 80$ µs



Safe operating area

$I_D = f(V_{DS})$

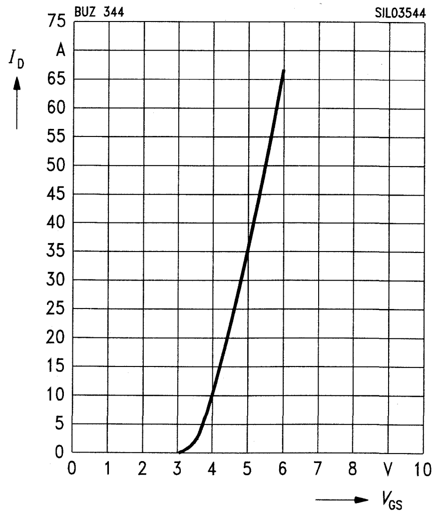
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

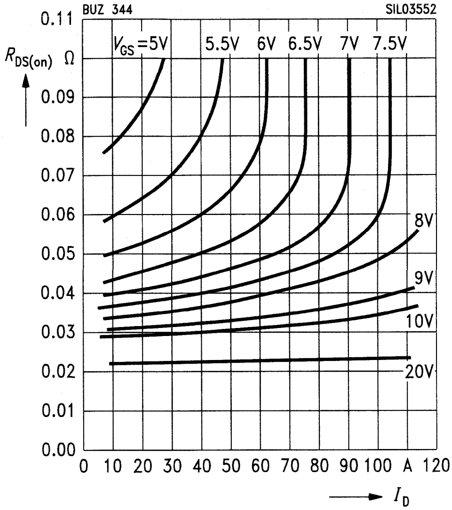
$I_D = f(V_{GS})$

parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



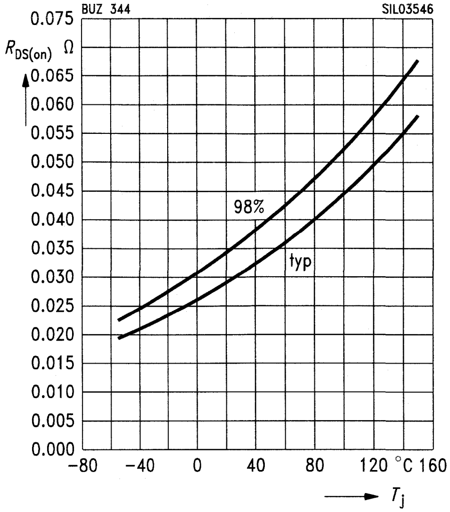
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



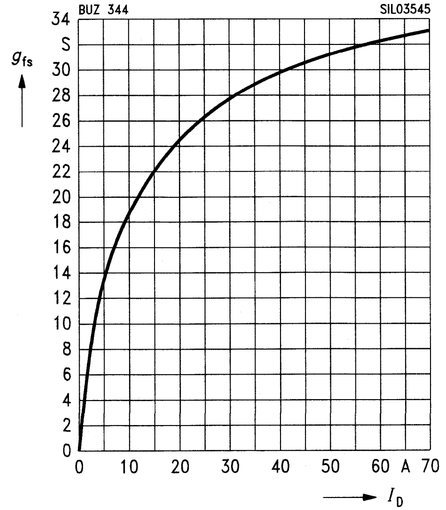
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 32 A, V_{GS} = 10 V, (spread)



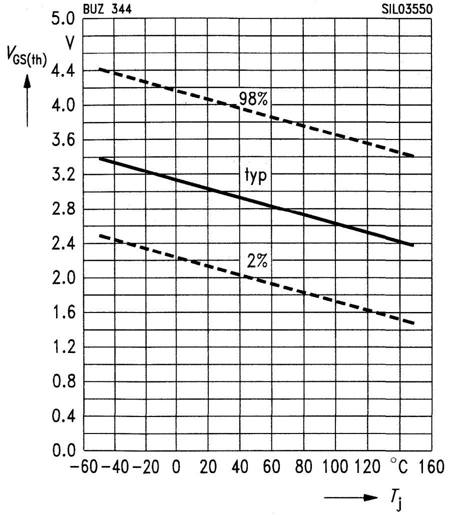
Typ.forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs

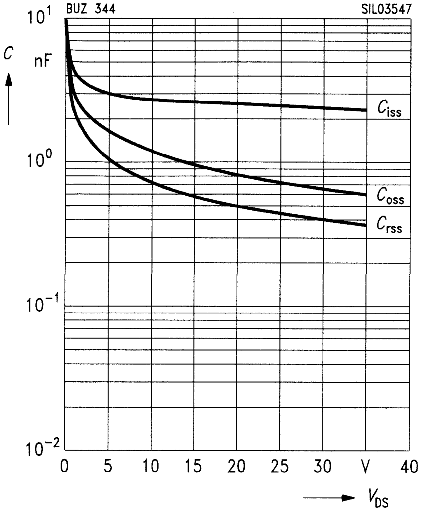


Gate threshold voltage

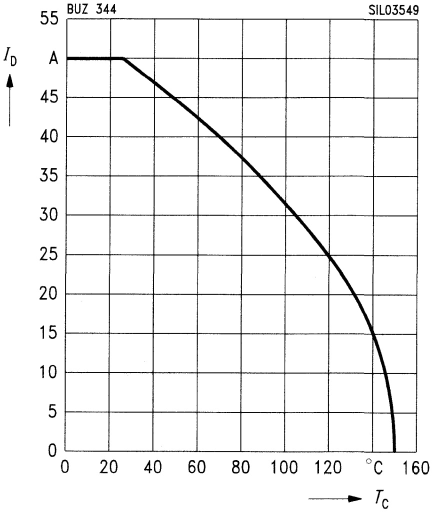
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



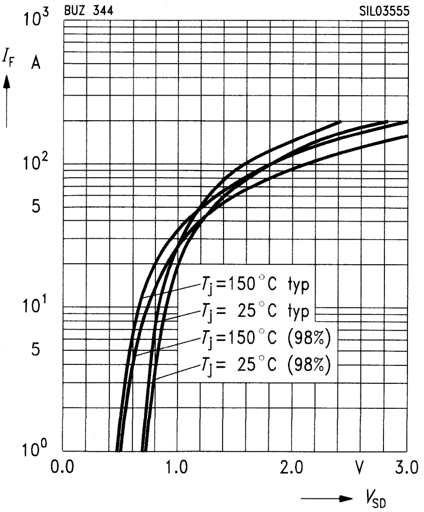
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



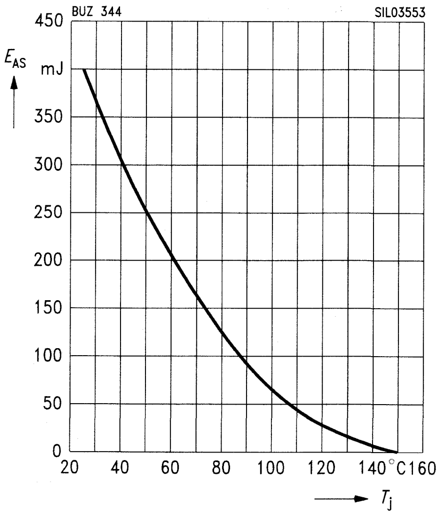
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: $t_p = 80$ µs, T_j



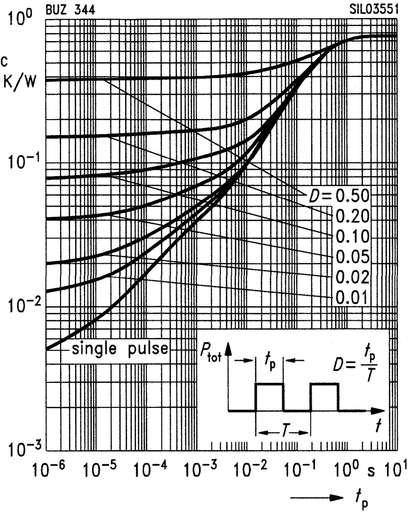
Avalanche energy $E_{AS} = f(T_j)$
parameter: $I_D = 50$ A, $V_{DD} = 25$ V
$R_{GS} = 25\ \Omega$, $L = 240$ µH



Transient thermal impedance

$Z_{th JC} = f(t_p)$

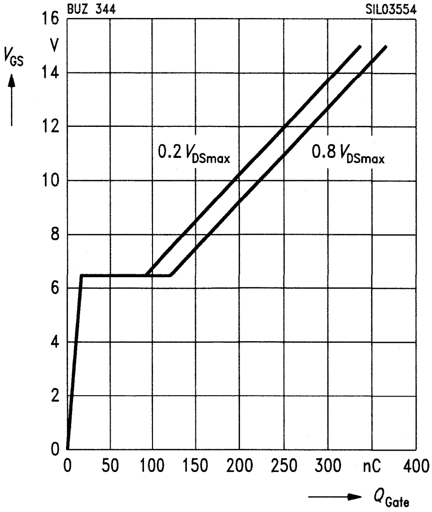
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{Gate})$

parameter: $I_{D puls} = 75$

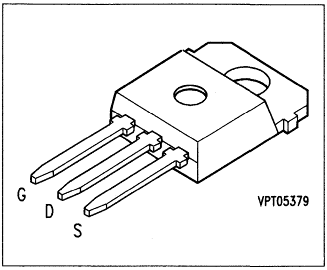


SIEMENS

SIPMOS® Power Transistor

BUZ 345

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 345	100 V	41 A	0.045 Ω	TO-218 AA	C67078-S3121-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 28 °C	I_D	**41**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**164**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**41**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**18**	mJ
Avalanche energy, single pulse I_D = 41 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 249.9 µH, T_j = 25 °C	E_{AS}	**280**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**150**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 0.83**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	100	–	–	V
Gate threshold voltage V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 100 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 26 A	$R_{DS(on)}$	–	0.040	0.045	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 26 A	g_{fs}	10	20	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1800	2700	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	560	840	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	270	400	
Turn-on time t_{on}, ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	30	45	ns
	t_r	–	110	165	
Turn-off time t_{off}, ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	300	390	
	t_f	–	150	195	

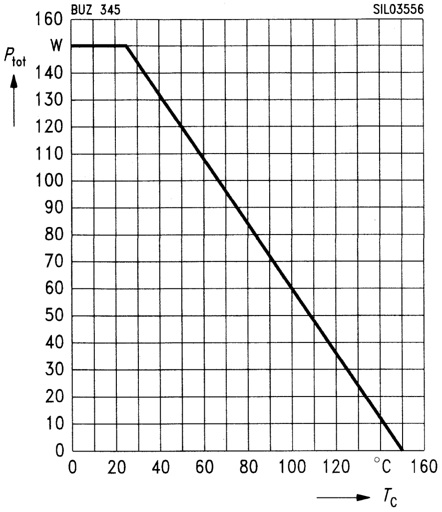
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	41	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	164	
Diode forward on-voltage I_S = 82 A, V_{GS} = 0 V	V_{SD}	–	1.6	1.8	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	120	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.6	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Total power dissipation

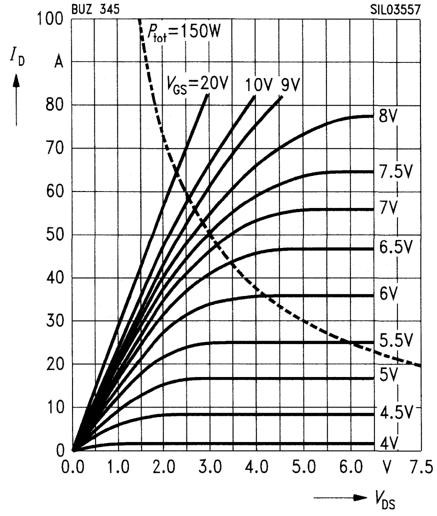
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

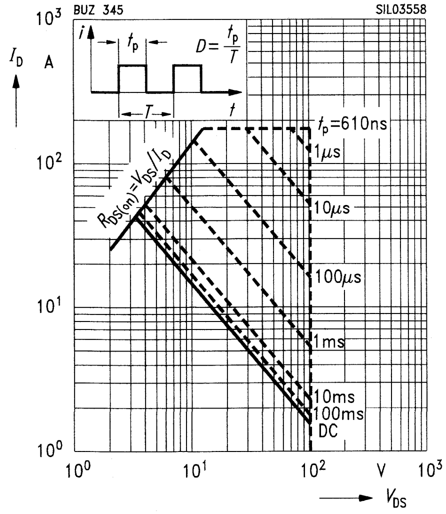
parameter: $t_p = 80$ µs



Safe operating area

$I_D = f(V_{DS})$

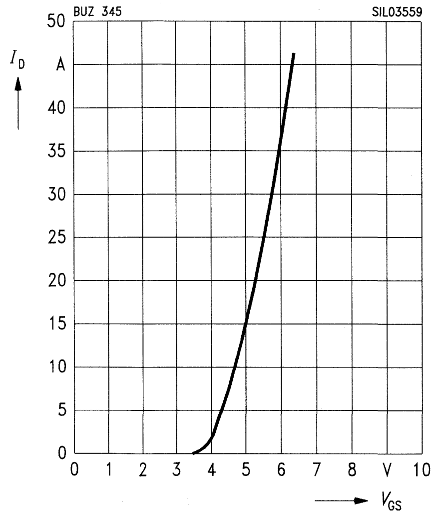
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

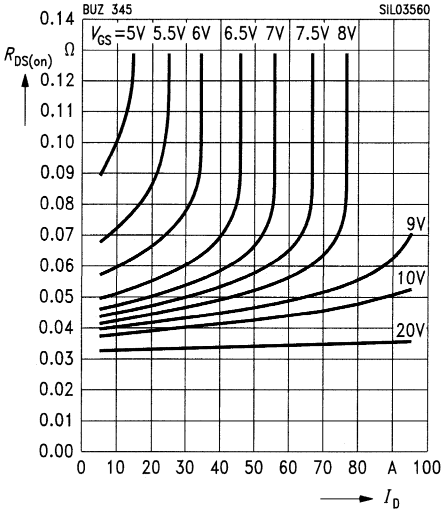
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

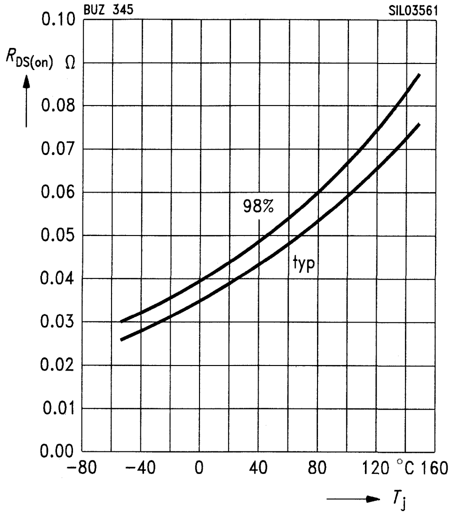
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

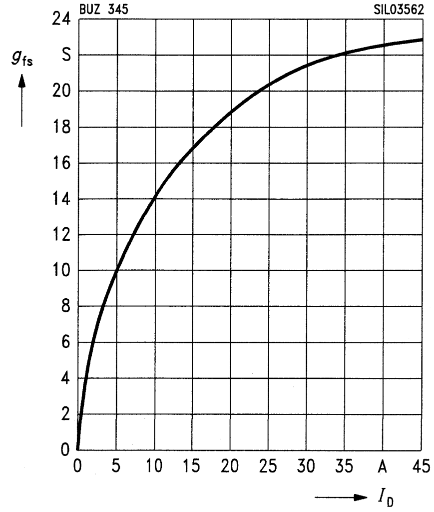
parameter: I_D = 26 A, V_{GS} = 10 V, (spread)



Typ.forward transconductance

$g_{fs} = f\,(I_D)$

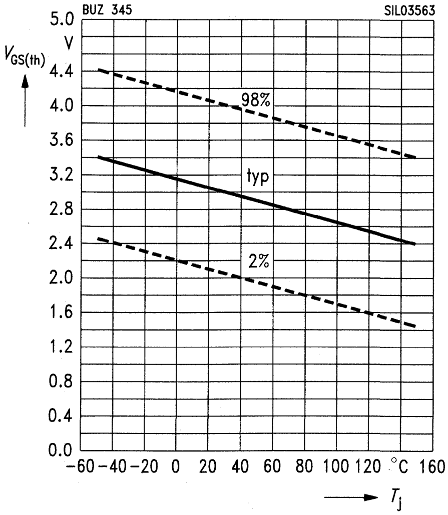
parameter: t_p = 80 µs



Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

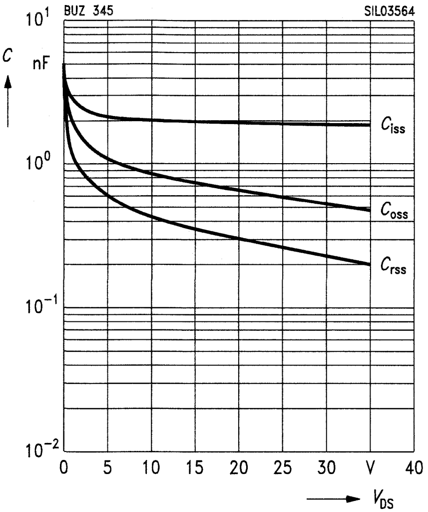
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

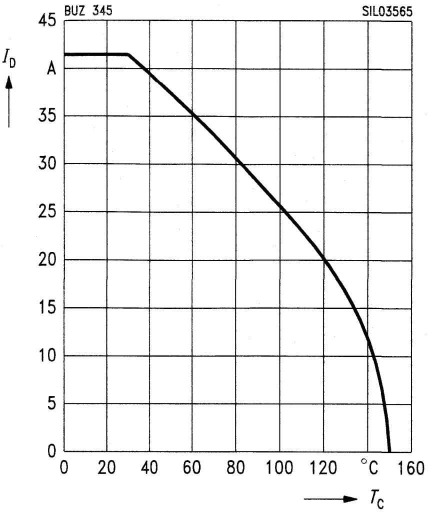
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

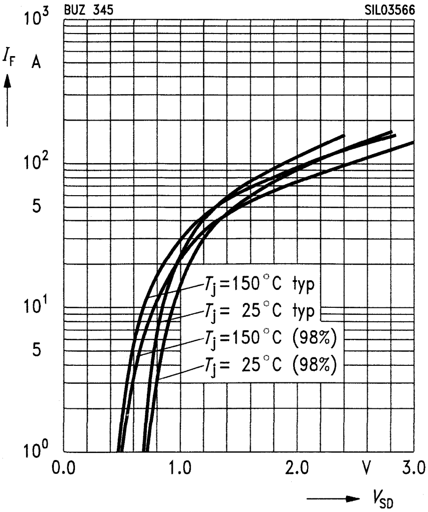
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

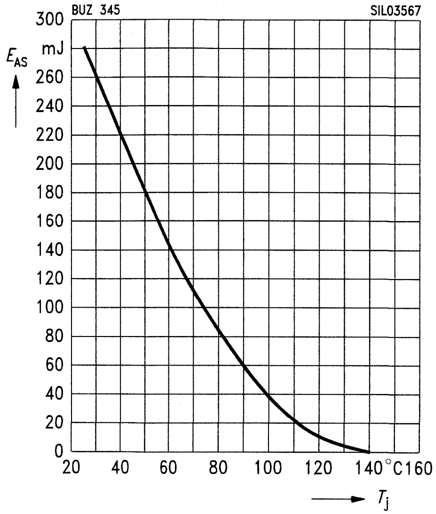
parameter: $t_p = 80$ µs, T_j



Avalanche energy $E_{AS} = f(T_j)$

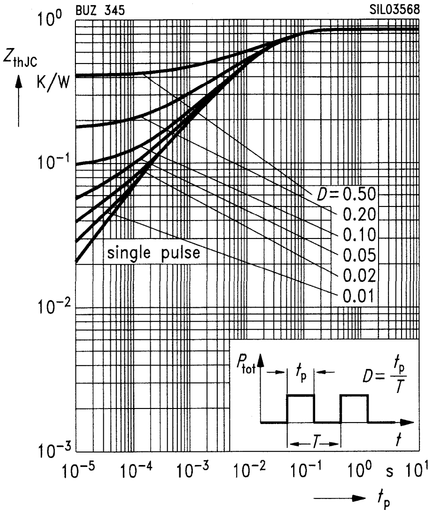
parameter: $I_D = 41$ A, $V_{DD} = 25$ V

$R_{GS} = 25\ \Omega$, $L = 249.9$ µH



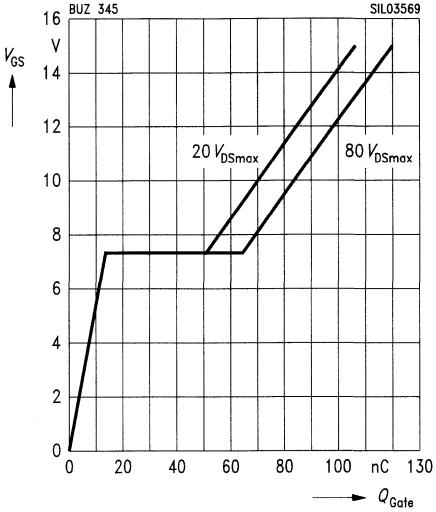
Transient thermal impedance

$Z_{\mathrm{th\,JC}} = f\,(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f\,(Q_{Gate})$
parameter: $I_{D\,puls} = 61.5$ A

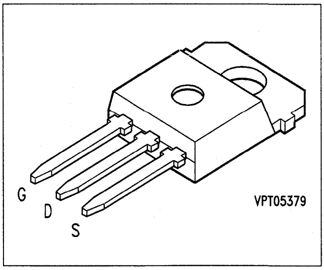


SIEMENS

SIPMOS® Power Transistors

BUZ 346
BUZ 346 S2

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	T_C	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 346	50 V	58 A	73 °C	0.018 Ω	TO-218 AA	C67078-S3120-A2
BUZ 346 S2	60 V	58 A	73 °C	0.018 Ω	TO-218 AA	C67078-S3120-A4

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		346	**346 S2**	
Continuous drain current	I_D	**58**		A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**232**		
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**58**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**4.5**		mJ
Avalanche energy, single pulse $I_D = 58$ A, $V_{DD} = 25$ V, $R_{GS} = 25\ \Omega$ $L = 21.4\ \mu H\ /\ 31.2\ \mu H$, $T_j = 25$ °C	E_{AS}	**72**		
Gate-source voltage	V_{GS}	**± 20**		V
Power dissipation, $T_C = 25$ °C	P_{tot}	**170**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 0.74**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

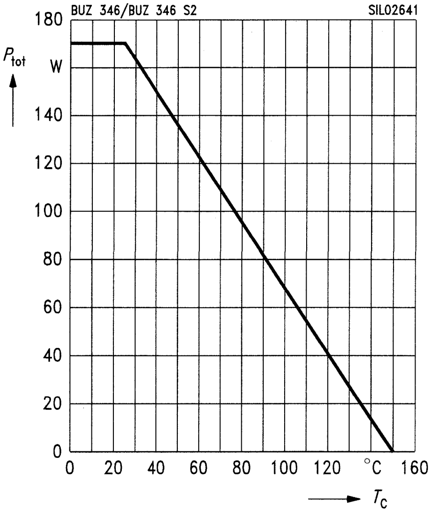
Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA BUZ 346 BUZ 346 S2	$V_{(BR)\,DSS}$	 50 60	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{GS} = 0 V, V_{DS} = 50 V BUZ 346 V_{DS} = 60 V BUZ 346 S2 T_j = 25 ˚C T_j = 125 ˚C	I_{DSS}	 – –	 0.1 10	 1.0 100	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 47 A	$R_{DS\,(on)}$	–	0.012	0.018	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 47 A	g_{fs}	30	42	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	2900	4300	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	1400	2100	
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	500	750	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	55	80	ns
	t_r	–	140	210	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3.0 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	420	560	
	t_f	–	250	330	

Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

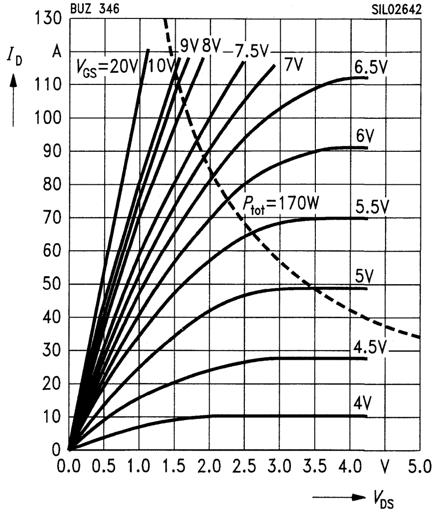
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	58	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	232	
Diode forward on-voltage I_S = 116 A, V_{GS} = 0 V	V_{SD}	–	1.6	2.0	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	100	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.3	–	µC

Characteristics at $T_j = 25$ °C, unless otherwise specified.

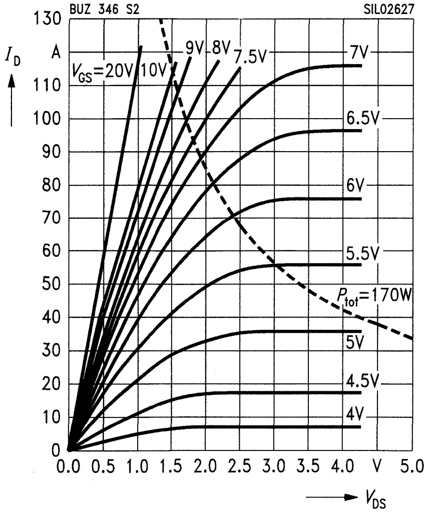
Total power dissipation
$P_{tot} = f(T_C)$



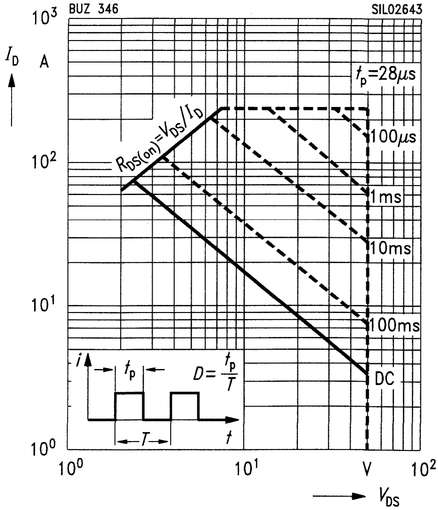
Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 346**
parameter: t_p = 80 µs



Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 346 S2**
parameter: t_p = 80 µs

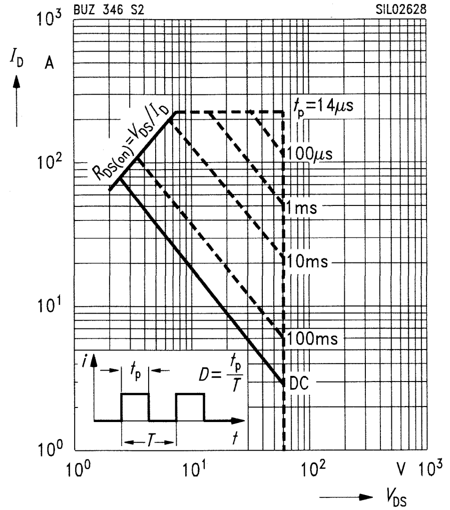


Safe operating area
$I_D = f(V_{DS})$ **BUZ 346**
parameter: D = 0.01, T_C = 25 °C



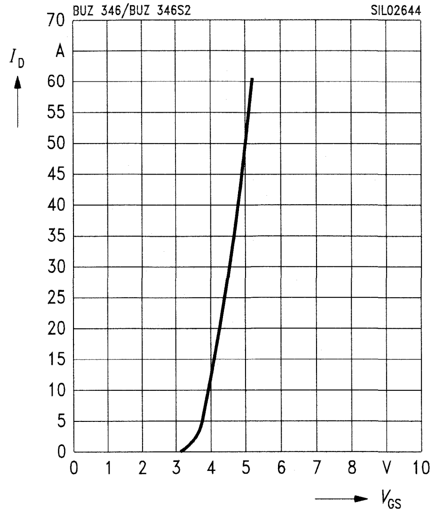
Safe operating area

$I_D = f(V_{DS})$ **BUZ 346 S2**
parameter: $D = 0.01$, $T_C = 25$ °C



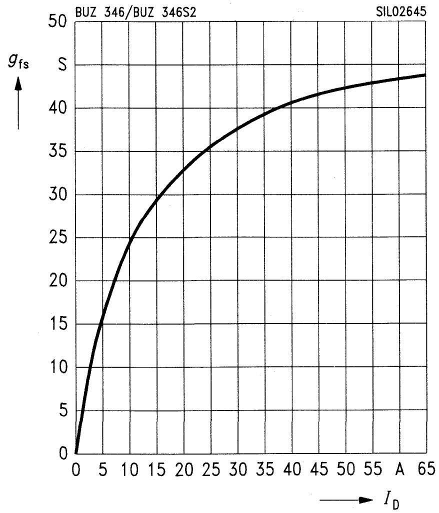
Typ. transfer characteristics

$I_D = f(V_{GS})$
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V



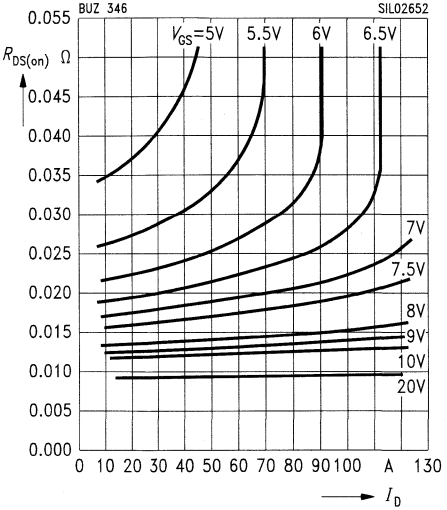
Typ.forward transconductance

$g_{fs} = f(I_D)$
parameter: $t_p = 80$ µs



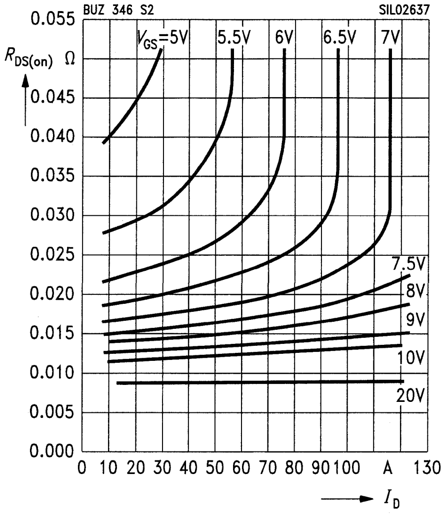
Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$ **BUZ 346**
parameter: V_{GS}



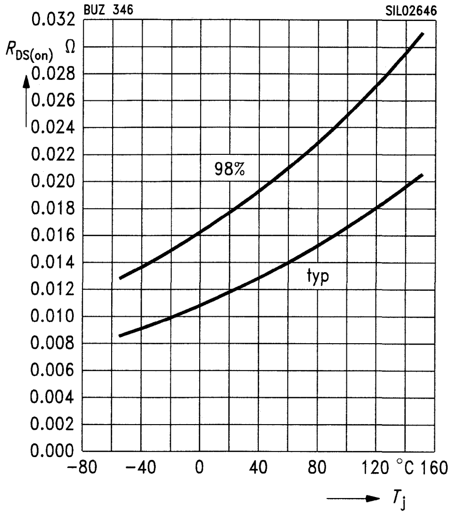
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 346 S2**
parameter: V_{GS}



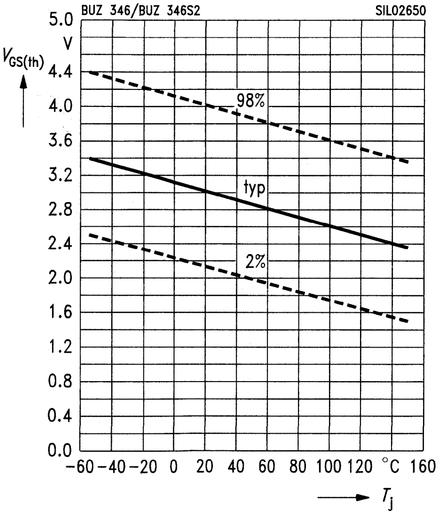
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 47 A, V_{GS} = 10 V, (spread)



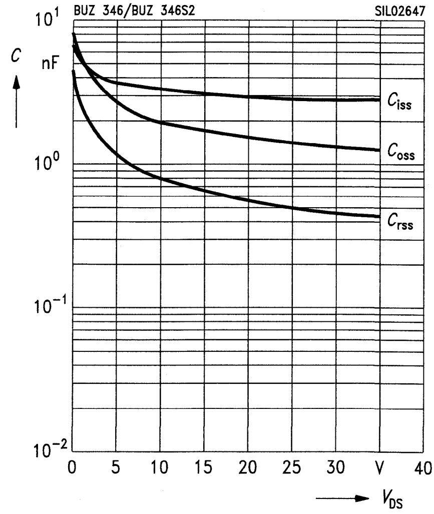
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)

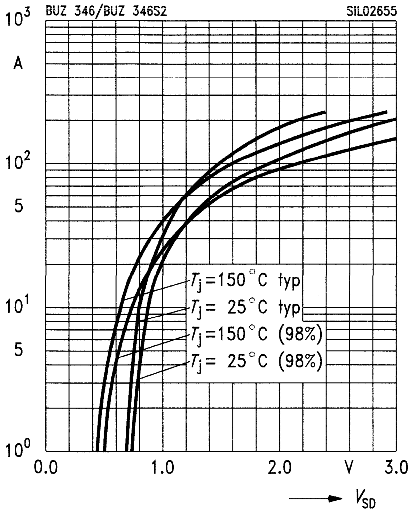


Typ. capacitances

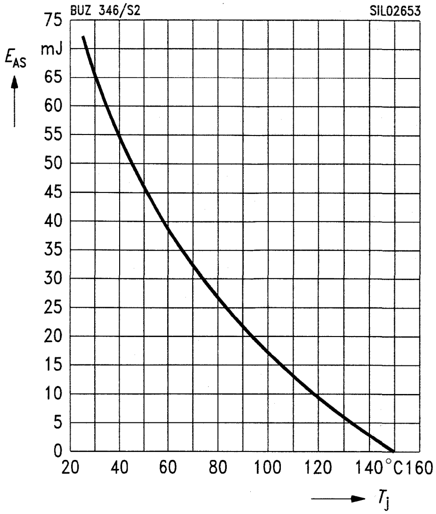
$C = f\,(V_{DS})$
parameter: V_{GS} = 0 V, f = 1 MHz



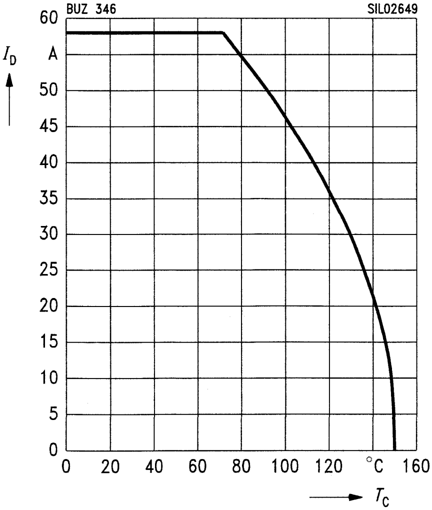
Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: t_p = 80 µs, T_j



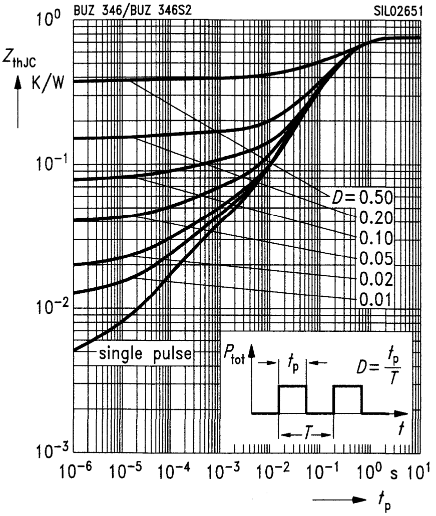
Avalanche energy $E_{AS} = f(T_j)$
parameter: I_D = 58 A, V_{DD} = 25 V
R_{GS} = 25 Ω, L = 21.4 µH



Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



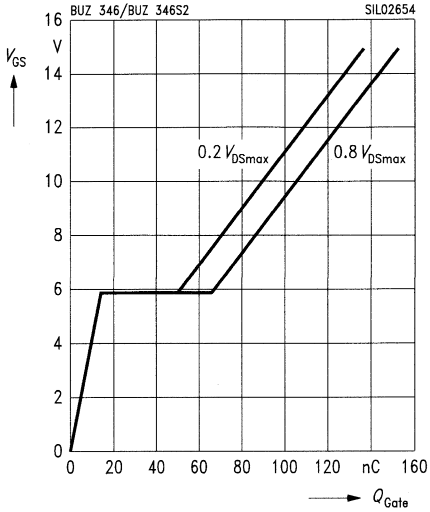
Transient thermal impedance
$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{Gate})$

parameter: $I_{D\,puls}$ = 87.0 A

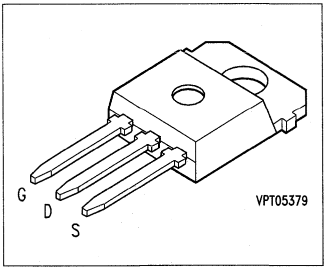


SIEMENS

SIPMOS® Power Transistor

BUZ 347

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 347	50V	45A	0.03 Ω	TO-218 AA	C67078-S3115-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, T_C = 28 °C	I_D	**45**	A
Pulsed drain current, T_C = 25°C	$I_{D\,puls}$	**180**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**45**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**2.5**	mJ
Avalanche energy, single pulse I_D = 42 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 20.2 µH, T_j = 25 °C	E_{AS}	**41**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, T_C = 25 °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	50	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 50 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 29 A	$R_{DS(on)}$	–	0.025	0.030	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 29 A	g_{fs}	7.0	22.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1800	2400	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	800	1200	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	280	450	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	35	50	ns
	t_r	–	85	130	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	220	280	
	t_f	–	140	180	

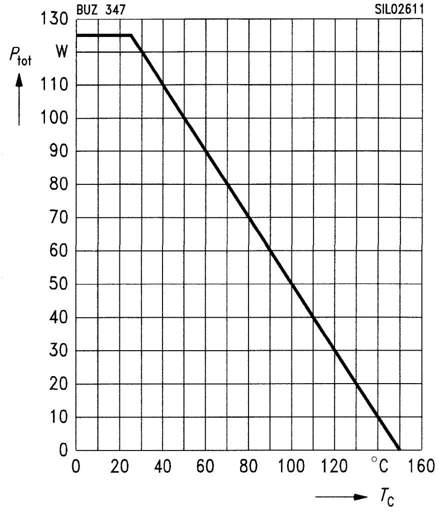
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	45	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	180	
Diode forward on-voltage I_S = 90 A, V_{GS} = 0 V	V_{SD}	–	1.8	2.2	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	80	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.14	–	µC

Characteristics at T_j = 25 ˚C, unless otherwise specified.

Total power dissipation

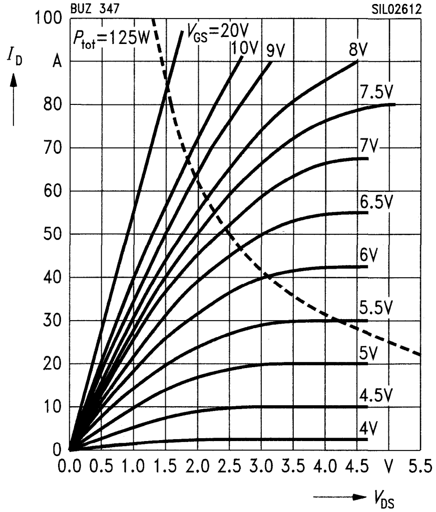
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

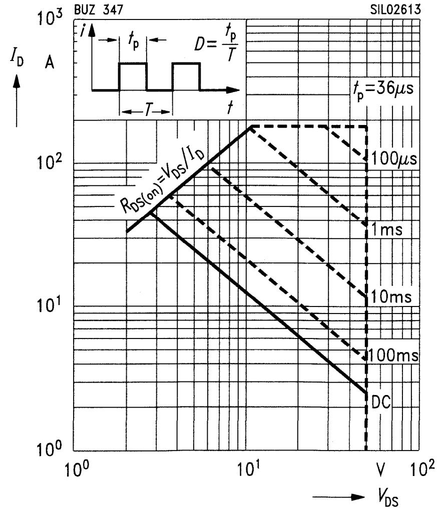
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

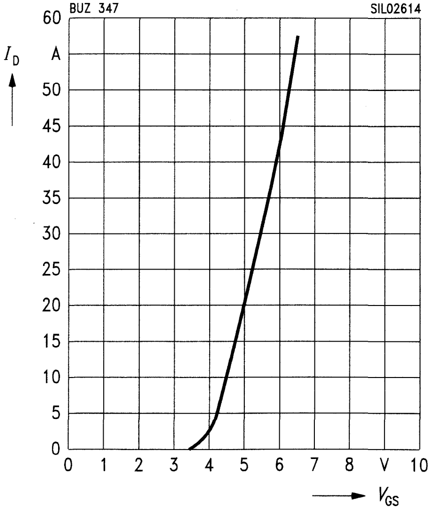
parameter: D = 0.01, T_C = 25 ˚C



Typ. transfer characteristics

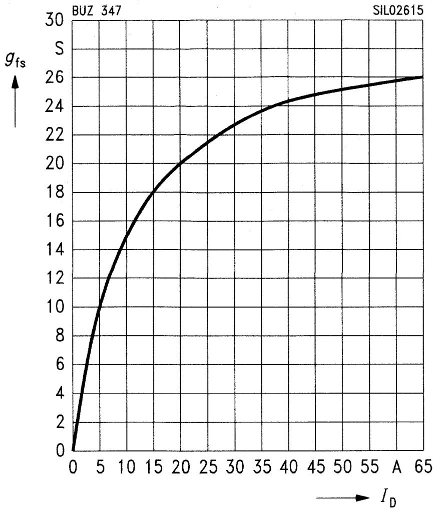
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



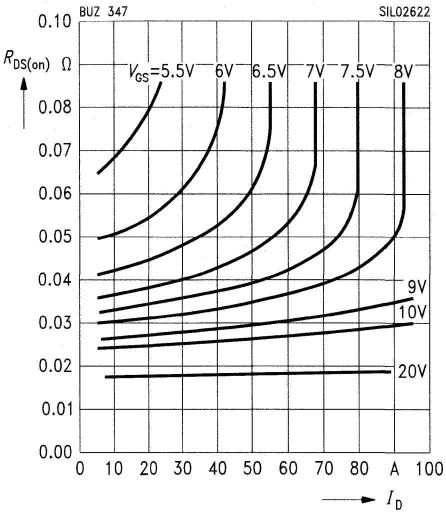
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: t_p = 80 µs



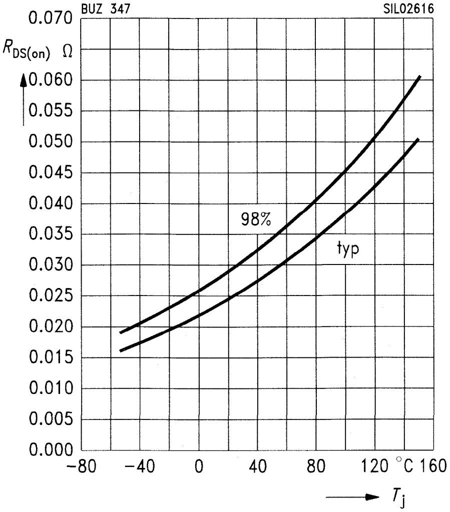
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$
parameter: V_{GS}



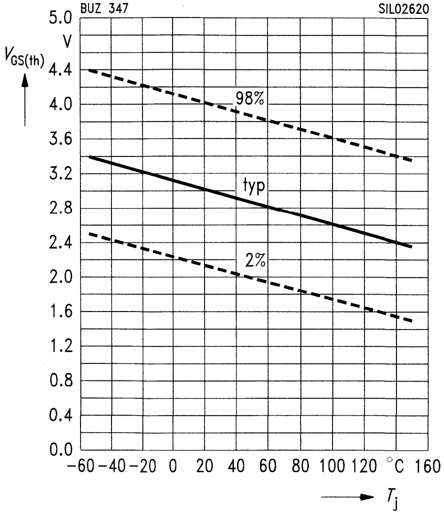
Drain-source on-resistance

$R_{DS(on)} = f(T_j)$
parameter: I_D = 28 A, V_{GS} = 10 V, (spread)



Gate threshold voltage

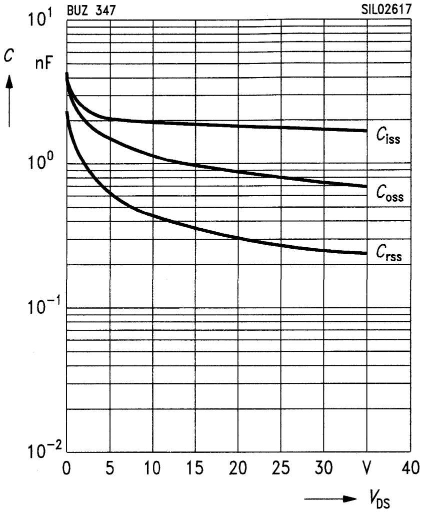
$V_{GS(th)} = f(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

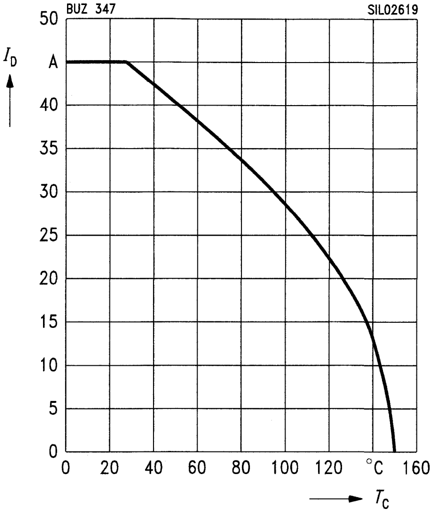
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

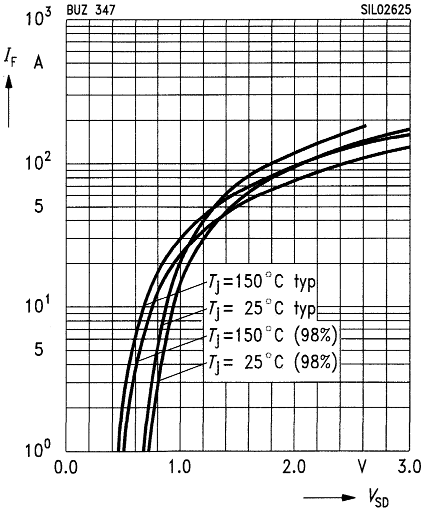
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

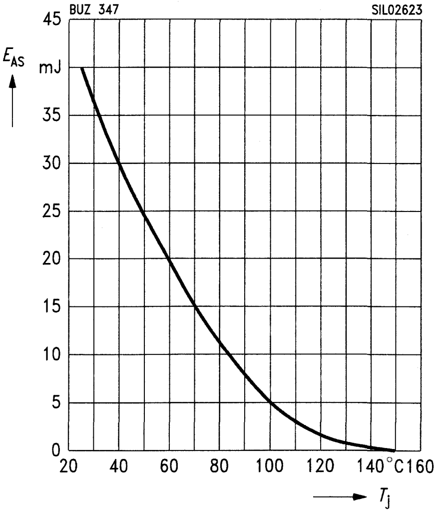
parameter: T_j , $t_p = 80$ µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

parameter: $I_D = 45$ A, $V_{DD} = 25$ V

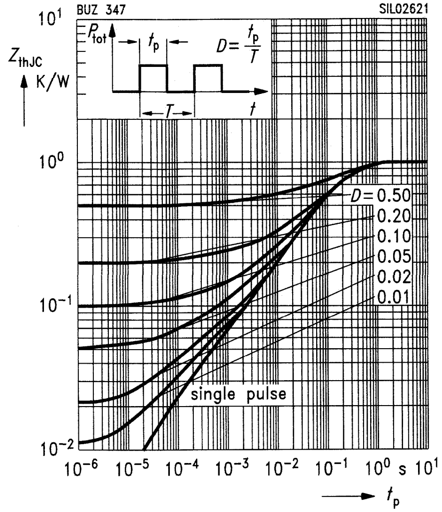
$R_{GS} = 25\ \Omega$, $L = 20.2$ µH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

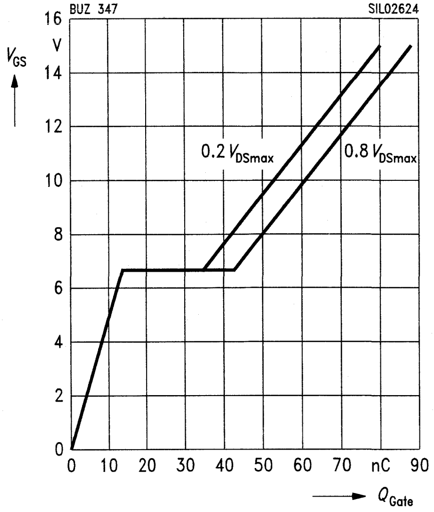
parameter: $D = t_p / T$



Typ. gate charge

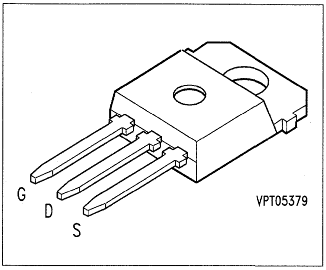
$V_{GS} = f(Q_{\text{Gate}})$

parameter: $I_{\text{D puls}} = 63.0$ A



SIPMOS® Power Transistor **BUZ 349**

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 349	100 V	32 A	0.06 Ω	TO-218 AA	C67078-S3113-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, $T_C = 27$ °C	I_D	**32**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\ puls}$	**128**	
Avalanche current, limited by $T_{j\ max}$	I_{AR}	**32**	
Avalanche energy, periodic limited by $T_{j\ (max)}$	E_{AR}	**15**	mJ
Avalanche energy, single pulse $I_D = 32$ A, $V_{DD} = 25$ V, $R_{GS} = 25\ \Omega$ $L = 322\ \mu$H, $T_j = 25$ °C	E_{AS}	**220**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, $T_C = 25$ °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\ JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	100	–	–	V
Gate threshold voltage V_{GS} = V_{DS}, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 100 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 21 A	$R_{DS\,(on)}$	–	0.05	0.06	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 21 A	g_{fs}	10	17	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1400	1850	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	450	700	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	230	370	
Turn-on time t_{on}, ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	30	45	ns
	t_r	–	80	125	
Turn-off time t_{off}, ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	250	320	
	t_f	–	120	160	

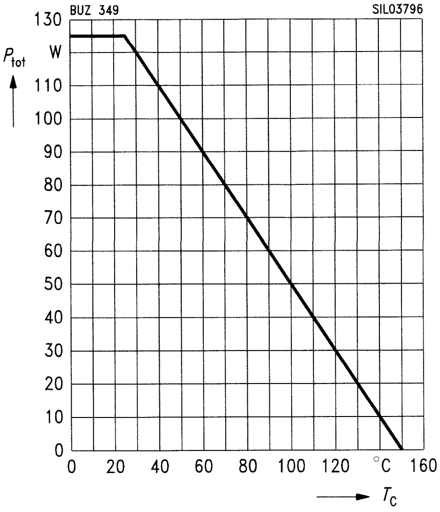
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	32	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	128	
Diode forward on-voltage I_S = 64 A, V_{GS} = 0 V	V_{SD}	–	1.4	1.7	V
Reverse recovery time V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	130	–	ns
Reverse recovery charge V_R = 30 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.7	–	µC

Characteristics at T_j = 25 ˚C, unless otherwise specified.

Total power dissipation

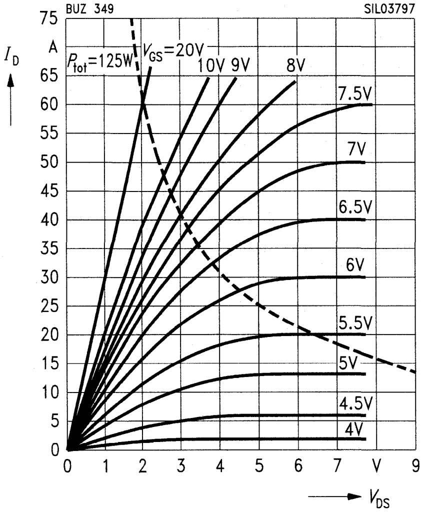
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

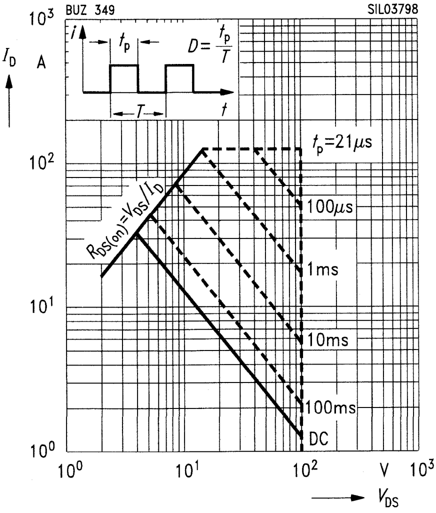
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

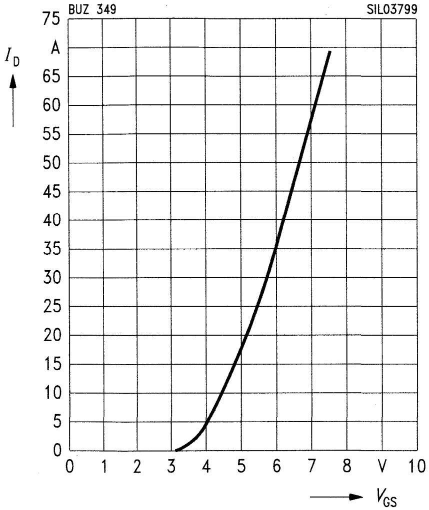
parameter: D = 0.01, T_C = 25 ˚C



Typ. transfer characteristics

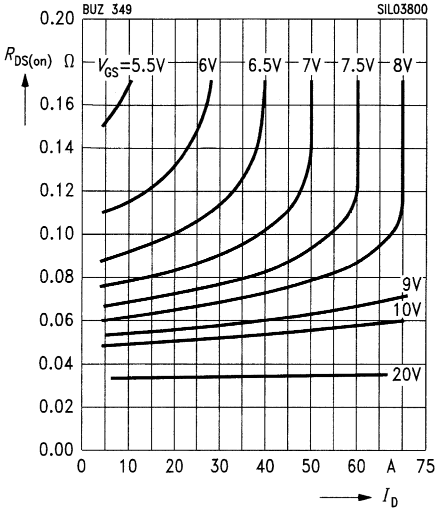
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



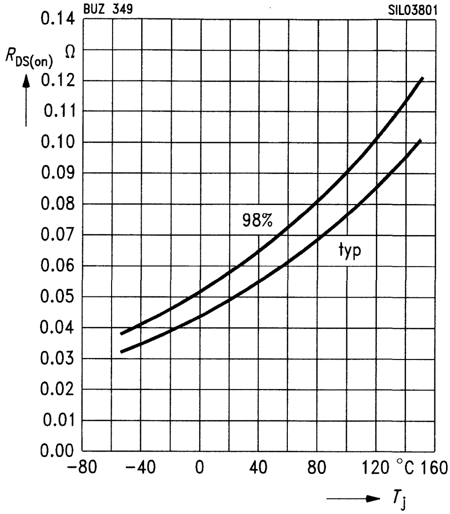
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



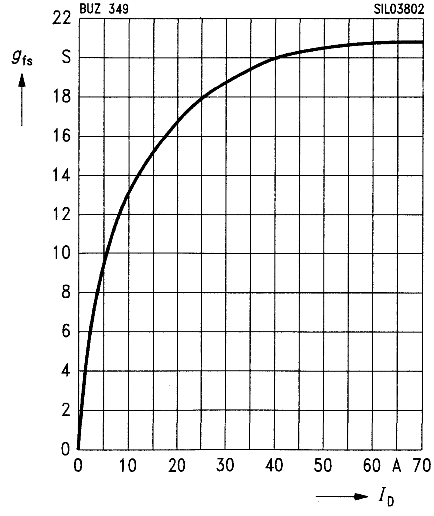
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 20 A, V_{GS} = 10 V, (spread)



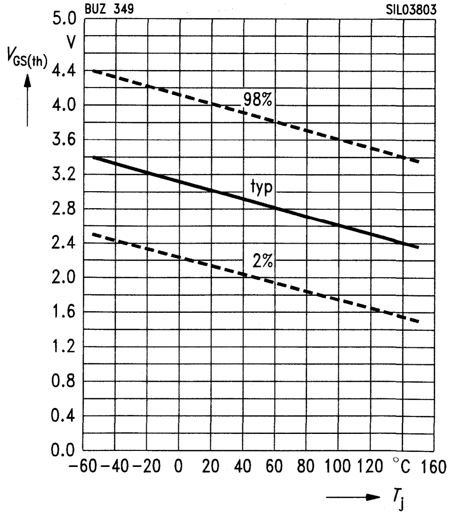
Typ. forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

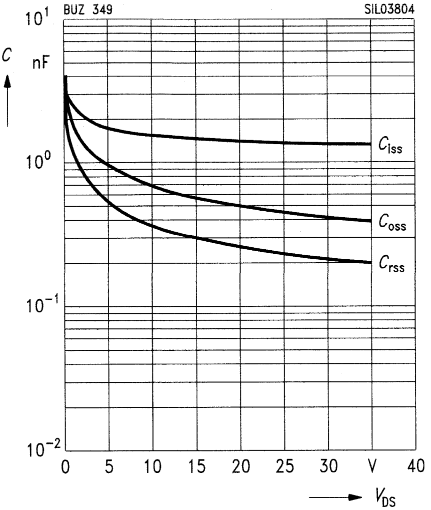
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

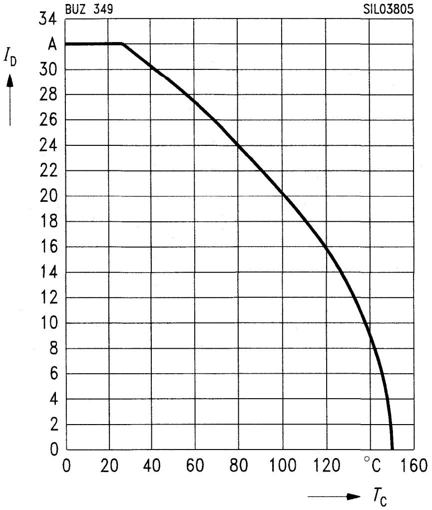
parameter: V_{GS} = 0 V, f = 1 MHz



Drain current

$I_D = f(T_C)$

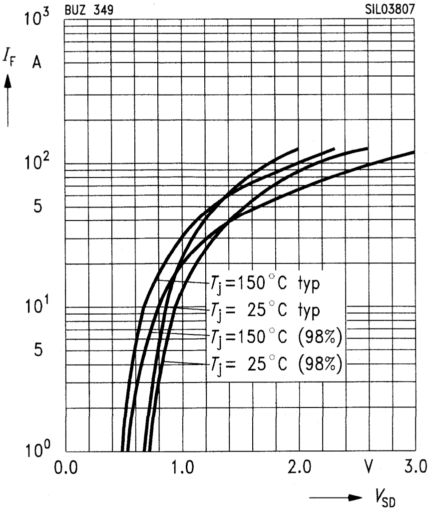
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

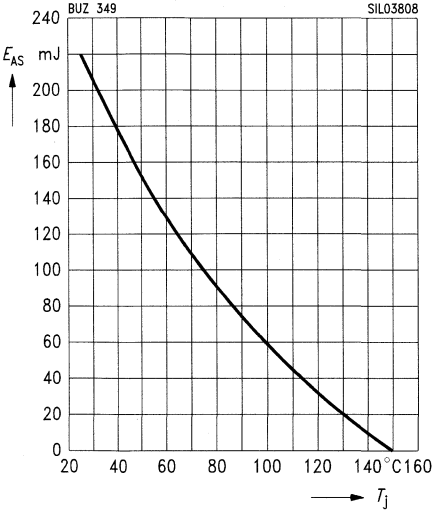
parameter: T_j, t_p = 80 µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

parameter: I_D = 32 A, V_{DD} = 25 V

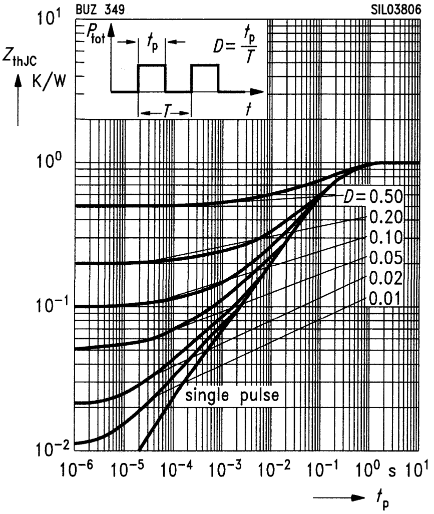
R_{GS} = 25 Ω, L = 322 µH



Transient thermal impedance

$Z_{thJC} = f(t_p)$

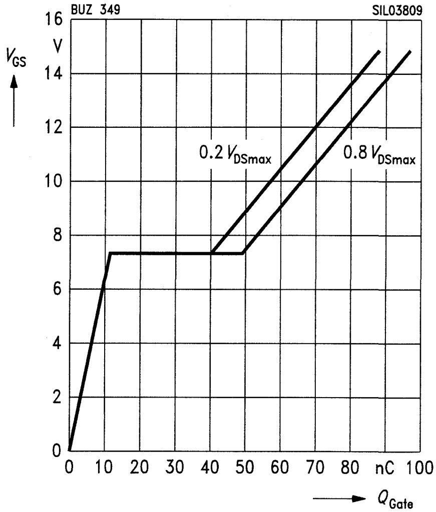
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{Gate})$

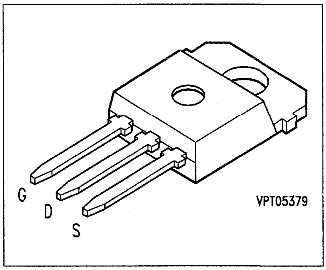
parameter: $I_{D\,puls} = 51.0$ A



SIPMOS® Power Transistor

BUZ 350

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 350	200 V	22 A	0.12 Ω	TO-218 AA	C67078-S3117-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, $T_C = 33$ °C	I_D	**22**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**88**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**22.0**	
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**13**	mJ
Avalanche energy, single pulse $I_D = 22$ A, $V_{DD} = 50$ V, $R_{GS} = 25$ Ω $L = 1.77$ mH, $T_j = 25$ °C	E_{AS}	**570**	
Gate-source voltage	V_{GS}	**± 20**	V
Power dissipation, $T_C = 25$ °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	200	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 200 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	10	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 14 A	$R_{DS\,(on)}$	–	0.09	0.12	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 14 A	g_{fs}	9.0	15	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1400	1900	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	280	400	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	130	200	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	30	45	ns
	t_r	–	70	110	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	250	320	
	t_f	–	90	120	

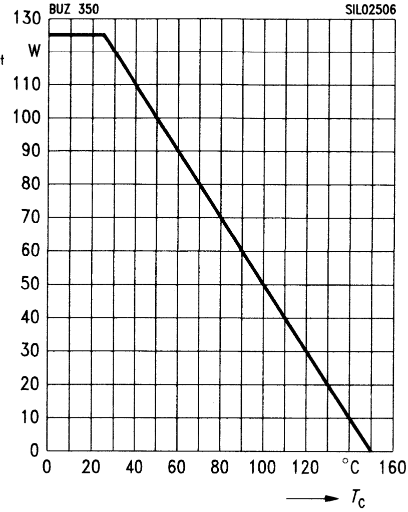
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 °C	I_S	–	–	22	A
Pulsed reverse drain current T_C = 25 °C	I_{SM}	–	–	88	
Diode forward on-voltage I_S = 44 A, V_{GS} = 0 V	V_{SD}	–	1.2	1.7	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	180	–	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	1.2	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

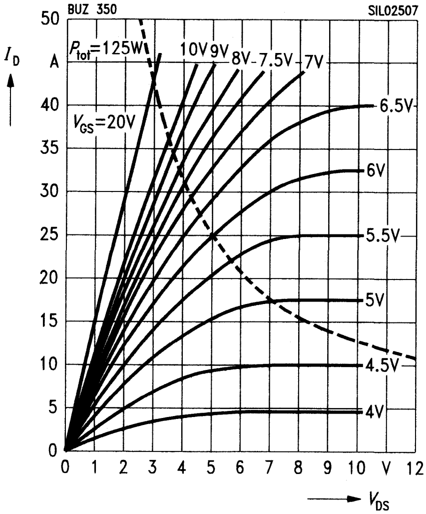
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

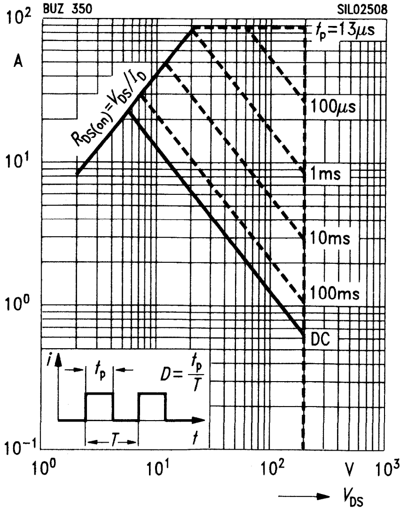
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

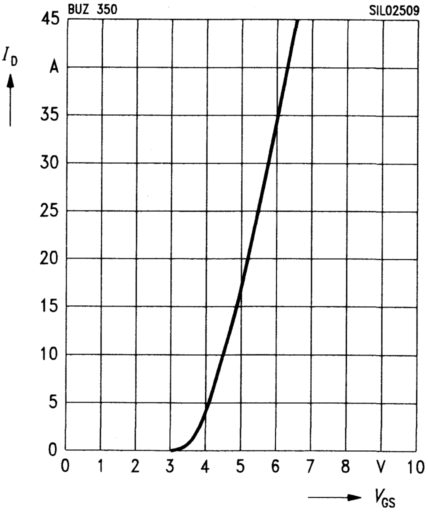
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

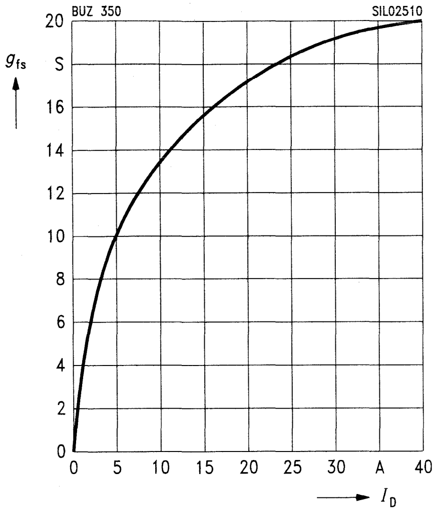
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



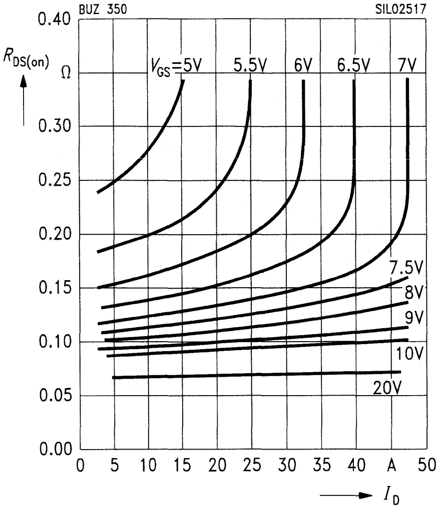
Typ. forward transconductance

$g_{fs} = f(I_D)$
parameter: t_p = 80 µs



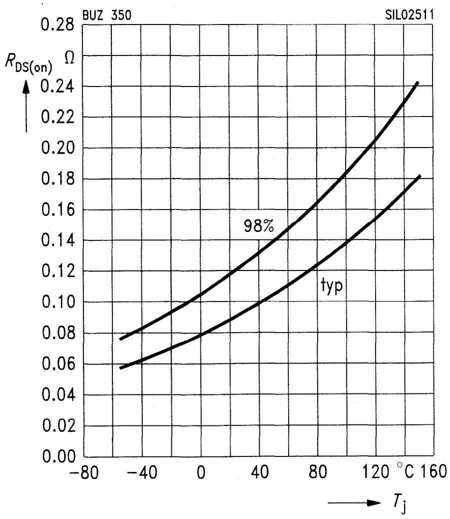
Typ. drain-source on-resistance

$R_{DS(on)} = f(I_D)$
parameter: V_{GS}



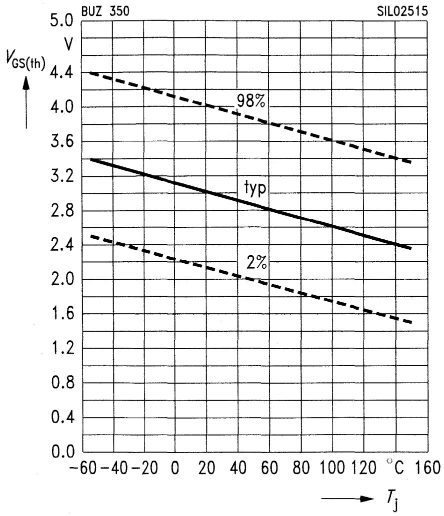
Drain-source on-resistance

$R_{DS(on)} = f(T_j)$
parameter: I_D = 14 A, V_{GS} = 10 V, (spread)



Gate threshold voltage

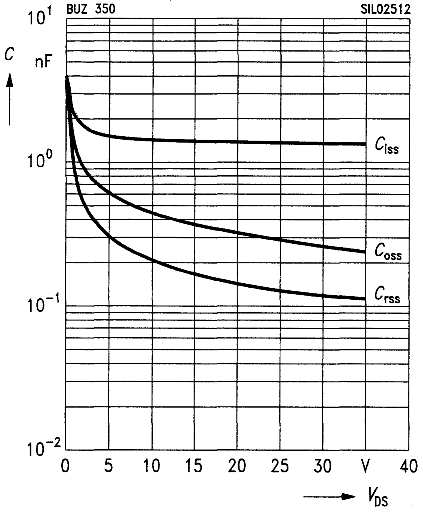
$V_{GS(th)} = f(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

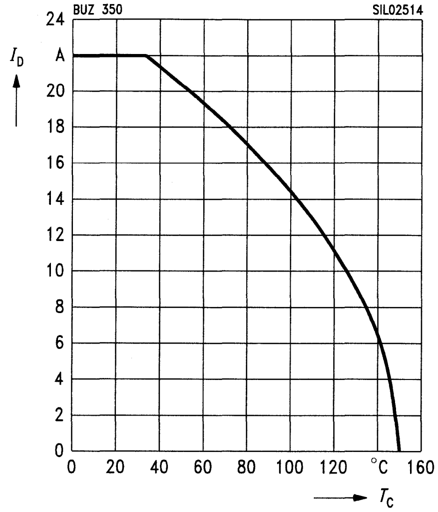
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



Drain current

$I_D = f(T_C)$

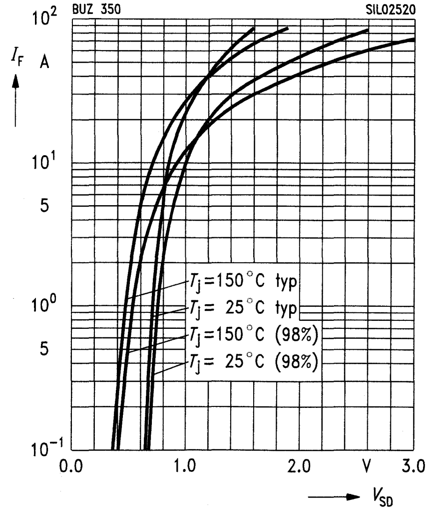
parameter: $V_{GS} \geq 10$ V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

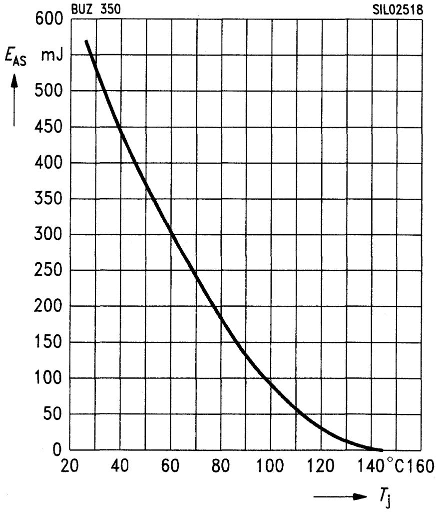
parameter: T_j, $t_p = 80$ µs, (spread)



Avalanche energy $E_{AS} = f(T_j)$

parameter: $I_D = 22$ A, $V_{DD} = 50$ V

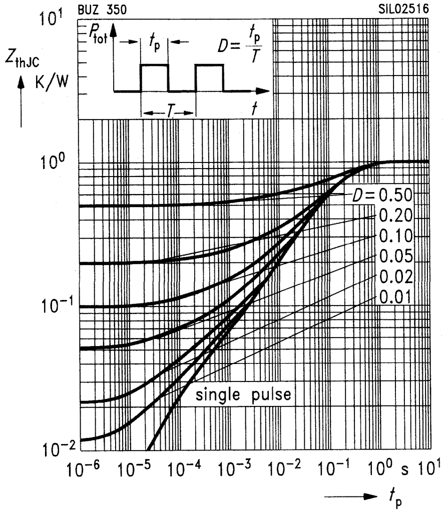
$R_{GS} = 25\ \Omega$, $L = 1.77$ mH



Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$

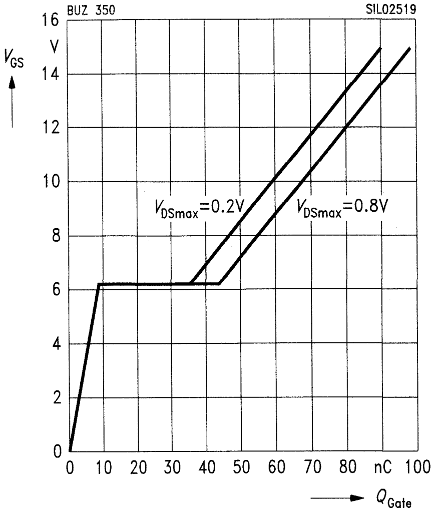
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{\text{Gate}})$

parameter: $I_{\text{D puls}} = 33.0$ A

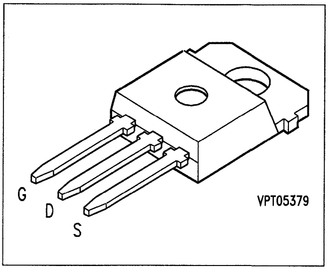


SIEMENS

SIPMOS® Power Transistors

BUZ 355
BUZ 356

- N channel
- Enhancement mode



Type	V_{DS}	I_D	T_C	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 355	800 V	6.0 A	29 °C	1.5 Ω	TO-218 AA	C67078-A3107-A2
BUZ 356	800 V	5.3 A	25 °C	2.0 Ω	TO-218 AA	C67078-A3108-A2

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		355	356	
Continuous drain current	I_D	**6.0**	**5.3**	A
Pulsed drain current, T_C = 25 °C	$I_{D\,puls}$	**21**		
Drain source voltage	V_{DS}	**800**		V
Drain-gate voltage, R_{GS} = 20 kΩ	V_{DGR}	**800**		
Gate-source voltage	V_{GS}	**± 20**		
Power dissipation, T_C = 25 °C	P_{tot}	**125**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**C**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	800	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 800 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	20	250	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS\,(on)}$				Ω
V_{GS} = 10 V, I_D = 3.0 A BUZ 355		–	1.3	1.5	
BUZ 356		–	1.6	2.0	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 3.0 A	g_{fs}	1.8	3.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	3.9	5.0	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	200	350	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	80	140	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	60	90	ns
	t_r	–	90	140	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	330	430	
	t_f	–	110	140	

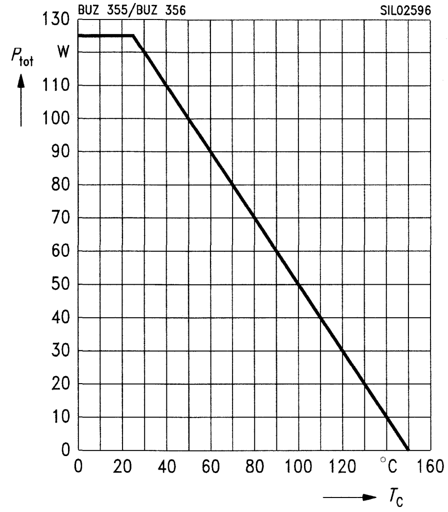
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter		**Symbol**	**Values**			**Unit**
			min.	**typ.**	**max.**	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 ˚C	BUZ 355		–	–	6.0	
	BUZ 356		–	–	5.3	
Pulsed reverse drain current		I_{SM}				
T_C = 25 ˚C	BUZ 355		–	–	24	
	BUZ 356		–	–	21	
Diode forward on-voltage I_S = 12 A, V_{GS} = 0 V		V_{SD}	–	1.1	1.5	V
Reverse recovery time V_R = 100 V, I_F = I_S, di_F / dt = 100 A/µs		t_{rr}	–	1.8	–	µs
Reverse recovery charge V_R = 100 V, I_F = I_S, di_F / dt = 100 A/µs		Q_{rr}	–	25	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

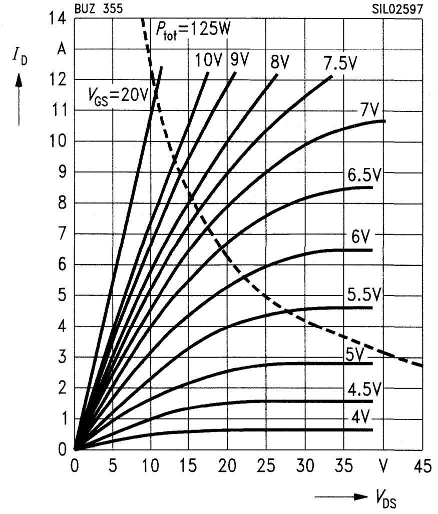
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 355**

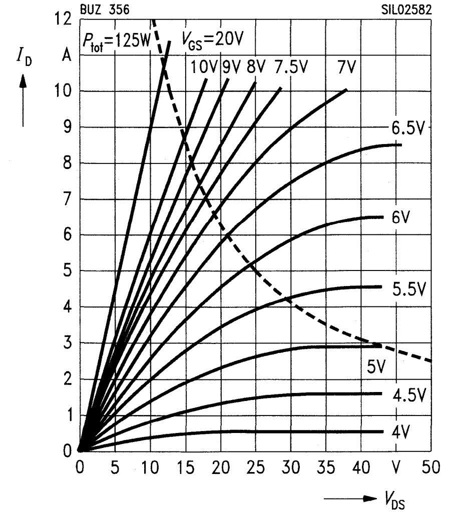
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 356**

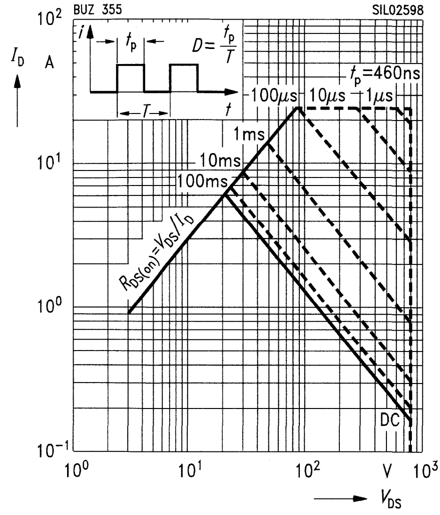
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$ **BUZ 355**

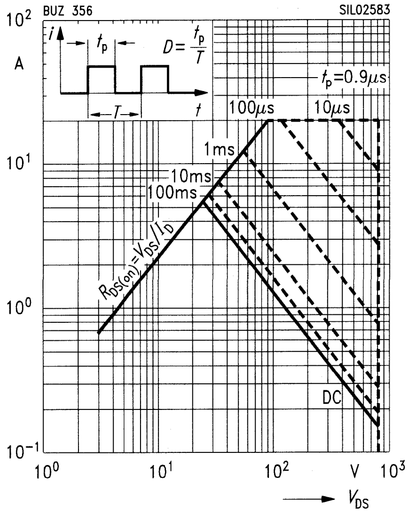
parameter: D = 0.01, T_C = 25 °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 356**

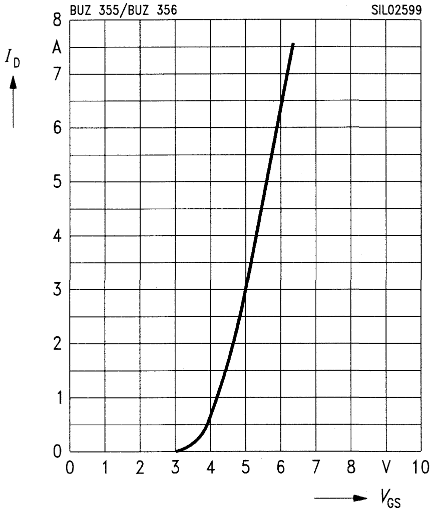
parameter: $D = 0.01$, $T_C = 25\ ^\circ C$



Typ. transfer characteristics

$I_D = f(V_{GS})$

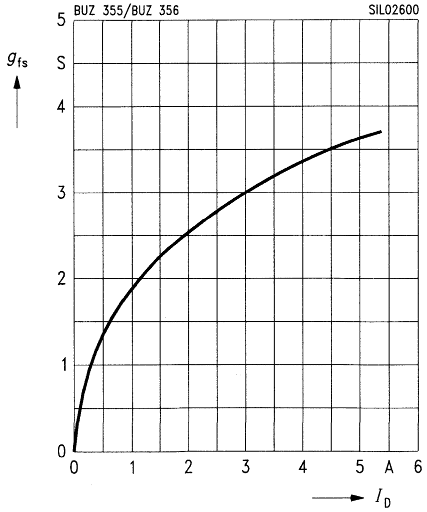
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. forward transconductance

$g_{fs} = f(I_D)$

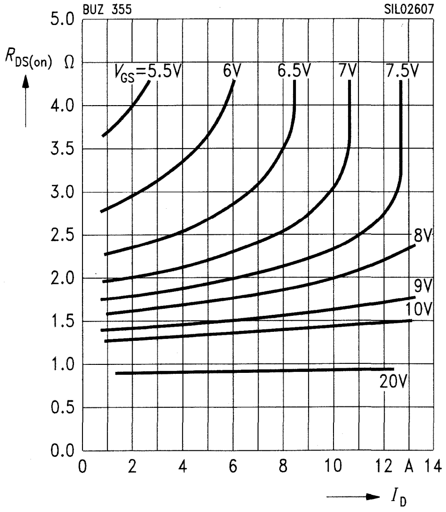
parameter: t_p = 80 µs



Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$ **BUZ 355**

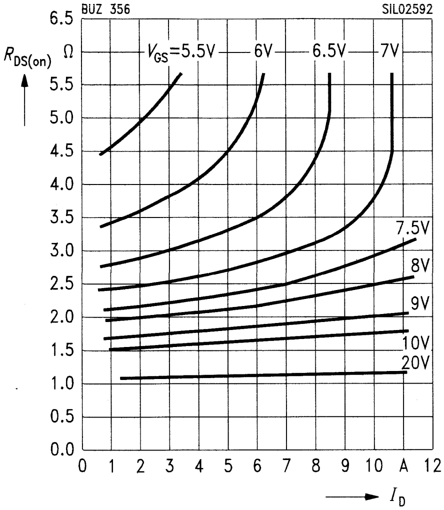
parameter: V_{GS}



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 356**

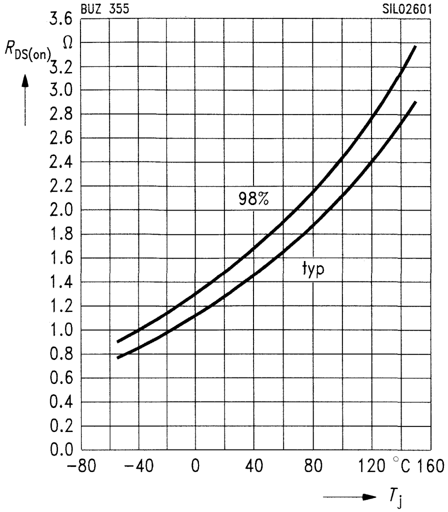
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 355**

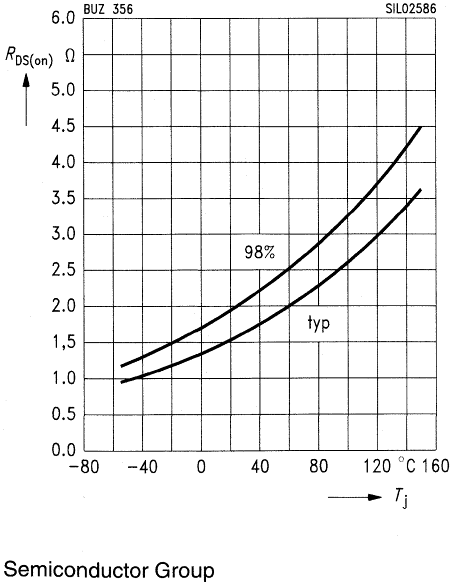
parameter: I_D = 3.8 A, V_{GS} = 10 V, (spread)



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 356**

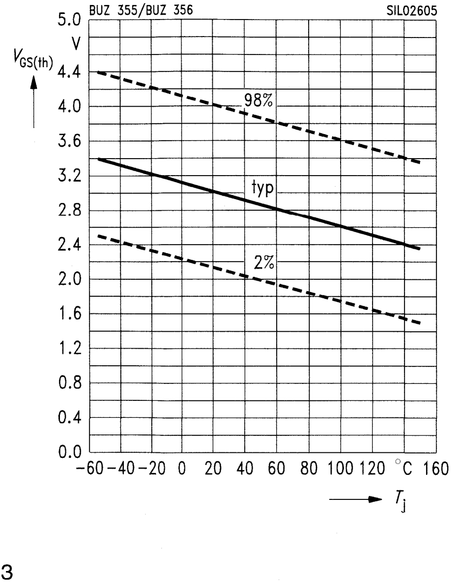
parameter: I_D = 3.8 A, V_{GS} = 10 V, (spread)



Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

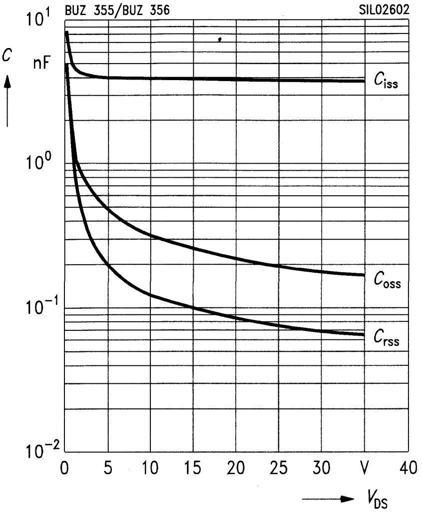
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

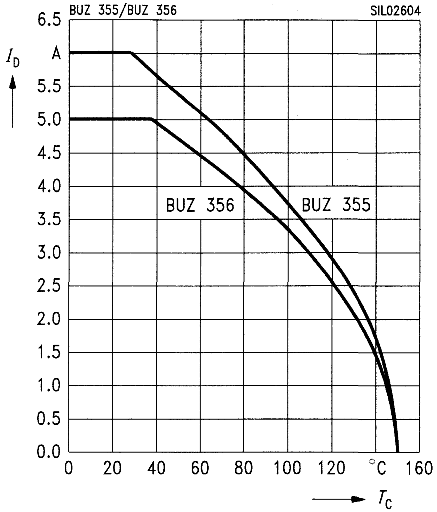
parameter: V_{GS} = 0 V, f = 1 MHz



Drain current

$I_D = f(T_C)$

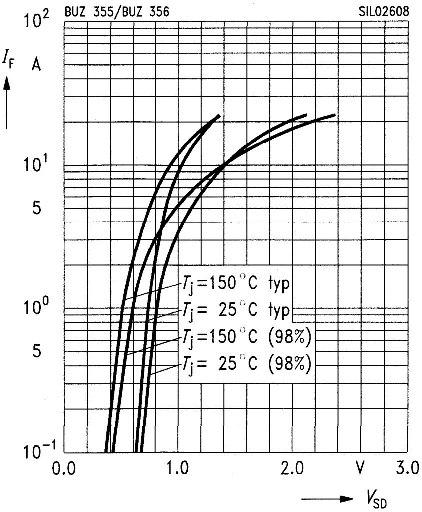
parameter: $V_{GS} \geq$ 10 V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

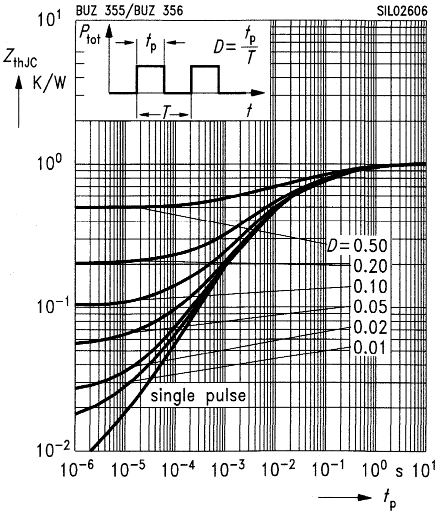
parameter: T_j , t_p = 80 µs, (spread)



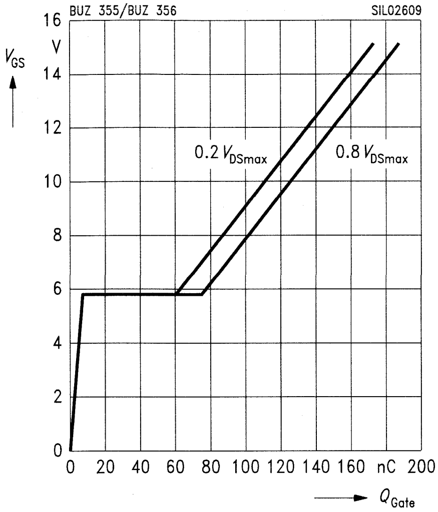
Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

parameter: $D = t_p / T$



Typ. gate charge
$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 9$ A

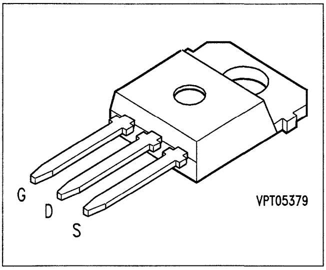


SIEMENS

SIPMOS® Power Transistors

BUZ 357
BUZ 358

- N channel
- Enhancement mode
- Avalanche-rated



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1]	Ordering Code
BUZ 357	1000 V	5.1 A	2.0 Ω	TO-218 AA	C67078-S3110-A2
BUZ 358	1000 V	4.5 A	2.6 Ω	TO-218 AA	C67078-S3111-A2

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		357	358	
Continuous drain current, T_C = 25 ˚C	I_D	**5.1**	**4.5**	A
Pulsed drain current, T_C = 25 ˚C	$I_{D\,puls}$	**20**	**18**	
Avalanche current, limited by $T_{j\,max}$	I_{AR}	**5.1**		
Avalanche energy, periodic limited by $T_{j\,(max)}$	E_{AR}	**18**		mJ
Avalanche energy, single pulse I_D = 5.1 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 62 mH, T_j = 25 ˚C	E_{AS}	**850**		
Gate-source voltage	V_{GS}	**± 20**		V
Power dissipation, T_C = 25 ˚C	P_{tot}	**125**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		˚C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

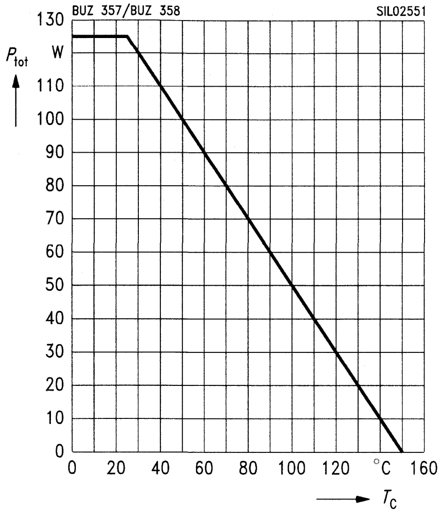
Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	1000	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 1000 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	0.1	1.0	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance	$R_{DS(on)}$				Ω
V_{GS} = 10 V, I_D = 3.2 A BUZ 357		–	1.7	2.0	
BUZ 358		–	2.3	2.6	
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 3.2 A	g_{fs}	2.5	5.2	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1700	2200	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	170	300	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	80	40	
Turn-on time t_{on} , ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	30	45	ns
	t_r	–	100	160	
Turn-off time t_{off} , ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	400	520	
	t_f	–	130	170	

Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

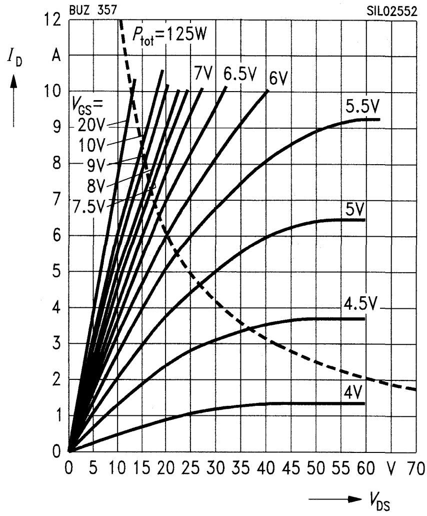
Parameter		Symbol	Values			Unit
			min.	typ.	max.	
Reverse diode						
Continuous reverse drain current		I_S				A
T_C = 25 °C	BUZ 357		–	–	5.1	
	BUZ 358		–	–	4.5	
Pulsed reverse drain current		I_{SM}				
T_C = 25 °C	BUZ 357		–	–	20	
	BUZ 358		–	–	18	
Diode forward on-voltage I_S =10 A, V_{GS} = 0 V		V_{SD}	–	1.0	1.2	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		t_{rr}	–	1.5	–	µs
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		Q_{rr}	–	6.5	–	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

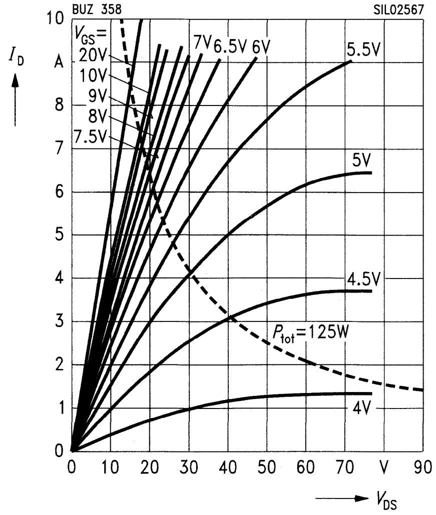
Total power dissipation
$P_{tot} = f(T_C)$



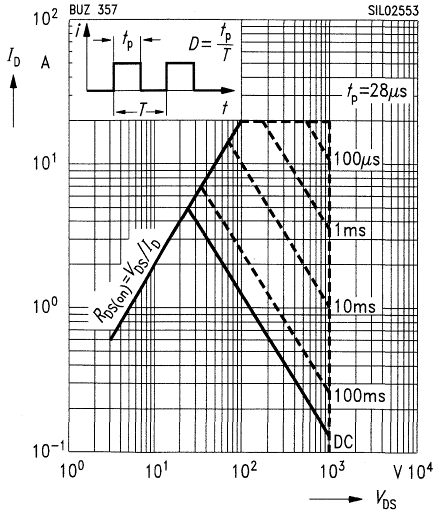
Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 357**
parameter: t_p = 80 µs



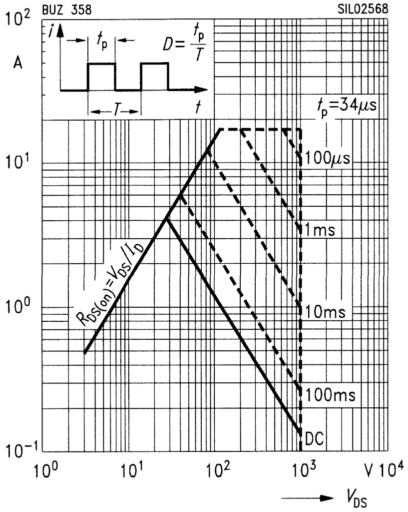
Typ. output characteristics
$I_D = f(V_{DS})$ **BUZ 358**
parameter: t_p = 80 µs



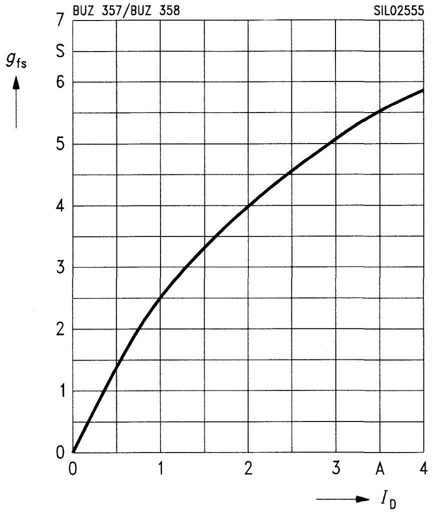
Safe operating area
$I_D = f(V_{DS})$ **BUZ 357**
parameter: D = 0.01, T_C = 25 °C



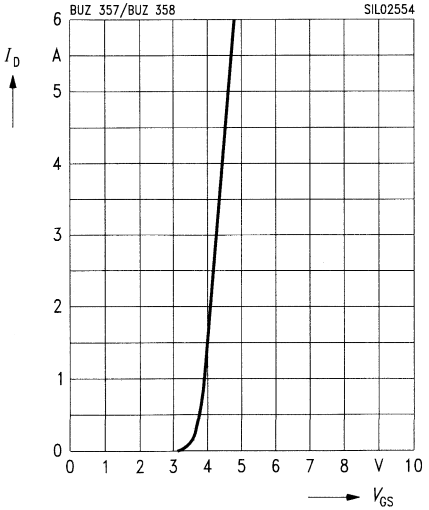
Safe operating area
$I_D = f(V_{DS})$ **BUZ 358**
parameter: $D = 0.01$, $T_C = 25$ °C



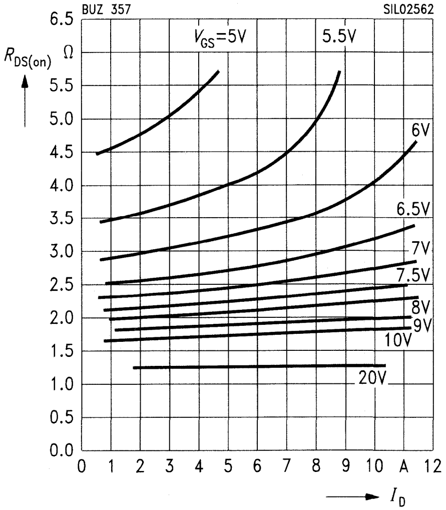
Typ. forward transconductance
$g_{fs} = f(I_D)$
parameter: $t_p = 80$ µs



Typ. transfer characteristics
$I_D = f(V_{GS})$
parameter: $t_p = 80$ µs, $V_{DS} = 25$ V

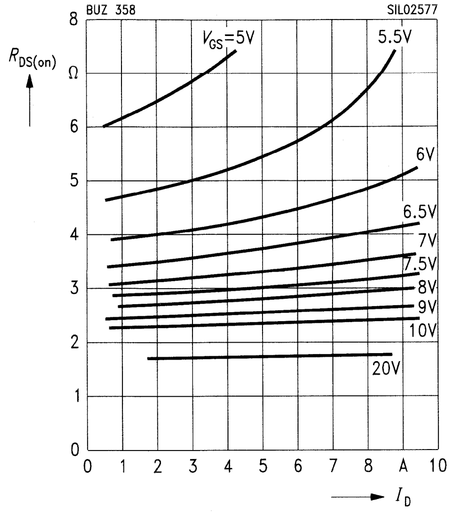


Typ. drain-source on-resistance
$R_{DS(on)} = f(I_D)$ **BUZ 357**
parameter: V_{GS}



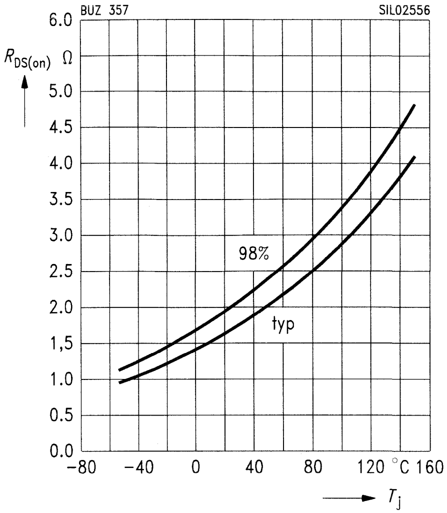
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 358**
parameter: V_{GS}



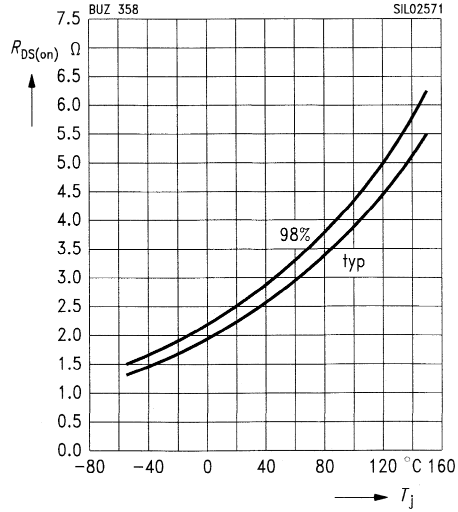
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 357**
parameter: I_D = 3.2 A, V_{GS} = 10 V, (spread)



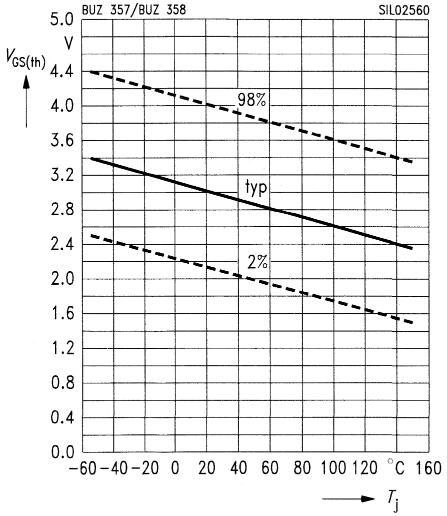
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 358**
parameter: I_D = 3.2 A, V_{GS} = 10 V, (spread)



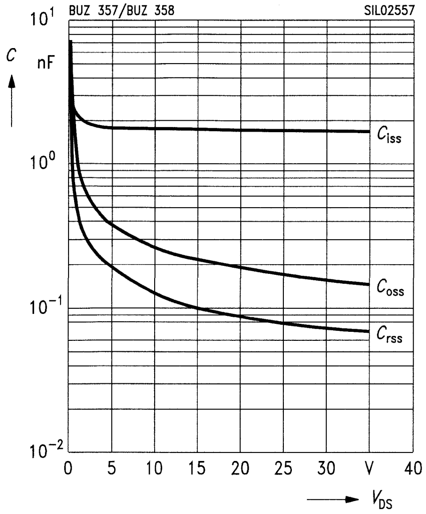
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



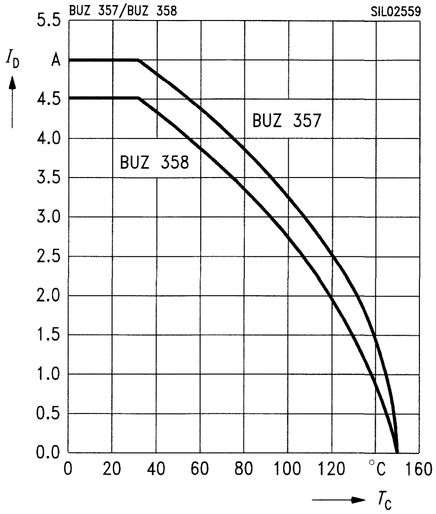
Typ. capacitances

$C = f(V_{DS})$
parameter: V_{GS} = 0 V, f = 1 MHz



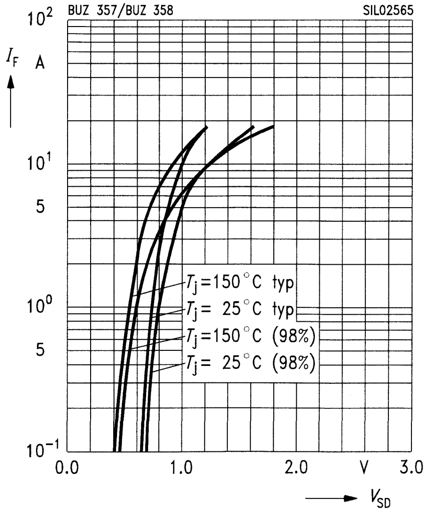
Drain current

$I_D = f(T_C)$
parameter: V_{GS} ≥ 10 V



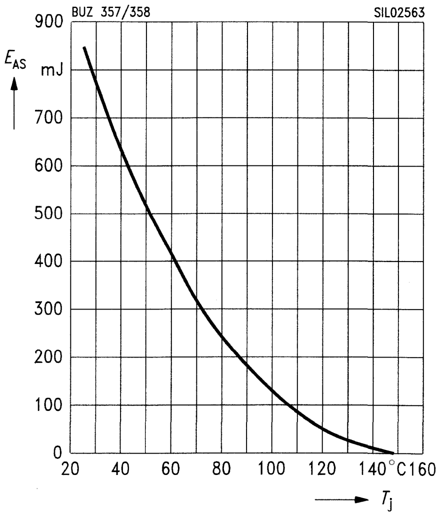
Forward characteristics of reverse diode

$I_F = f(V_{SD})$
parameter: T_j, t_p = 80 µs, (spread)



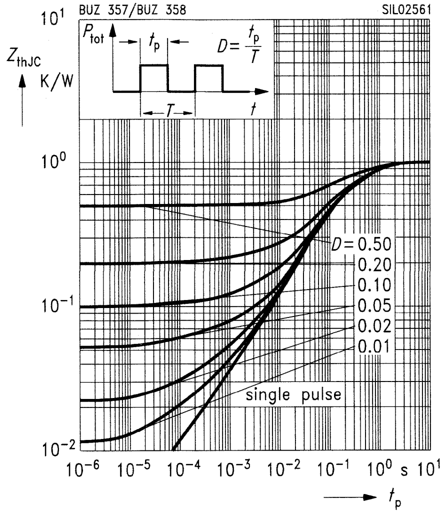
Avalanche energy $E_{AS} = f(T_j)$

parameter: I_D = 5 A, V_{DD} = 50 V
R_{GS} = 25 Ω, L = 64.6 mH



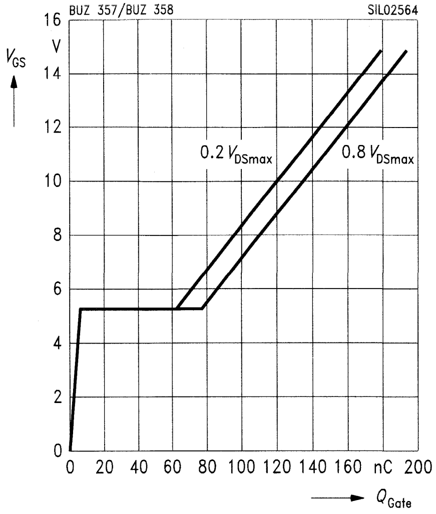
Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$



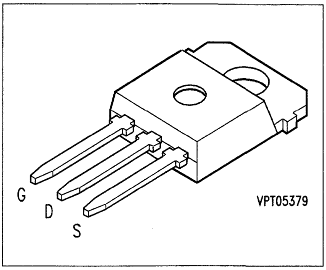
Typ. gate charge

$V_{\text{GS}} = f(Q_{\text{Gate}})$
parameter: $I_{\text{D puls}} = 7.5$ A



SIPMOS® Power Transistor **BUZ 380**

- N channel
- Enhancement mode
- FREDFET



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 380	1000 V	5.5 A	2.0 Ω	TO-218 AA	C67078-A3205-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, $T_C = 30$ °C	I_D	**5.5**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**22**	
Drain-source voltage	V_{DS}	**1000**	V
Drain-gate voltage, $R_{GS} = 20$ kΩ	V_{DGR}	**1000**	
Gate-source voltage	V_{GS}	**± 20**	
Power dissipation, $T_C = 25$ °C	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	1000	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.5	4.0	
Zero gate voltage drain current V_{DS} = 1000 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	20	250	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 3.5 A	$R_{DS\,(on)}$	–	1.7	2.0	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 3.5 A	g_{fs}	1.4	4.0	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	3.9	5.0	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	180	300	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	70	120	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = – 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	60	90	ns
	t_r	–	90	140	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = – 30 V, V_{GS} = 10 V, I_D = 2.5 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	330	430	
	t_f	–	110	140	

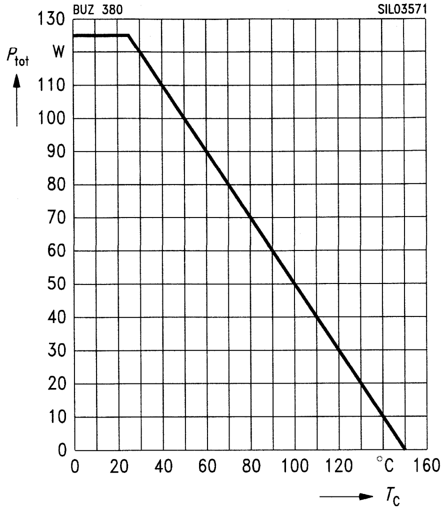
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	5.5	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	22	
Diode forward on-voltage I_S = 1 A, V_{GS} = 0 V	V_{SD}	–	1.25	1.6	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	150	220	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.6	0.9	µC

Characteristics at T_j = 25 ˚C, unless otherwise specified.

Total power dissipation

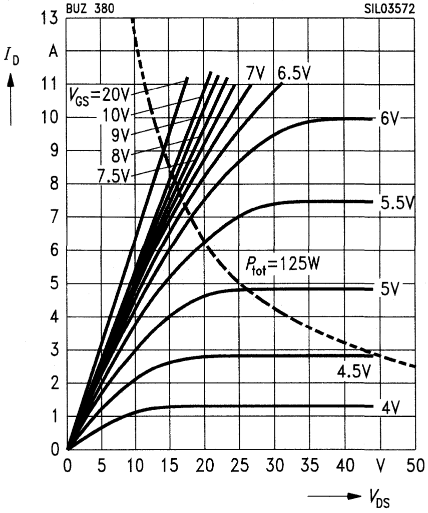
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

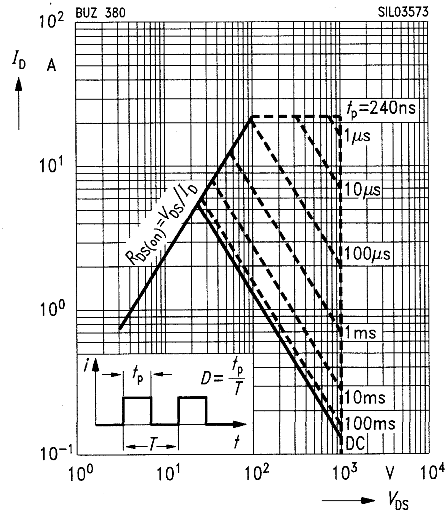
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

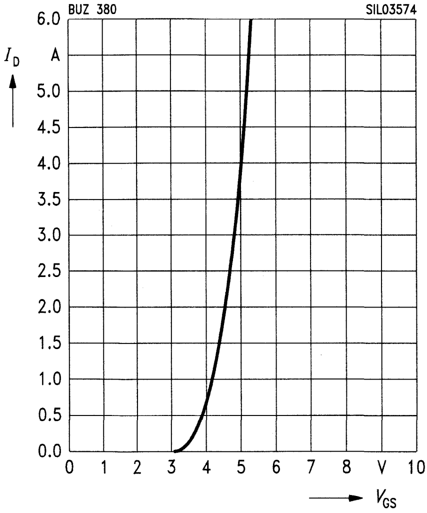
parameter: D = 0.01, T_C = 25 ˚C



Typ. transfer characteristics

$I_D = f(V_{GS})$

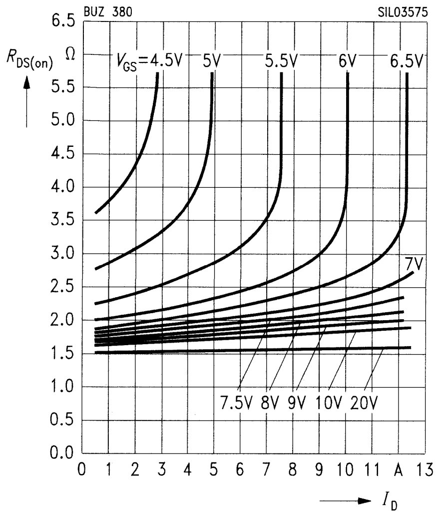
parameter: t_p = 80 µs, V_{DS} = 25 V



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$

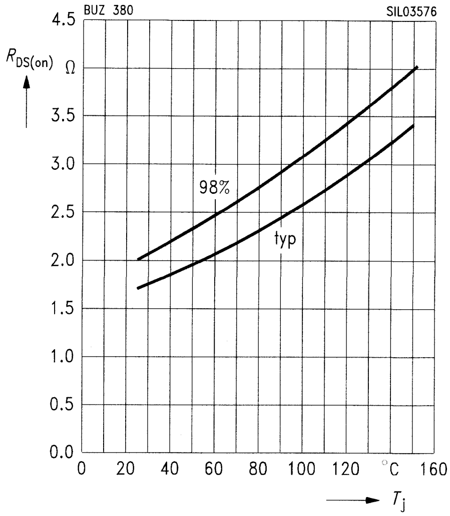
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$

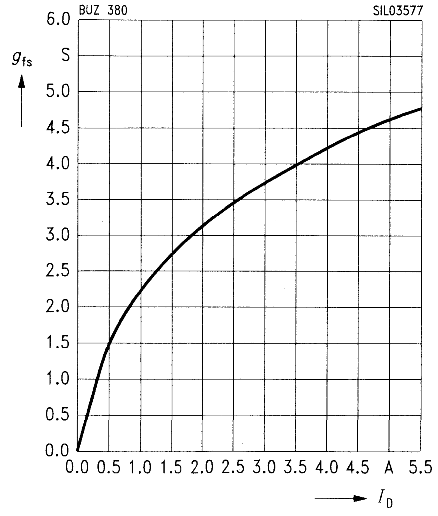
parameter: I_D = 3.5 A, V_{GS} = 10 V, (spread)



Typ. forward transconductance

$g_{fs} = f\,(I_D)$

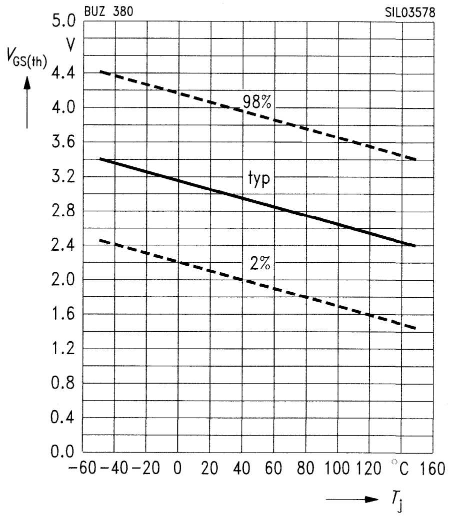
parameter: t_p = 80 µs



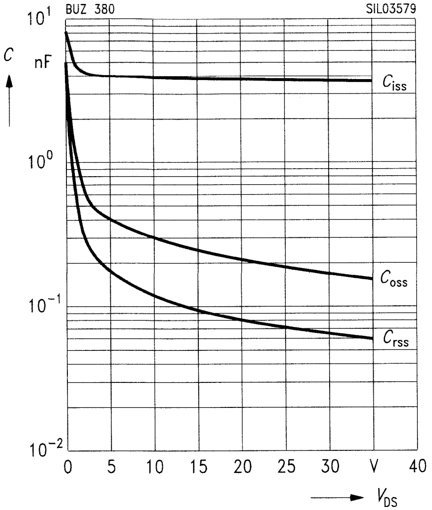
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

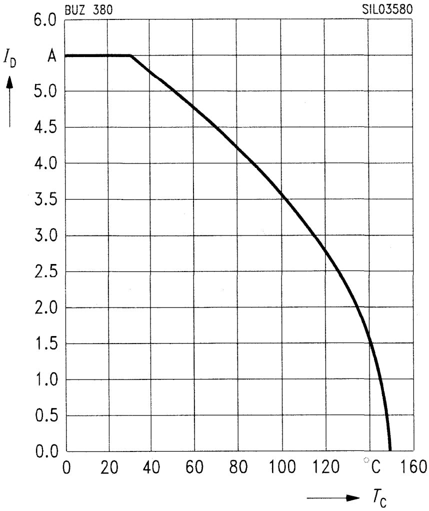
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



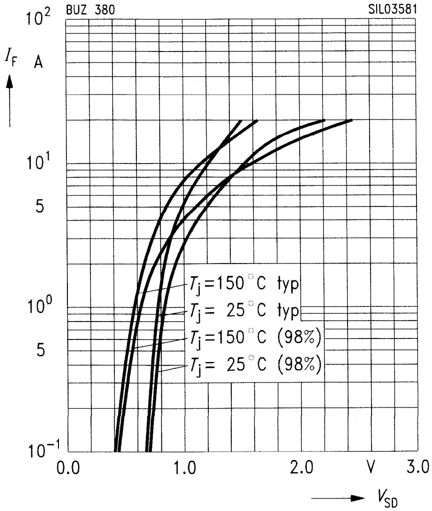
Typ. capacitances
$C = f(V_{DS})$
parameter: $V_{GS} = 0$ V, $f = 1$ MHz



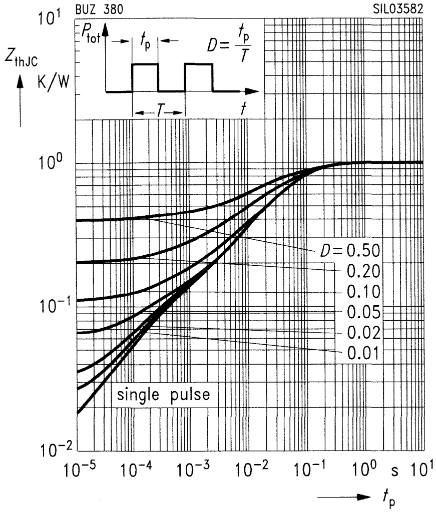
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq 10$ V



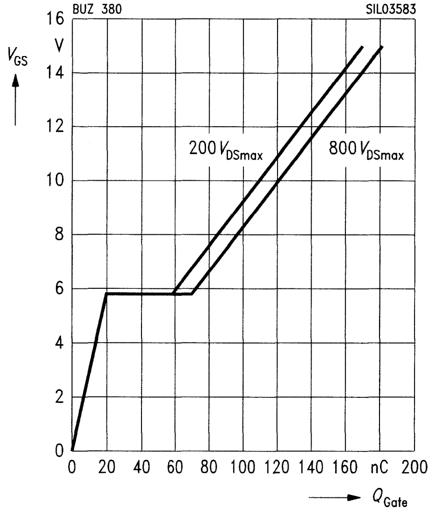
Forward characteristics of reverse diode
$I_F = f(V_{SD})$
parameter: $t_p = 80$ µs, T_j



Transient thermal impedance
$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



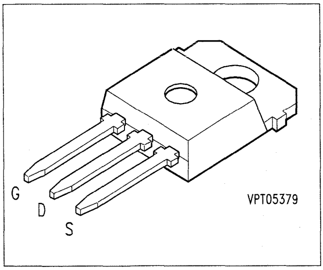
Typ. gate charge
$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 8$ A



SIPMOS® Power Transistor

BUZ 382

- N channel
- Enhancement mode
- FREDFET



Type	V_{DS}	I_D	$R_{DS(on)}$	Package [1]	Ordering Code
BUZ 382	400 V	12.5 A	0.4 Ω	TO-218 AA	C67078-A3207-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current, $T_C = 30\ ^\circ C$	I_D	**12.5**	A
Pulsed drain current, $T_C = 25\ ^\circ C$	$I_{D\ puls}$	**50**	
Drain-source voltage	V_{DS}	**400**	V
Drain-gate voltage, $R_{GS} = 20\ k\Omega$	V_{DGR}	**400**	
Gate-source voltage	V_{GS}	**± 20**	
Power dissipation, $T_C = 25\ ^\circ C$	P_{tot}	**125**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	˚C

Thermal resistance, chip-case	$R_{th\ JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

Static characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)\,DSS}$	400	–	–	V
Gate threshold voltage $V_{GS} = V_{DS}$, I_D = 1 mA	$V_{GS\,(th)}$	2.1	3.5	4.0	
Zero gate voltage drain current V_{DS} = 400 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	20	250	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 8.0 A	$R_{DS\,(on)}$	–	0.35	0.4	Ω

Dynamic characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 8.0 A	g_{fs}	3.3	6.2	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	3.8	4.9	nF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	300	500	nF
Reverse transfer capacitance V_{GS} = 0 V , V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	120	200	
Turn-on time t_{on} , ($t_{on} = t_{d\,(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_{GS} = 50 Ω	$t_{d\,(on)}$	–	50	75	ns
	t_r	–	80	120	
Turn-off time t_{off} , ($t_{off} = t_{d\,(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.9 A, R_{GS} = 50 Ω	$t_{d\,(off)}$	–	330	430	
	t_f	–	110	140	

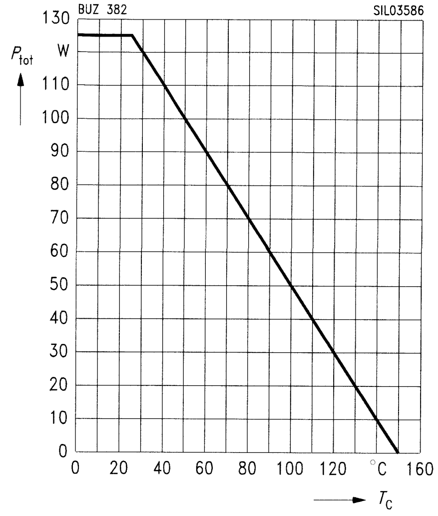
Electrical Characteristics (cont'd)
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse diode					
Continuous reverse drain current T_C = 25 ˚C	I_S	–	–	12.5	A
Pulsed reverse drain current T_C = 25 ˚C	I_{SM}	–	–	50	
Diode forward on-voltage I_S = 25 A, V_{GS} = 0 V	V_{SD}	–	1.3	1.7	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	t_{rr}	–	180	250	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs	Q_{rr}	–	0.65	1.2	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

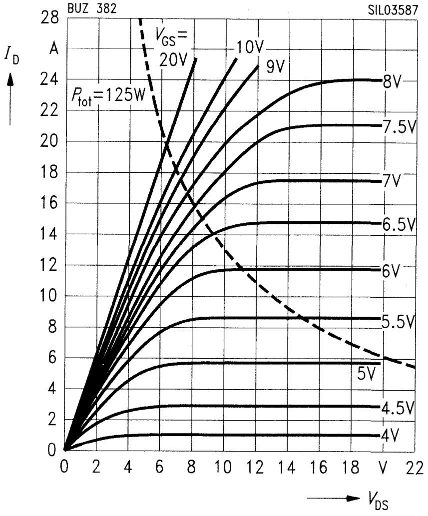
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$

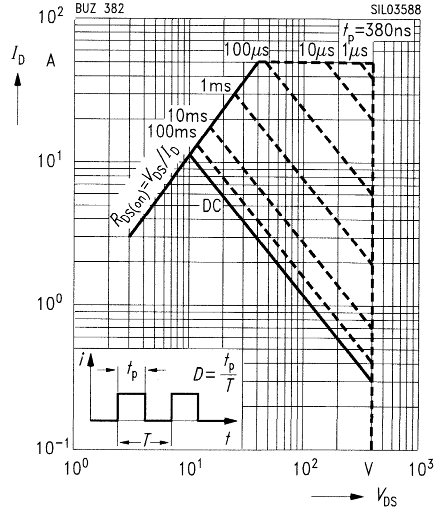
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$

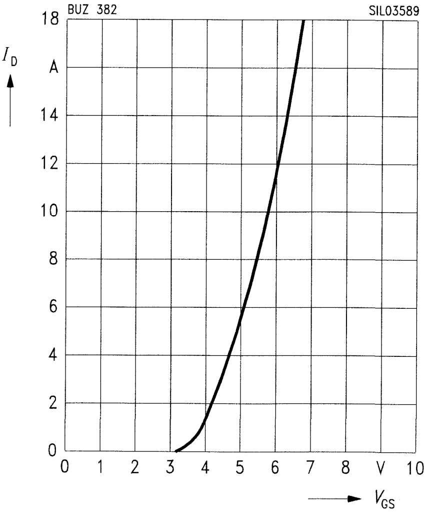
parameter: D = 0.01, T_C = 25 °C



Typ. transfer characteristics

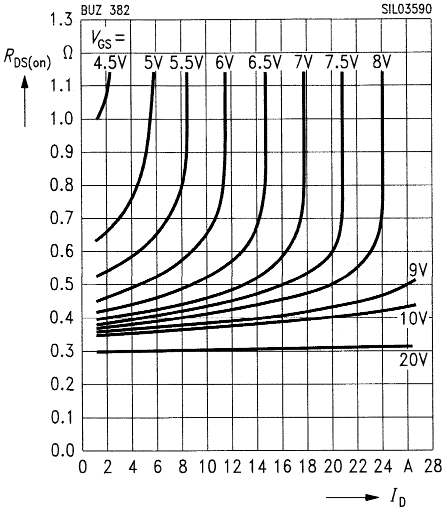
$I_D = f(V_{GS})$

parameter: t_p = 80 µs, V_{DS} = 25 V



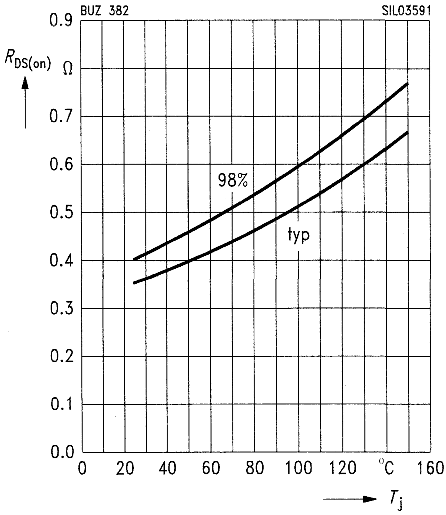
Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}



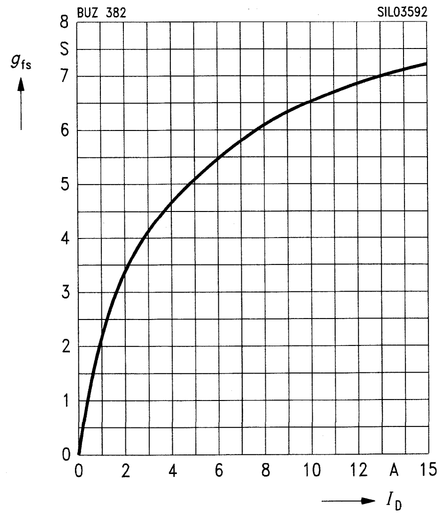
Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 8 A, V_{GS} = 10 V, (spread)



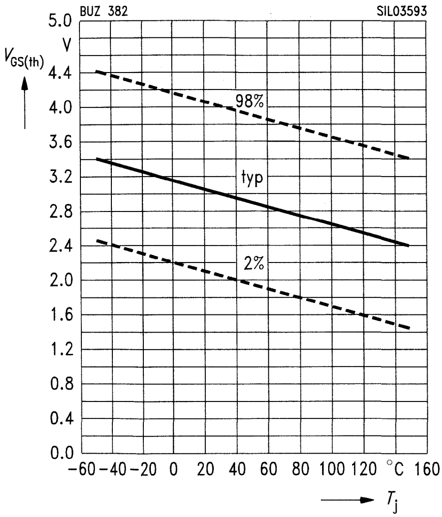
Typ.forward transconductance

$g_{fs} = f\,(I_D)$
parameter: t_p = 80 µs



Gate threshold voltage

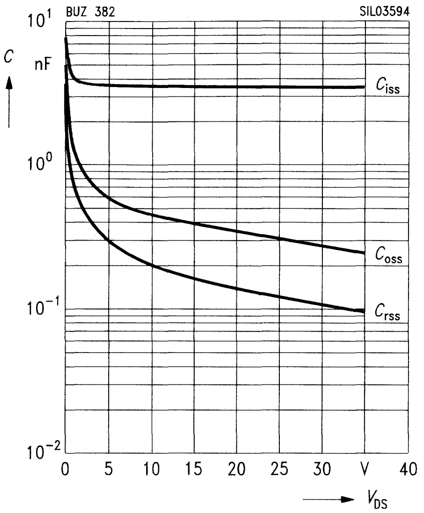
$V_{GS\,(th)} = f\,(T_j)$
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA, (spread)



Typ. capacitances

$C = f(V_{DS})$

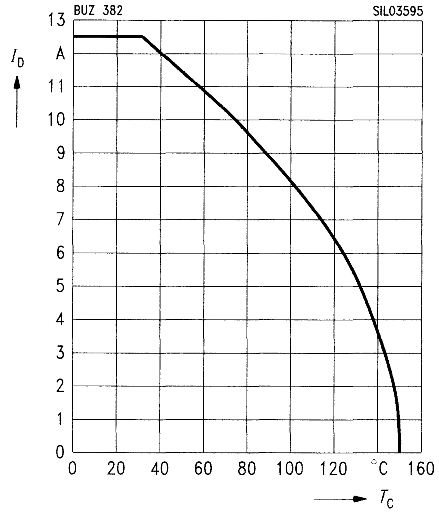
parameter: V_{GS} = 0 V, f = 1 MHz



Drain current

$I_D = f(T_C)$

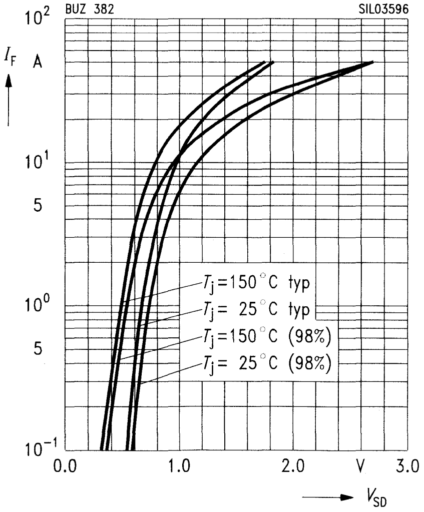
parameter: $V_{GS} \geq$ 10 V



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

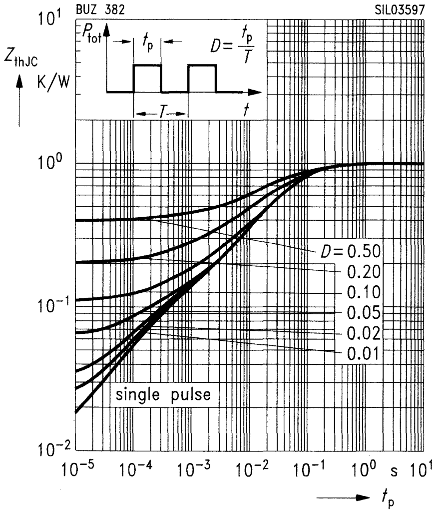
parameter: t_p = 80 µs, T_j



Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

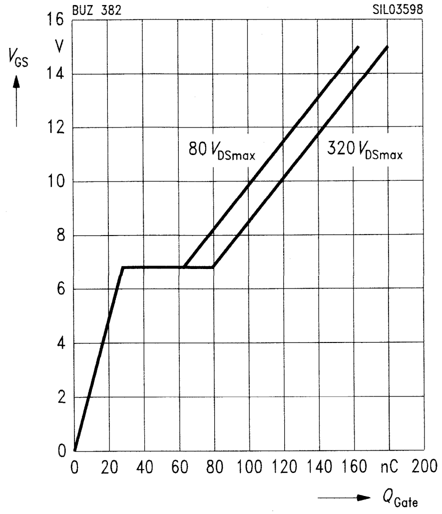
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{Gate})$

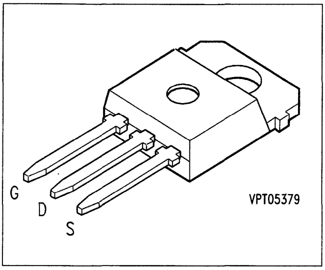
parameter: $I_{D\ puls} = 17.3$ A



SIPMOS® Power Transistors

BUZ 384
BUZ 385

- N channel
- Enhancement mode
- FREDFET



Type	V_{DS}	I_D	$R_{DS\,(on)}$	Package [1)]	Ordering Code
BUZ 384	500 V	10.5 A	0.6 Ω	TO-218 AA	C67078-A3209-A2
BUZ 385	500 V	9.0 A	0.8 Ω	TO-218 AA	C67078-A3210-A2

Maximum Ratings

Parameter	Symbol	BUZ		Unit
		384	**385**	
Continuous drain current, $T_C = 25$ °C	I_D	**10.5**	**9.0**	A
Pulsed drain current, $T_C = 25$ °C	$I_{D\,puls}$	**42**	**36**	
Drain-source voltage	V_{DS}	**500**		V
Drain-gate voltage, $R_{GS} = 20$ kΩ	V_{DGR}	**500**		
Gate-source voltage	V_{GS}	**± 20**		
Power dissipation, $T_C = 25$ °C	P_{tot}	**125**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		°C

Thermal resistance, chip-case	$R_{th\,JC}$	**≤ 1.0**	K/W
DIN humidity category, DIN 40 040		**E**	–
IEC climatic category, DIN IEC 68-1		**55/150/56**	

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	500	–	–	V
Gate threshold voltage V_{GS} = V_{DS} , I_D = 1 mA	$V_{GS(th)}$	2.1	3.0	4.0	
Zero gate voltage drain current V_{DS} = 500 V, V_{GS} = 0 V	I_{DSS}				µA
T_j = 25 °C		–	20	250	
T_j = 125 °C		–	100	1000	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	–	10	100	nA
Drain-source on-resistance V_{GS} = 10 V, I_D = 6.5 A	$R_{DS(on)}$	–	0.55	0.6	Ω
Dynamic characteristics					
Forward transconductance $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$, I_D = 6.5 A	g_{fs}	2.7	5.3	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	3800	4900	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	–	250	400	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	100	170	
Turn-on time t_{on}, ($t_{on} = t_{d(on)} + t_r$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.8 A, R_{GS} = 50 Ω	$t_{d(on)}$	–	50	75	ns
	t_r	–	80	120	
Turn-off time t_{off}, ($t_{off} = t_{d(off)} + t_f$) V_{DD} = 30 V, V_{GS} = 10 V, I_D = 2.8 A, R_{GS} = 50 Ω	$t_{d(off)}$	–	330	430	
	t_f	–	110	140	

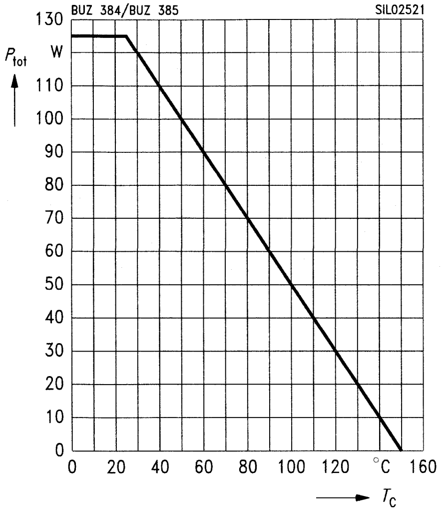
Electrical Characteristics (cont'd)
at T_j = 25 °C, unless otherwise specified.

Parameter		Symbol	Values			Unit
			min.	typ.	max.	
Reverse diode						
Continuous reverse drain current T_C = 25 °C		I_S				A
	BUZ 384		–	–	10.5	
	BUZ 385		–	–	9.0	
Pulsed reverse drain current T_C = 25 °C		I_{SM}				
	BUZ 384		–	–	42	
	BUZ 385		–	–	36	
Diode forward on-voltage I_S = 21 A, V_{GS} = 0 V		V_{SD}	–	1.3	1.7	V
Reverse recovery time V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		t_{rr}	–	180	250	ns
Reverse recovery charge V_R = 100 V, $I_F = I_S$, di_F / dt = 100 A/µs		Q_{rr}	–	0.65	1.2	µC

Characteristics at T_j = 25 °C, unless otherwise specified.

Total power dissipation

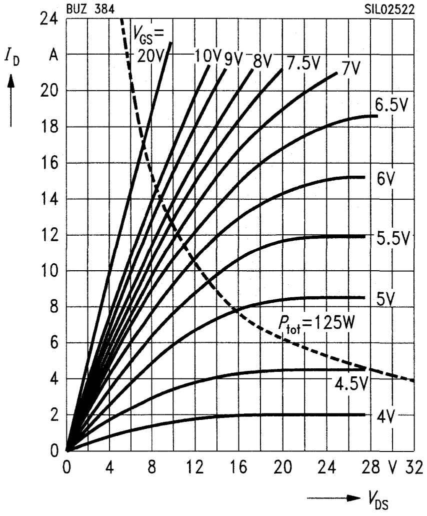
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 384**

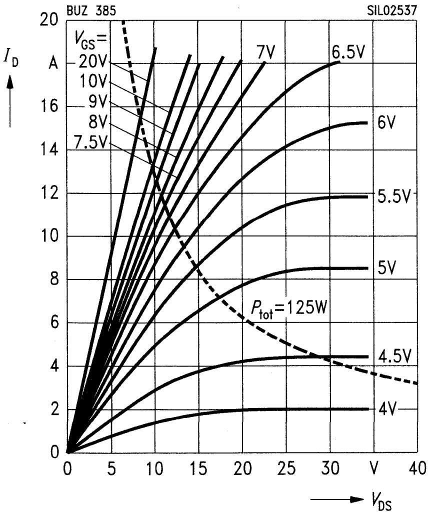
parameter: t_p = 80 µs



Typ. output characteristics

$I_D = f(V_{DS})$ **BUZ 385**

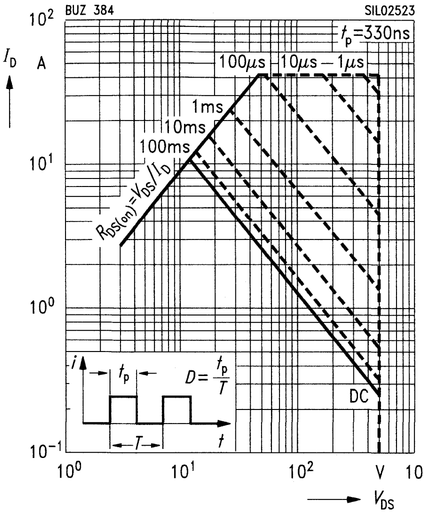
parameter: t_p = 80 µs



Safe operating area

$I_D = f(V_{DS})$ **BUZ 384**

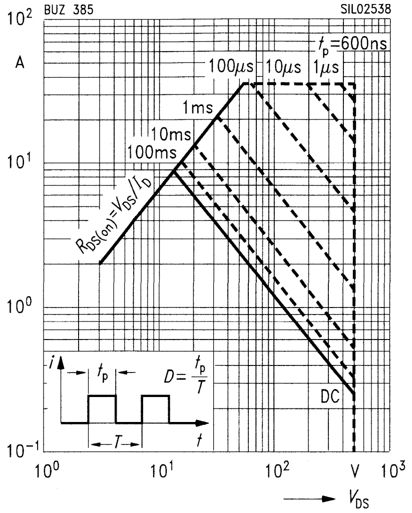
parameter: D = 0.01, T_C = 25 °C



Safe operating area

$I_D = f(V_{DS})$ **BUZ 385**

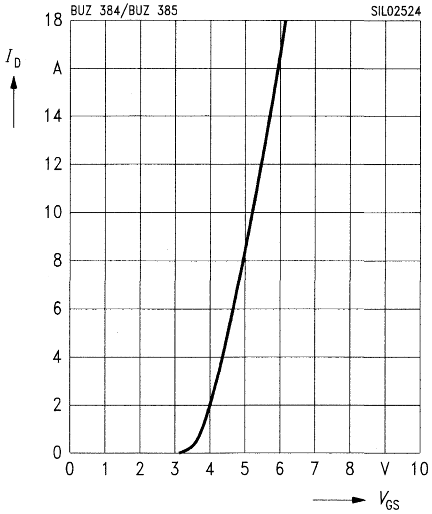
parameter: $D = 0.01$, $T_C = 25$ °C



Typ. transfer characteristics

$I_D = f(V_{GS})$

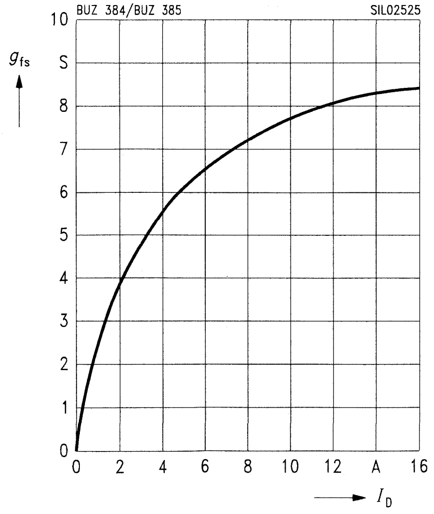
parameter: $t_p = 80$ μs, $V_{DS} = 25$ V



Typ. forward transconductance

$g_{fs} = f(I_D)$

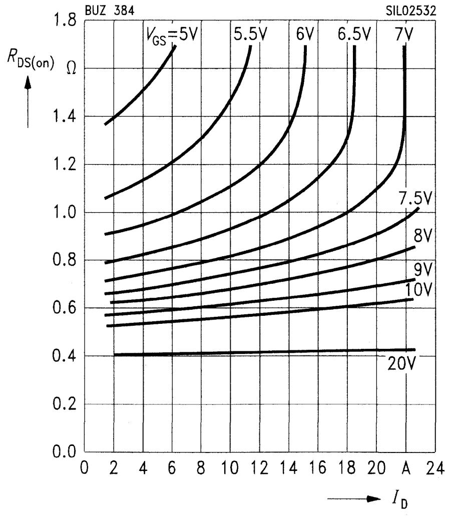
parameter: $t_p = 80$ μs



Typ. drain-source on-resistance

$R_{DS\,(on)} = f(I_D)$ **BUZ 384**

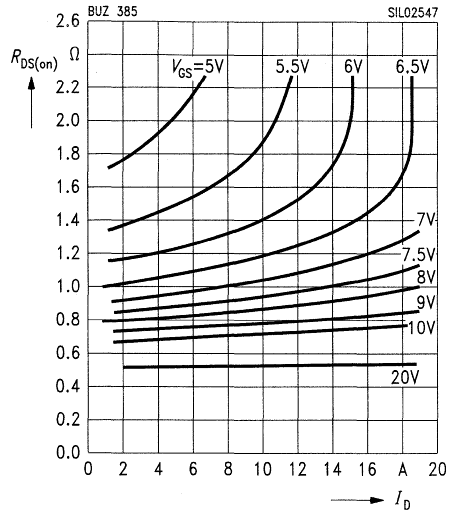
parameter: V_{GS}



Typ. drain-source on-resistance

$R_{DS\,(on)} = f\,(I_D)$ **BUZ 385**

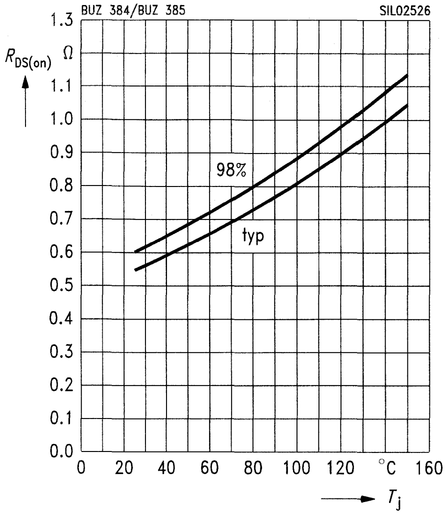
parameter: V_{GS}



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 384**

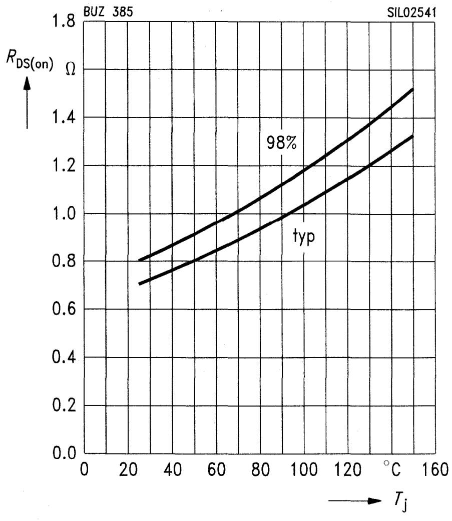
parameter: I_D = 6.5 A, V_{GS} = 10 V, (spread)



Drain-source on-resistance

$R_{DS\,(on)} = f\,(T_j)$ **BUZ 385**

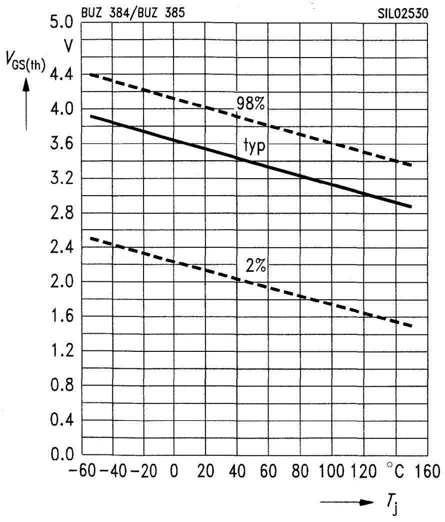
parameter: I_D = 6.5 A, V_{GS} = 10 V, (spread)



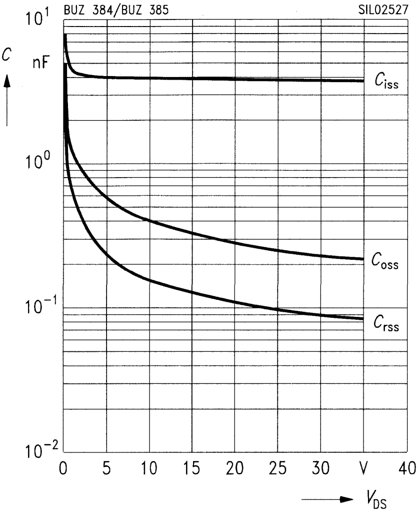
Gate threshold voltage

$V_{GS\,(th)} = f\,(T_j)$

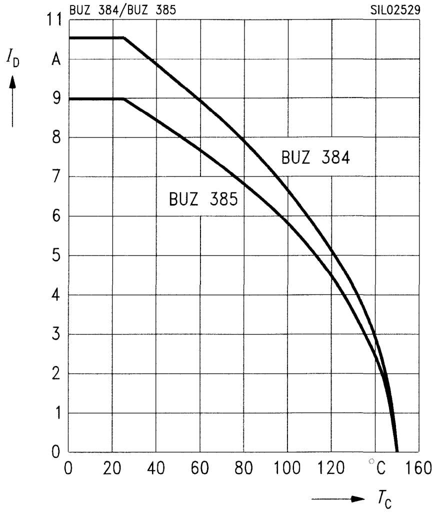
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA



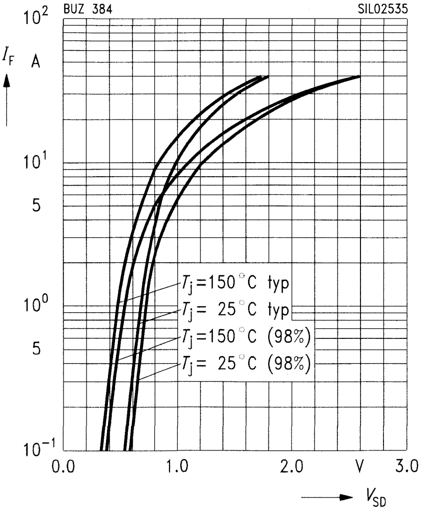
Typ. capacitances
$C = f(V_{DS})$
parameter: V_{GS} = 0 V, f = 1 MHz



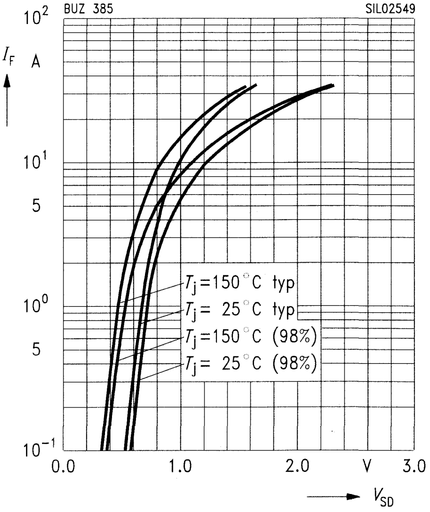
Drain current
$I_D = f(T_C)$
parameter: $V_{GS} \geq$ 10 V



Forward characteristics of reverse diode
$I_F = f(V_{SD})$ **BUZ 384**
parameter: t_p = 80 µs, T_j

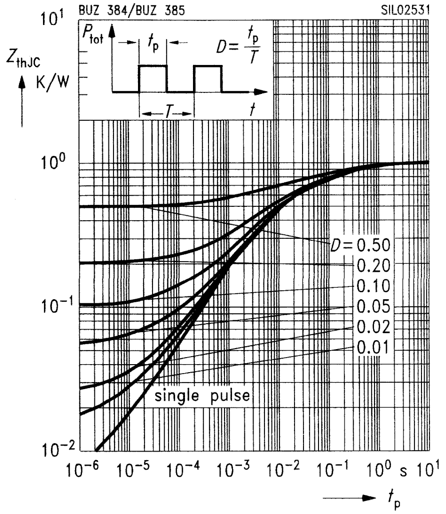


Forward characteristics of reverse diode
$I_F = f(V_{SD})$ **BUZ 385**
parameter: t_p = 80 µs, T_j



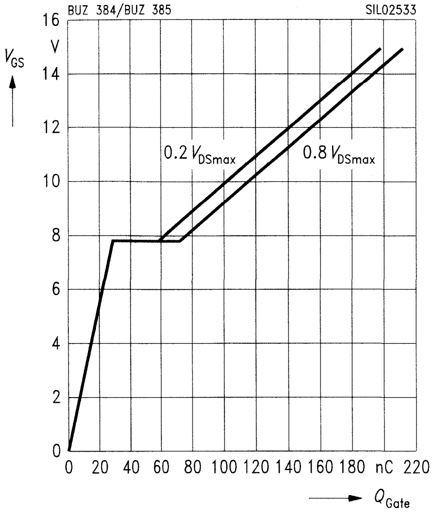
Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

$V_{GS} = f(Q_{\text{Gate}})$
parameter: $I_{\text{D puls}}$ = 14.4 A



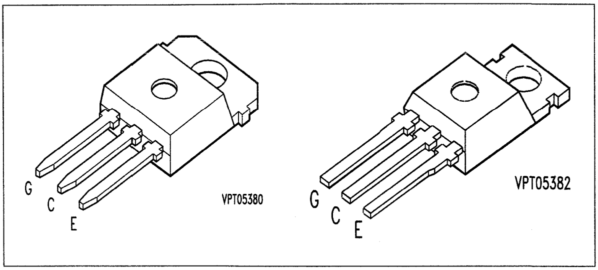
IGBT-Transistoren
Datenblätter
in alphanumerischer Reihenfolge

IGBT Transistors
Data sheets
in alphanumerical order

IGBT Transistors

BUP 200
BUP 300

- N channel
- MOS input (voltage-controlled)
- Low forward voltage drop
- High switching speed
- Very low tail current
- Low temperature sensitivity
- Avalanche-rated
- Latch-up-free
- Suitable free wheeling diode on request



Type	V_{CE}	I_C	Package [1]	Ordering Code
BUP 200	1200 V	3.5 A	TO-220 AB	C67078-A4400-A2
BUP 300	1200 V	3.5 A	TO-218 AA	C67078-A4203-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous collector current, T_C = 25 °C	I_C	**3.5**	A
T_C = 90 °C		**2.5**	
Pulsed collector current, T_C = 90 °C	$I_{C\,puls}$	**5**	
Repetitive avalanche current, $T_{j\,max}$ = 150 °C	I_{AR}	**0.3**	
Avalanche energy, single pulse I_C = 1.5 A, V_{CC} = 24 V, R_{GE} = 25 Ω	E_{AS}	**2**	mJ
Collector-emitter voltage	V_{CE}	**1200**	V
Gate-emitter voltage	V_{GE}	**± 20**	
Power dissipation, T_C = 25 °C	P_{tot}	**50**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance	$R_{th\,JC}$	**≤ 2.5**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

IGBT = **I**nsulated **G**ate **B**ipolar **T**ransistor

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Collector-emitter breakdown voltage V_{GE} = 0 V, I_C = 0.5 mA	$V_{(BR)\,CES}$	1200	–	–	V
Gate threshold voltage V_{GE} = V_{CE} , I_C = 0.1 mA	$V_{GE\,(th)}$	4.5	5.5	6.5	
Zero gate voltage collector current V_{CE} = 1000 V, V_{GE} = 0 V	I_{CES}				µA
T_j = 25 °C		–	1	25	
T_j = 125 °C		–	–	100	
Gate-emitter leakage current V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	–	0.1	100	nA
Collector-emitter saturation voltage V_{GE} = 15 V, I_C = 1.5 A	$V_{CE\,(sat)}$				V
T_j = 25 °C		–	2.8	3.3	
T_j = 125 °C		–	3.8	4.3	
T_j = 150 °C		–	4.0	4.5	
Dynamic characteristics					
Forward transconductance V_{CE} = 20 V, I_C = 1.5 A	g_{fs}		0.6	–	S
Input capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{iss}	–	225	–	pF
Output capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{oss}	–	25	–	
Reverse transfer capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{rss}	–	13	–	

Switching Characteristics

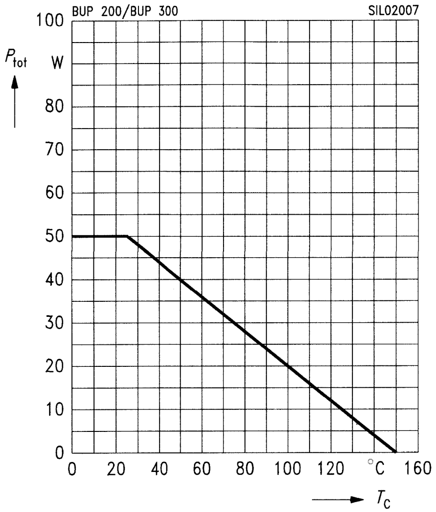
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Resistive load					
Turn-on delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 1.5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	$t_{d\,(on)}$	–	15	–	ns
Rise time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 1.5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	t_r	–	100	–	
Turn-off delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 1.5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	$t_{d\,(off)}$	–	120	–	
Fall time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 1.5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	t_f	–	150	–	
Inductive load					
Turn-off delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 1.5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	$t_{d\,(off)}$	90	120	150	ns
Fall time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 1.5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	t_f	15	20	30	
Turn-off loss ($E_{off} = E_{off\,1} + E_{off\,2}$) V_{CC} = 600 V, V_{GE} = 15 V, I_C = 1.5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	$E_{off\,1}$ $E_{off\,2}$	– –	0.09 0.1	–	mWs

Characteristics at $T_j = 25$ °C, unless otherwise specified.

Power dissipation

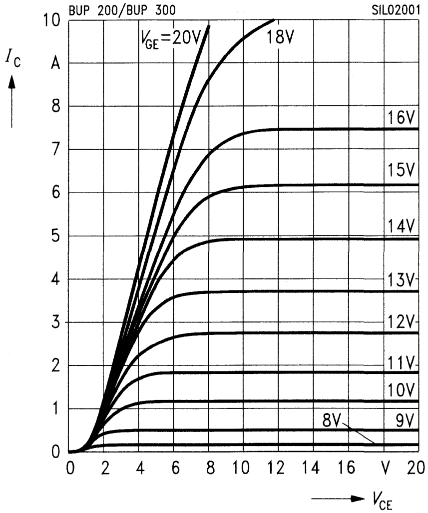
$P_{tot} = f\,(T_C)$



Typ. output characteristics

$I_C = f\,(V_{CE})$

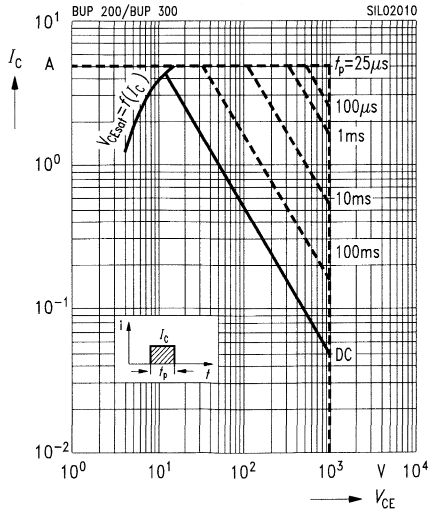
parameter: $t_p = 80$ µs



Safe operating area

$I_C = f\,(V_{CE})$

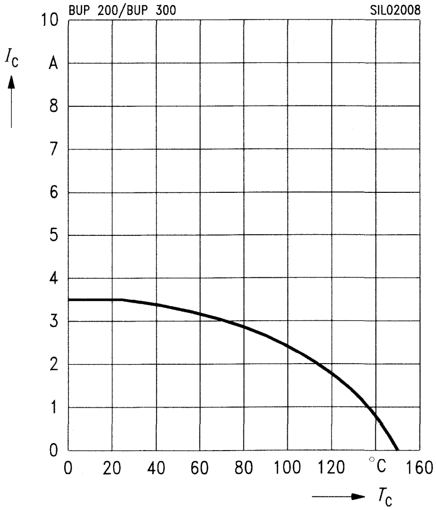
parameter: $T_C = 25$ °C, $T_j = 150$ °C



Collector current

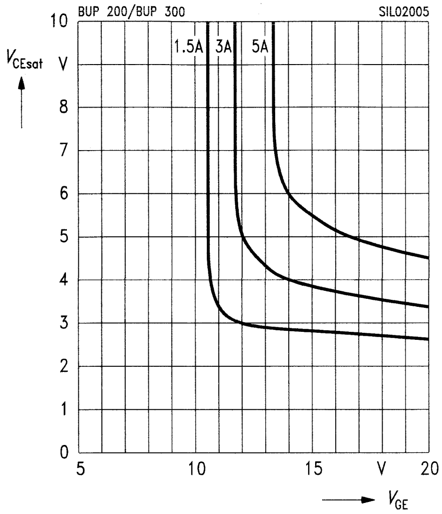
$I_C = f\,(T_C)$

parameter: $V_{GE} \geq 15$ V



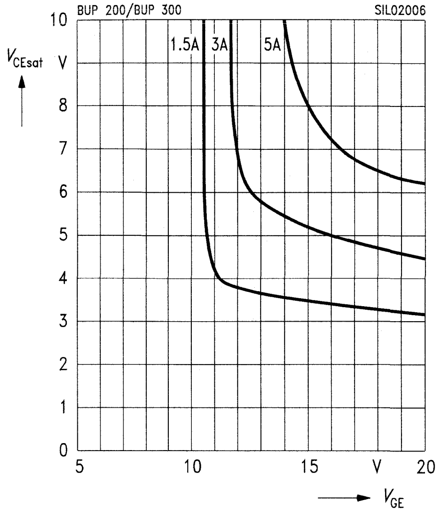
Typ. saturation characteristics

$V_{CE\,(sat)} = f\,(V_{GE})$
parameter: T_j = 25 °C



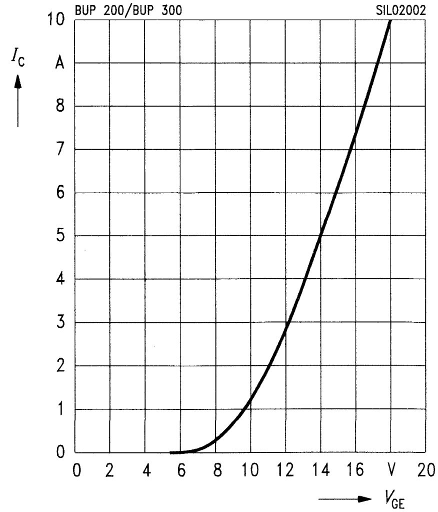
Typ. saturation characteristics

$V_{CE\,(sat)} = f\,(V_{GE})$
parameter: T_j = 125 °C



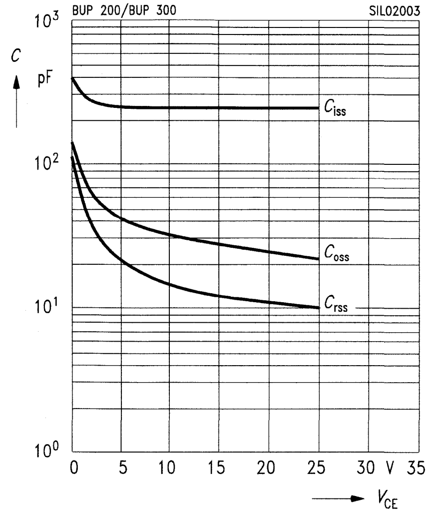
Typ. transfer characteristics

$I_C = f\,(V_{GE})$
parameter: t_p = 80 µs, V_{CE} = 20 V



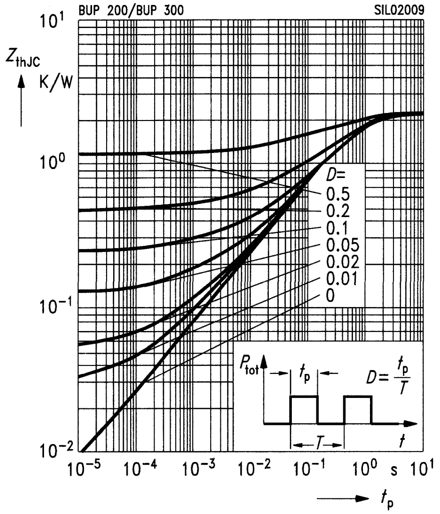
Typ. capacitances

$C = f\,(V_{CE})$
parameter: V_{GE} = 0 V, f = 1 MHz



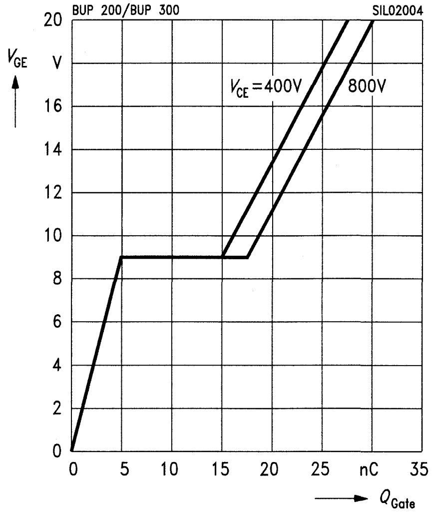
Transient thermal impedance

$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge

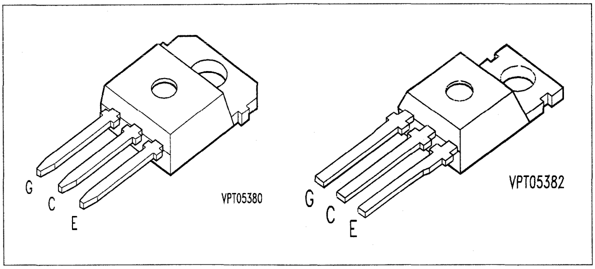
$V_{GE} = f(Q_{\text{Gate}})$
parameter: $I_{C\ \text{puls}} = 1$ A



IGBT Transistors

BUP 202
BUP 302

- N channel
- MOS input (voltage-controlled)
- Low forward voltage drop
- High switching speed
- Very low tail current
- Low temperature sensitivity
- Avalanche-rated
- Latch-up-free
- Suitable free wheeling diode on request



Type	V_{CE}	I_C	Package [1)]	Ordering Code
BUP 202	1000 V	12 A	TO-220 AB	C67078-A4401-A2
BUP 302	1000 V	12 A	TO-218 AA	C67078-A4205-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous collector current, $T_C = 25$ °C $T_C = 90$ °C	I_C	**12** **8**	A
Pulsed collector current, $T_C = 90$ °C	$I_{C\ puls}$	**16**	
Repetitive avalanche current, $T_{j\ max} = 150$ °C	I_{AR}	**1.6**	
Avalanche energy, single pulse $I_C = 5$ A, $V_{CC} = 24$ V, $R_{GE} = 25\ \Omega$	E_{AS}	**10**	mJ
Collector-emitter voltage	V_{CE}	**1000**	V
Gate-emitter voltage	V_{GE}	**± 20**	
Power dissipation, $T_C = 25$ °C	P_{tot}	**100**	W
Operating and storage temperature range	T_j, T_{stg}	**– 55 ... + 150**	°C

Thermal resistance	$R_{th\ JC}$	**≤ 1.25**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

IGBT = **I**nsulated **G**ate **B**ipolar **T**ransistor

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Collector-emitter breakdown voltage V_{GE} = 0 V, I_C = 0.1 mA	$V_{(BR)\,CES}$	1000	–	–	V
Gate threshold voltage $V_{GE} = V_{CE}$, I_C = 0.3 mA	$V_{GE\,(th)}$	4.5	5.5	6.5	
Zero gate voltage collector current V_{CE} = 1000 V, V_{GE} = 0 V T_j = 25 °C T_j = 125 °C	I_{CES}	 – –	 1 –	 100 300	µA
Gate-emitter leakage current V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	–	0.1	100	nA
Collector-emitter saturation voltage V_{GE} = 15 V, I_C = 5 A T_j = 25 °C T_j = 125 °C T_j = 150 °C	$V_{CE\,(sat)}$	 – – –	 2.8 3.8 4.0	 3.3 4.3 4.5	V
Dynamic characteristics					
Forward transconductance V_{CE} = 20 V, I_C = 5 A	g_{fs}	1.7	2.5	–	S
Input capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{iss}	–	650	–	pF
Output capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{oss}	–	50	–	
Reverse transfer capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{rss}	–	20	–	

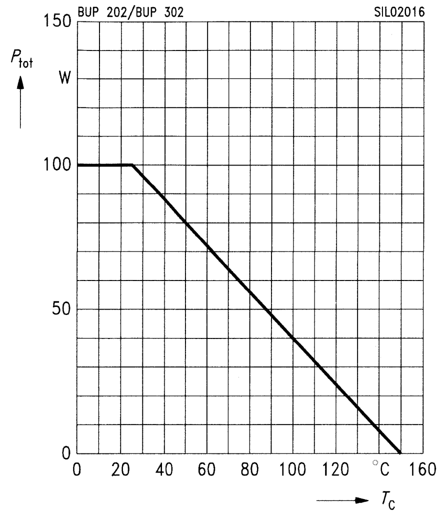
Switching Characteristics
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Resistive load					
Turn-on delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	$t_{d\,(on)}$	–	15	–	ns
Rise time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	t_r	–	100	–	
Turn-off delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	$t_{d\,(off)}$	–	120	–	
Fall time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	t_f	–	150	–	
Inductive load					
Turn-off delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	$t_{d\,(off)}$	90	120	150	ns
Fall time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	t_f	10	15	20	
Turn-off loss ($E_{off} = E_{off\,1} + E_{off\,2}$) V_{CC} = 600 V, V_{GE} = 15 V, I_C = 5 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	$E_{off\,1}$ $E_{off\,2}$	– –	0.25 0.35	–	mWs

Characteristics at $T_j = 25\ ^\circ C$, unless otherwise specified.

Power dissipation

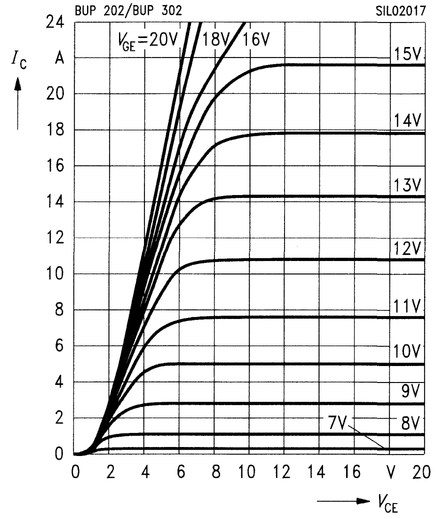
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_C = f(V_{CE})$

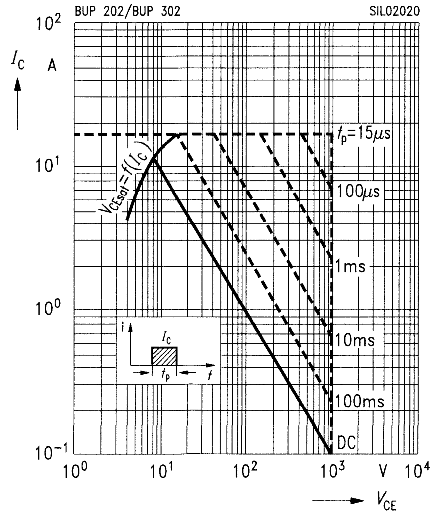
parameter: $t_p = 80\ \mu s$



Safe operating area

$I_C = f(V_{CE})$

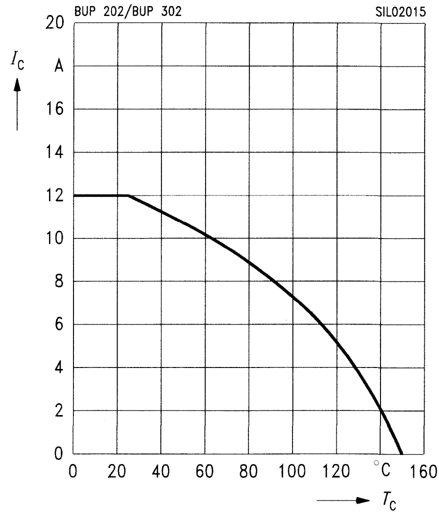
parameter: $T_C = 25\ ^\circ C$, $T_j \le 150\ ^\circ C$



Collector current

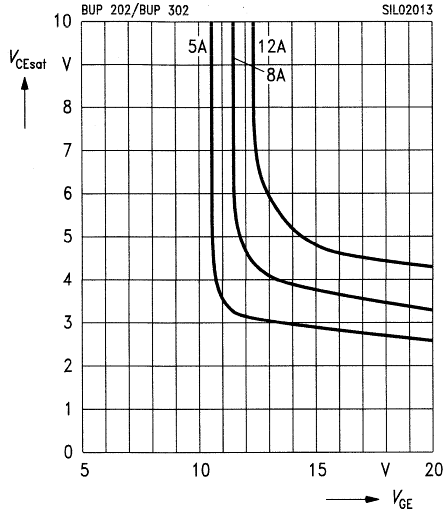
$I_C = f(T_C)$

parameter: $V_{GE} \ge 15$ V; $T_j \le 150\ ^\circ C$



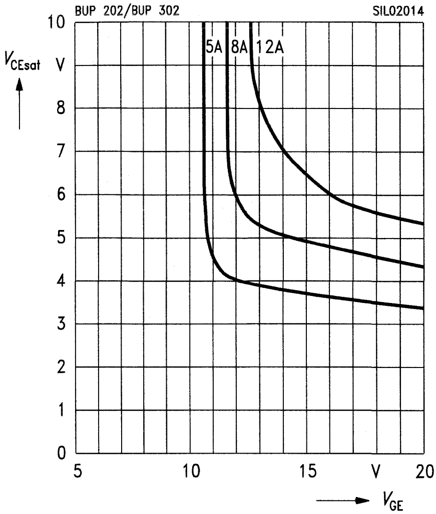
Typ. saturation characteristics

$V_{CE\,(sat)} = f\,(V_{GE})$
parameter: T_j = 25 °C



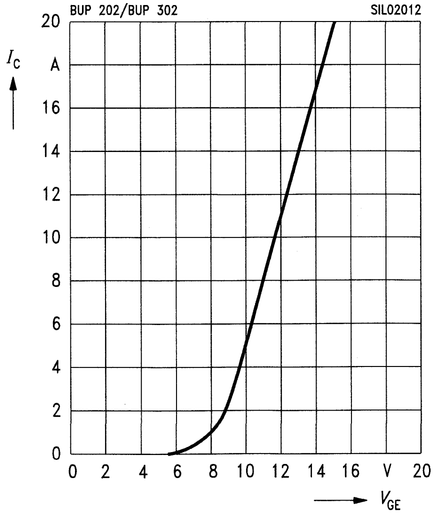
Typ. saturation characteristics

$V_{CE\,(sat)} = f\,(V_{GE})$
parameter: T_j = 125 °C



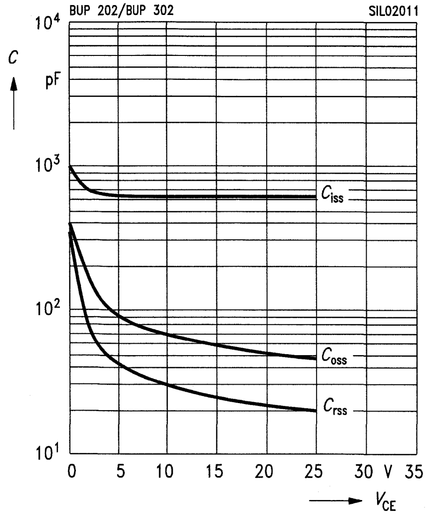
Typ. transfer characteristics

$I_C = f\,(V_{GE})$
parameter: t_p = 80 µs, V_{CE} = 20 V



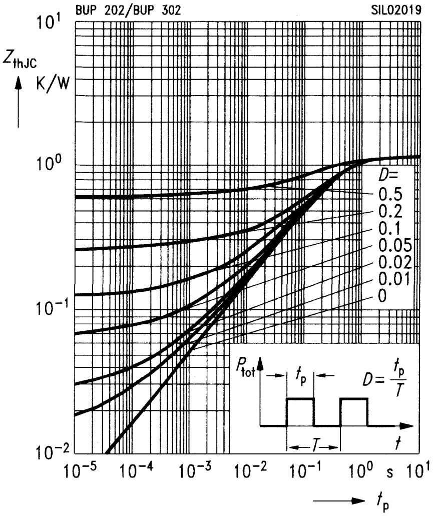
Typ. capacitances

$C = f\,(V_{CE})$
parameter: V_{GE} = 0 V, f = 1 MHz



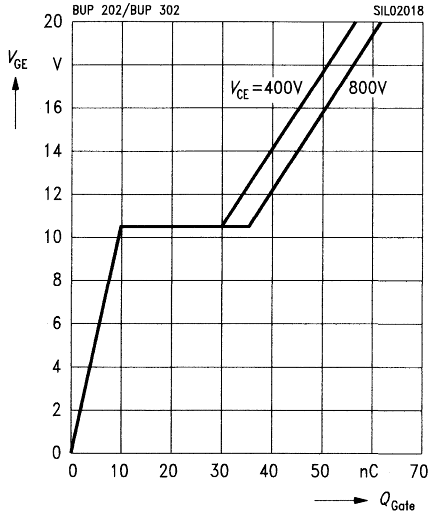
Transient thermal impedance

$Z_{\mathrm{th\,JC}} = f(t_p)$
parameter: $D = t_p / T$



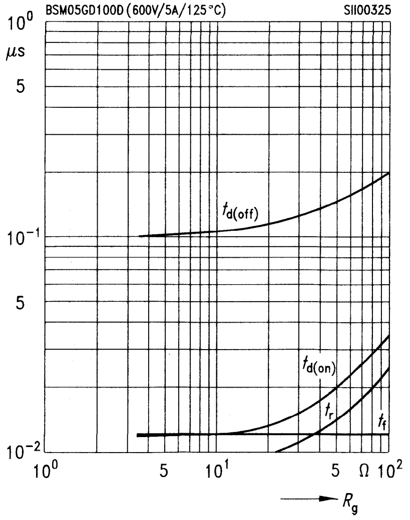
Typ. gate charge

$V_{GE} = f(Q_{\mathrm{Gate}})$
parameter: $I_{\mathrm{C\,puls}} = 6$ A



Typ. switching time $t = f(R_G)$ Inductive load

parameter: $T_j = 125$ °C, $V_{CE} = 600$ V,
$V_{GE} = \pm 15$ V, $I_C = 5$ A

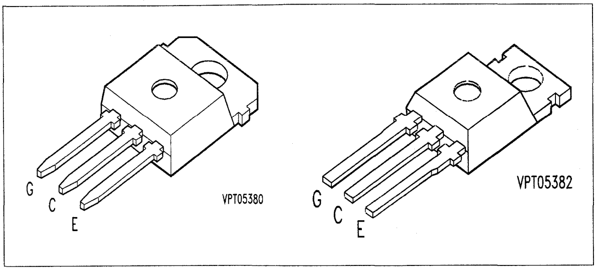


SIEMENS

IGBT Transistors

BUP 203
BUP 303

- N channel
- MOS input (voltage-controlled)
- Low forward voltage drop
- High switching speed
- Very low tail current
- Low temperature sensitivity
- Avalanche-rated
- Latch-up-free
- Suitable free wheeling diode BYP 101



Type	V_{CE}	I_C	**Package** [1]	**Ordering Code**
BUP 203	1000 V	21 A	TO-220 AB	C67078-A4402-A2
BUP 303	1000 V	21 A	TO-218 AA	C67078-A4202-A2

Maximum Ratings

Parameter	**Symbol**	**Values**	**Unit**
Continuous collector current, $T_C = 25$ °C $T_C = 90$ °C	I_C	**21** **15**	A
Pulsed collector current, $T_C = 90$ °C	$I_{C\,puls}$	**30**	
Repetitive avalanche current, $T_{j\,max} = 150$ °C	I_{AR}	**3**	
Avalanche energy, single pulse $I_C = 10$ A, $V_{CC} = 24$ V, $R_{GE} = 25\ \Omega$	E_{AS}	**20**	mJ
Collector-emitter voltage	V_{CE}	**1000**	V
Gate-emitter voltage	V_{GE}	**± 20**	
Power dissipation, $T_C = 25$ °C	P_{tot}	**165**	W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**	°C

Thermal resistance	$R_{th\,JC}$	**≤ 0.75**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

IGBT = **I**nsulated **G**ate **B**ipolar **T**ransistor

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Collector-emitter breakdown voltage V_{GE} = 0 V, I_C = 0.15 mA	$V_{(BR)\ CES}$	1000	–	–	V
Gate threshold voltage V_{GE} = V_{CE} , I_C = 0.7 mA	$V_{GE\ (th)}$	4.5	5.5	6.5	
Zero gate voltage collector current V_{CE} = 1000 V, V_{GE} = 0 V	I_{CES}				µA
T_j = 25 ˚C		–	1	150	
T_j = 125 ˚C		–	–	700	
Gate-emitter leakage current V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	–	0.1	100	nA
Collector-emitter saturation voltage V_{GE} = 15 V, I_C = 10 A	$V_{CE\ (sat)}$				V
T_j = 25 ˚C		–	2.8	3.3	
T_j = 125 ˚C		–	3.8	4.3	
T_j = 150 ˚C		–	4.0	4.5	
Dynamic characteristics					
Forward transconductance V_{CE} = 20 V, I_C = 10 A	g_{fs}	3.5	5.5	–	S
Input capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{iss}	–	1300	–	pF
Output capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{oss}	–	100	–	
Reverse transfer capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{rss}	–	50	–	

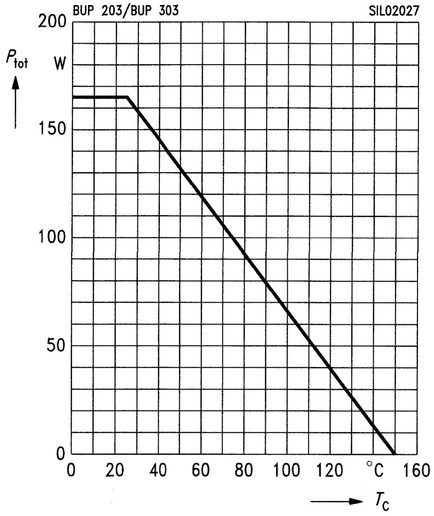
Switching Characteristics

at T_j = 25 °C, unless otherwise specified.

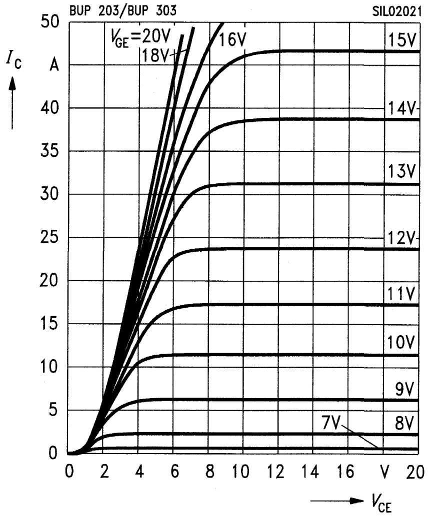
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Resistive load					
Turn-on delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 10 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	$t_{d\,(on)}$	–	15	–	ns
Rise time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 10A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	t_r	–	150	–	
Turn-off delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 10 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	$t_{d\,(off)}$	–	140	–	
Fall time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 10 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	t_f	–	200	–	
Inductive load					
Turn-off delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 10 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	$t_{d\,(off)}$	100	140	170	ns
Fall time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 10 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	t_f	10	20	30	
Turn-off loss ($E_{off} = E_{off\,1} + E_{off\,2}$) V_{CC} = 600 V, V_{GE} = 15 V, I_C = 10 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 °C	$E_{off\,1}$ $E_{off\,2}$	– –	0.5 0.6	–	mWs

Characteristics at $T_j = 25\ ^\circ\mathrm{C}$, unless otherwise specified.

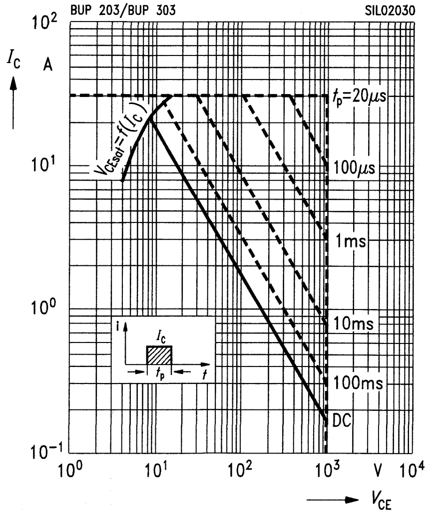
Power dissipation
$P_{tot} = f(T_C)$



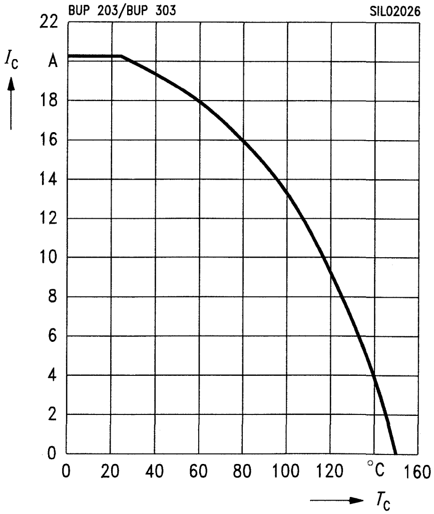
Typ. output characteristics
$I_C = f(V_{CE})$
parameter: $t_p = 80\ \mu s$



Safe operating area
$I_C = f(V_{CE})$
parameter: $T_C = 25\ ^\circ\mathrm{C}$, $T_j \leq 150\ ^\circ\mathrm{C}$

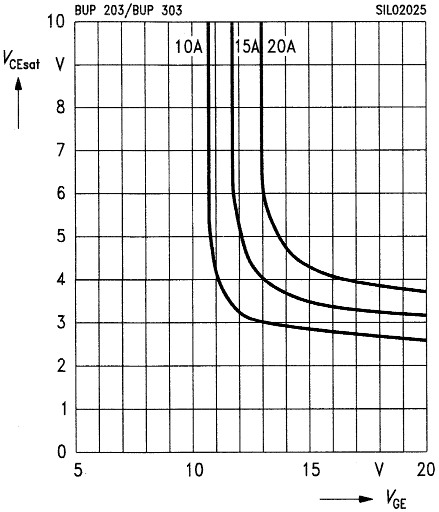


Collector current
$I_C = f(T_C)$
parameter: $V_{GE} \geq 15$ V; $T_j \leq 150\ ^\circ\mathrm{C}$



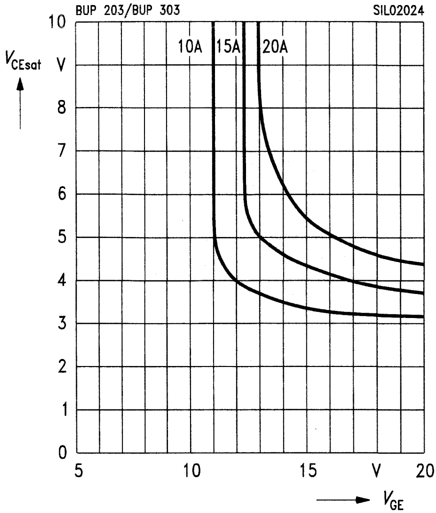
Typ. saturation characteristics

$V_{CE\,(sat)} = f\,(V_{GE})$
parameter: T_j = 25 °C



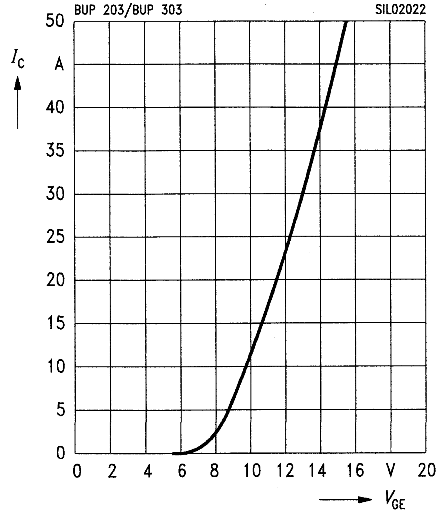
Typ. saturation characteristics

$V_{CE\,(sat)} = f\,(V_{GE})$
parameter: T_j = 125 °C



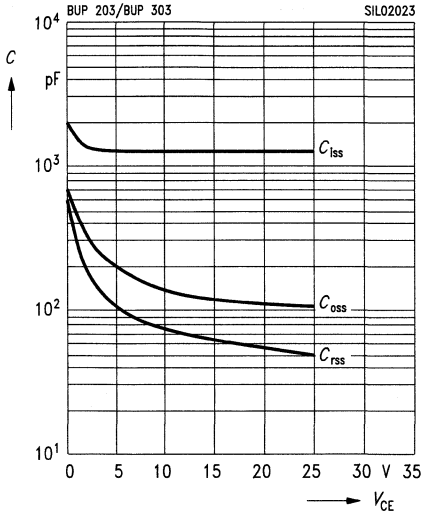
Typ. transfer characteristics

$I_C = f\,(V_{GE})$
parameter: t_p = 80 µs, V_{CE} = 20 V

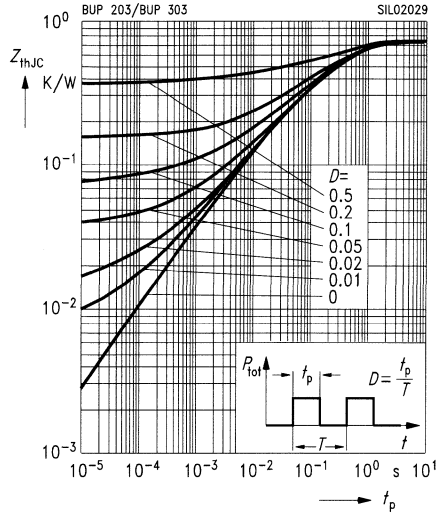


Typ. capacitances

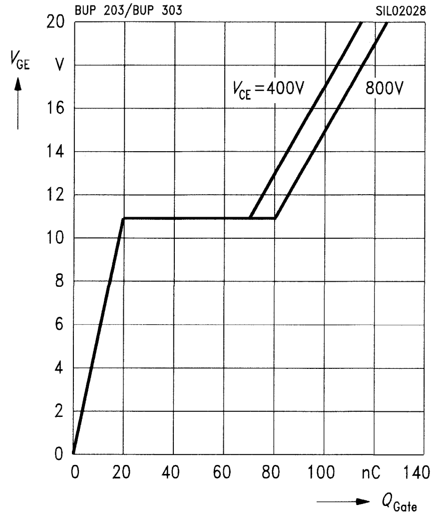
$C = f\,(V_{CE})$
parameter: V_{GE} = 0 V, f = 1 MHz



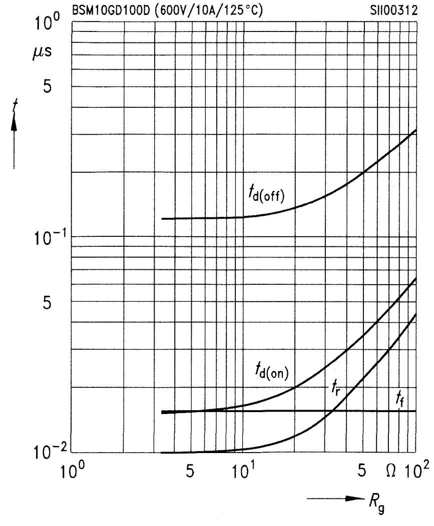
Transient thermal impedance
$Z_{\text{th JC}} = f(t_p)$
parameter: $D = t_p / T$



Typ. gate charge
$V_{GE} = f(Q_{\text{Gate}})$
parameter: $I_{\text{C puls}}$ = 10 A



Typ. switching time $t = f(R_G)$ Inductive load [1)]
parameter: T_j = 125 °C, V_{CE} = 600 V,
V_{GE} = ± 15 V, I_C = 10 A



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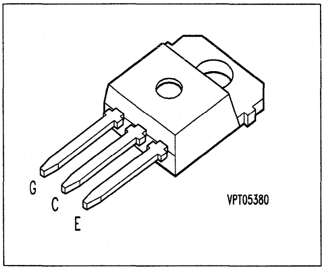
1) With freewheeling-diode BYP 101

IGBT Transistors

BUP 304
BUP 307

- N channel
- MOS input (voltage-controlled)
- Low forward voltage drop
- High switching speed
- Very low tail current
- Low temperature sensitivity
- Avalanche-rated
- Latch-up-free
- Suitable free wheeling diode
  1000 V: BYP 101 / BYP 102
  1200 V: On request



Type	V_{CE}	I_C	Package 1)	Ordering Code
BUP 304	1000 V	35 A	TO-218 AA	C67078-A4200-A2
BUP 307	1200 V	35 A	TO-218 AA	C67078-A4201-A2

Maximum Ratings

Parameter	Symbol	BUP		Unit
		304	307	
Continuous collector current, $T_C = 25$ °C $T_C = 90$ °C	I_C	**35** **25**		A
Pulsed collector current, $T_C = 90$ °C	$I_{C\,puls}$	**50**		
Repetitive avalanche current, $T_{j\,max} = 150$ °C	I_{AR}	**5**		
Avalanche energy, single pulse $I_C = 15$ A, $V_{CC} = 24$ V, $R_{GE} = 25\ \Omega$	E_{AS}	**22.5**		mJ
Collector-emitter voltage	V_{CE}	**1000**	**1200**	V
Gate-emitter voltage	V_{GE}	**± 20**		
Power dissipation, $T_C = 25$ °C	P_{tot}	**310**		W
Operating and storage temperature range	T_j , T_{stg}	**– 55 ... + 150**		°C

Thermal resistance	$R_{th\,JC}$	**≤ 0.4**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**55/150/56**	

IGBT = **I**nsulated **G**ate **B**ipolar **T**ransistor

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1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Static characteristics					
Collector-emitter breakdown voltage	$V_{(BR)CES}$				V
V_{GE} = 0 V, I_C = 0.25 mA BUP 304		1000	–	–	
BUP 307		1200	–	–	
Gate threshold voltage V_{GE} = V_{CE} , I_C = 1 mA	$V_{GE(th)}$	4.5	5.5	6.5	
Zero gate voltage collector current V_{CE} = 1000 V, V_{GE} = 0 V BUP 304 V_{CE} = 1200 V, V_{GE} = 0 V BUP 307	I_{CES}				µA
T_j = 25 ˚C		–	1	250	
T_j = 125 ˚C		–	–	1000	
Gate-emitter leakage current V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	–	0.1	100	nA
Collector-emitter saturation voltage V_{GE} = 15 V, I_C = 15 A	$V_{CE(sat)}$				V
T_j = 25 ˚C		–	2.8	3.3	
T_j = 125 ˚C		–	3.8	4.3	
T_j = 150 ˚C		–	4.0	4.5	
Dynamic characteristics					
Forward transconductance V_{CE} = 20 V, I_C = 15 A	g_{fs}	5.5	8	–	S
Input capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{iss}	–	2000	–	pF
Output capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{oss}	–	160	–	
Reverse transfer capacitance V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{rss}	–	65	–	

Switching Characteristics

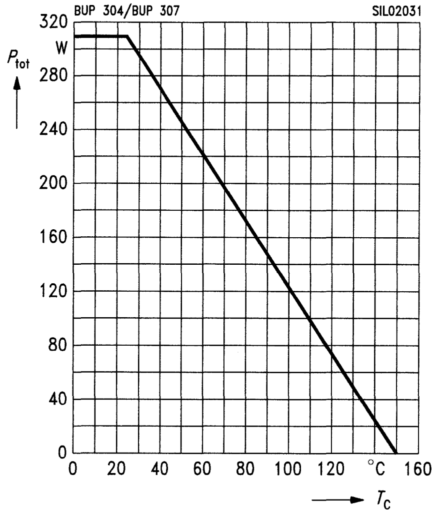
at T_j = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Resistive load					
Turn-on delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 15 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	$t_{d\,(on)}$	–	15	–	ns
Rise time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 15A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	t_r	–	200	–	
Turn-off delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 15 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	$t_{d\,(off)}$	–	150	–	
Fall time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 15 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	t_f	–	300	–	
Inductive load					
Turn-off delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 15 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	$t_{d\,(off)}$	10	15	20	ns
Fall time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 15 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	t_f	5	10	15	
Turn-off loss ($E_{off} = E_{off\,1} + E_{off\,2}$) V_{CC} = 600 V, V_{GE} = 15 V, I_C = 15 A $R_{g\,(on)}$ = 3.3 Ω, $R_{g\,(off)}$ = 3.3 Ω, T_j = 125 ˚C	$E_{off\,1}$ $E_{off\,2}$	– –	0.7 0.8	–	mWs

Characteristics at T_j = 25 °C, unless otherwise specified.

Power dissipation

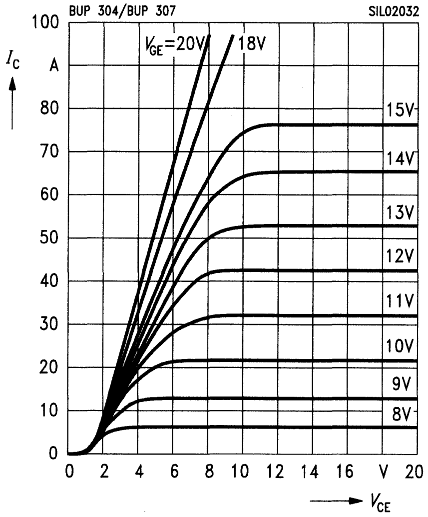
$P_{tot} = f(T_C)$



Typ. output characteristics

$I_C = f(V_{CE})$

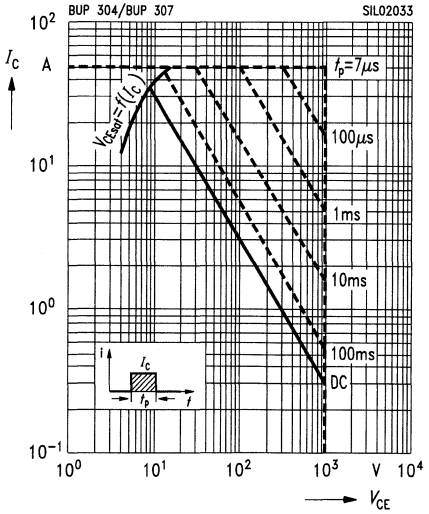
parameter: t_p = 80 µs



Safe operating area

$I_C = f(V_{CE})$

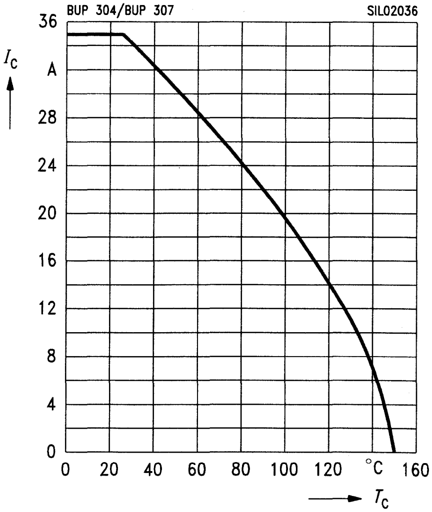
parameter: T_C = 25 °C, T_j = 150 °C



Collector current

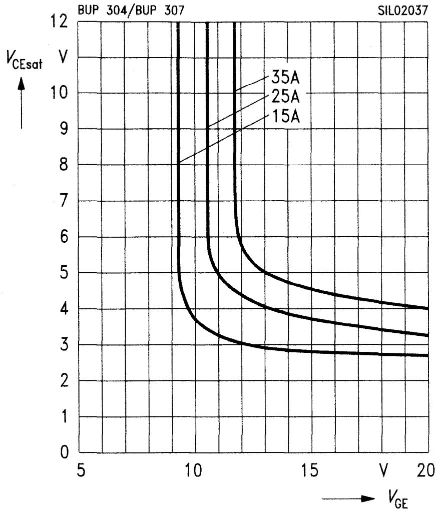
$I_C = f(T_C)$

parameter: $V_{GE} \geq 15$ V; $T_j \leq 150$ °C



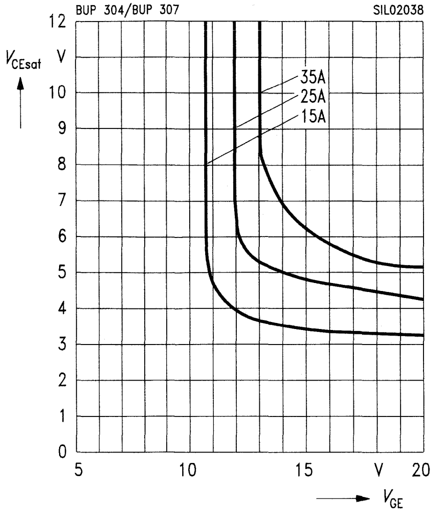
Typ. saturation characteristics

$V_{CE\,(sat)} = f\,(V_{GE})$
parameter: T_j = 25 °C



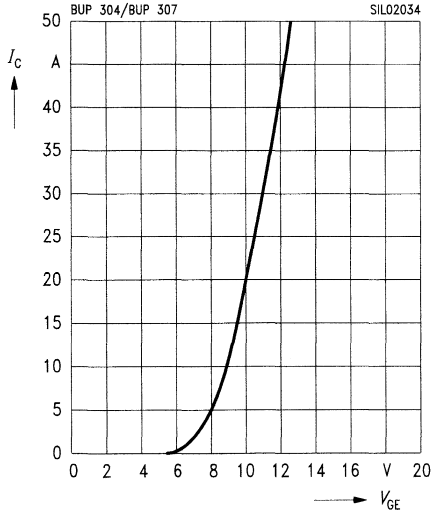
Typ. saturation characteristics

$V_{CE\,(sat)} = f\,(V_{GE})$
parameter: T_j = 125 °C



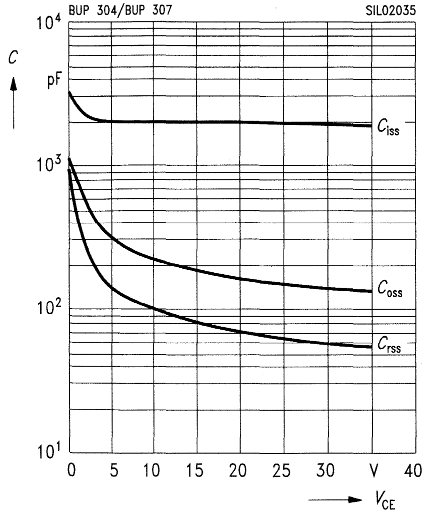
Typ. transfer characteristics

$I_C = f\,(V_{GE})$
parameter: t_p = 80 µs, V_{CE} = 20 V



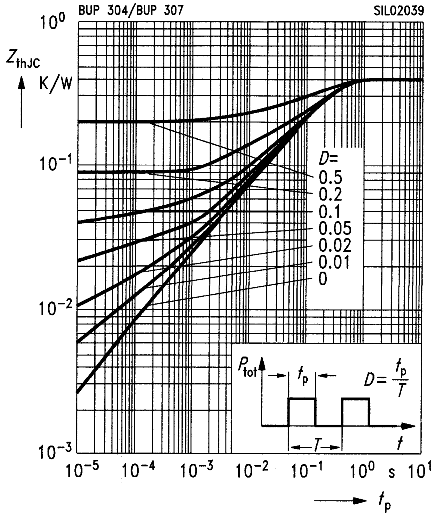
Typ. capacitances

$C = f\,(V_{CE})$
parameter: V_{GE} = 0 V, f = 1 MHz



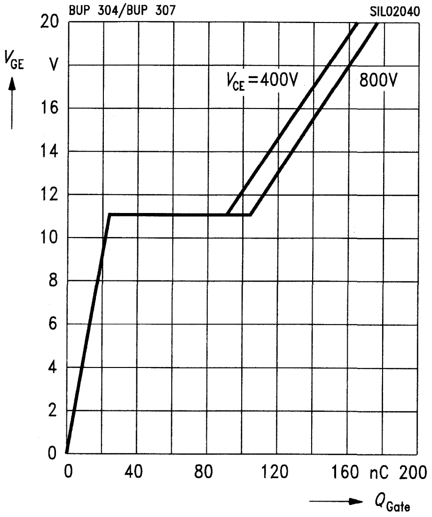
Transient thermal impedance

$Z_{th\,JC} = f(t_p)$
parameter: $D = t_p / T$



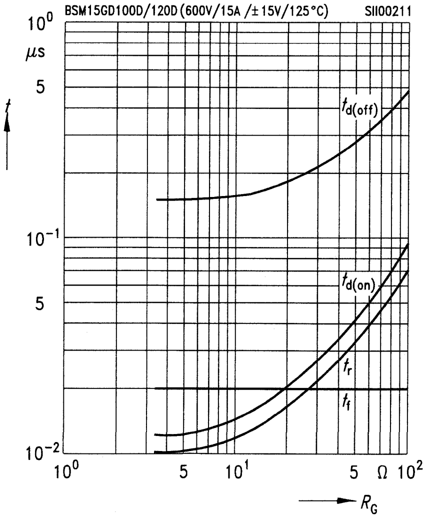
Typ. gate charge

$V_{GE} = f(Q_{Gate})$
parameter: $I_{C\,puls}$ = 20 A



Typ. switching time $t = f(R_G)$ Inductive load [1]

parameter: T_j = 125 °C, V_{CE} = 600 V,
V_{GE} = ± 15 V, I_C = 15 A



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[1] With freewheeling-diode BYP 101/BYP 102

FRED-Dioden
Datenblätter
in alphanumerischer Reihenfolge

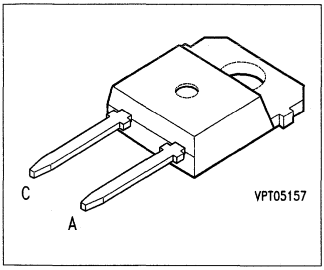
FRED Diodes
Data sheets
in alphanumerical order

FRED Diode

BYP 100

Preliminary data

- Soft recovery characteristics



Type	V_{RRM}	I_{FRMS}	t_{rr}	Package 1)	Ordering Code
BYP 100	1000 V	8.0 A	55 ns	TO-218 AD	C67047-A2254-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Mean forward current T_C = 90 ˚C, D = 0.5	I_{FAV}	**5.0**	A
RMS forward current	I_{FRMS}	**8.0**	
Surge forward current T_j = 100 ˚C, 50-Hz sine halfwave, aperiodic	I_{FSM}	**20**	
Repetitive peak forward current T_j = 100 ˚C, $t_p \leq 10\ \mu s$	I_{FRM}	**50**	
i^2t value T_j = 100 ˚C, t_p = 10 ms	$\int i^2 dt$	**2.0**	A^2s
Repetitive peak reverse voltage	V_{RRM}	**1000**	V
Surge peak reverse voltage	V_{RSM}	**1000**	
Power dissipation T_C = 90 ˚C	P_{tot}	**15**	W
Operating and storage temperature range	T_j , T_{stg}	**– 40 ... + 150**	˚C

Thermal resistance Chip-case Chip-ambient, without heat sink	 $R_{th\ JC}$ $R_{th\ JA}$	 **≤ 9.8** **≤ 46**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**40/150/56**	

FRED = **F**ast **R**ecovery **E**pitaxial **D**iode

1) See chapter Package Outlines.

Electrical Characteristics

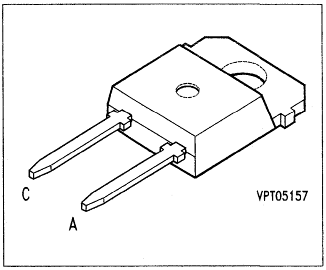
at $T_j = 25$ °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Forward voltage drop $I_F = 5$ A $T_j = 25$ °C $T_j = 100$ °C	V_F	 – –	 2.0 1.7	 2.45 –	V
Reverse current $V_R = 1000$ V $T_j = 25$ °C $T_j = 100$ °C $T_j = 150$ °C	I_R	 – – –	 0.01 0.05 0.15	 – – –	mA
Dynamic characteristics					
Reverse recovery charge $I_F = 5$ A, $V_{CC} = 300$ V $di_F / dt = -800$ A / µs, $T_j = 100$ °C	Q_{rr}	–	0.8	–	µC
Peak reverse recovery current $I_F = 5$ A, $V_{CC} = 300$ V $di_F / dt = -800$ A / µs, $T_j = 100$ °C	I_{RRM}	–	22	–	A
Reverse recovery time $I_F = 5$ A, $V_{CC} = 300$ V $di_F / dt = -800$ A / µs, $T_j = 100$ °C	t_{rr}	–	55	–	ns
Storage time $I_F = 5$ A, $V_{CC} = 300$ V $di_F / dt = -800$ A / µs, $T_j = 100$ °C	t_s	–	30	–	
Soft factor $I_F = 5$ A, $V_{CC} = 300$ V $di_F / dt = -800$ A / µs, $T_j = 100$ °C	S	–	0.8	–	–

FRED Diode

BYP 101

- Soft recovery characteristics



Type	V_{RRM}	I_{FRMS}	t_{rr}	Package[1)]	Ordering Code
BYP 101	1000 V	25 A	80 ns	TO-218 AD	C67047-A2072-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Mean forward current $T_C = 90\ ^\circ C, D = 0.5$	I_{FAV}	**15**	A
RMS forward current	I_{FRMS}	**25**	
Surge forward current $T_j = 100\ ^\circ C$, 50-Hz sine halfwave, aperiodic	I_{FSM}	**70**	
Repetitive peak forward current $T_j = 100\ ^\circ C, t_p \leq 10\ \mu s$	I_{FRM}	**150**	
i^2t value $T_j = 100\ ^\circ C, t_p = 10$ ms	$\int i^2 dt$	**25**	A^2s
Repetitive peak reverse voltage	V_{RRM}	**1000**	V
Surge peak reverse voltage	V_{RSM}	**1000**	
Power dissipation $T_C = 90\ ^\circ C$	P_{tot}	**40**	W
Operating and storage temperature range	T_j , T_{stg}	**– 40 ... + 150**	˚C

Thermal resistance Chip-case Chip-ambient, without heat sink	 $R_{th\,JC}$ $R_{th\,JA}$	 **≤ 1.5** **≤ 46**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**40/150/56**	

FRED = **F**ast **R**ecovery **E**pitaxial **D**iode

1) See chapter Package Outlines.

Electrical Characteristics

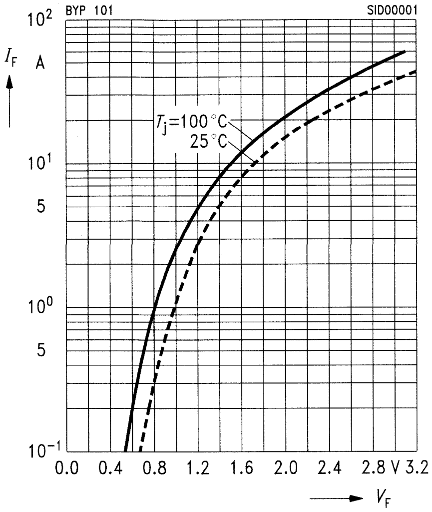
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Forward voltage drop I_F = 15 A T_j = 25 °C T_j = 100 °C	V_F	 – –	 2.0 1.7	 2.4 –	V
Reverse current V_R = 1000 V T_j = 25 °C T_j = 100 °C T_j = 150 °C	I_R	 – – –	 0.01 0.05 0.15	 – – –	mA
Max. forward characteristic T_j = 100 °C	V_F	$1.35 + 0.035 \times I_F$			V
Forward power dissipation T_j = 100 °C	P_F	$1.35 \times I_{FAV} + 0.035 \times (I_{FRMS})^2$			W
Dynamic characteristics					
Reverse recovery charge I_F = 15 A, V_{CC} = 300 V $di_F / dt = -1000$ A / µs, T_j = 100 °C	Q_{rr}	–	2.2	–	µC
Peak reverse recovery current I_F = 15 A, V_{CC} = 300 V $di_F / dt = -1000$ A / µs, T_j = 100 °C	I_{RRM}	–	35	–	A
Reverse recovery time I_F = 15 A, V_{CC} = 300 V $di_F / dt = -1000$ A / µs, T_j = 100 °C	t_{rr}	–	80	–	ns
Storage time I_F = 15 A, V_{CC} = 300 V $di_F / dt = -1000$ A / µs, T_j = 100 °C	t_s	–	45	–	
Soft factor I_F = 15 A, V_{CC} = 300 V $di_F / dt = -1000$ A / µs, T_j = 100 °C	S	–	0.8	–	–

Characteristics

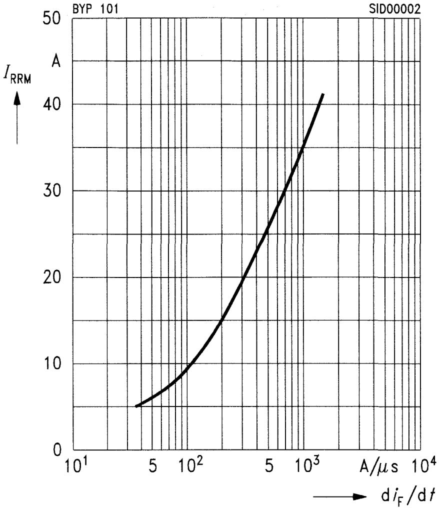
Typ. forward characteristics

$I_F = f(V_F)$
parameter: T_j



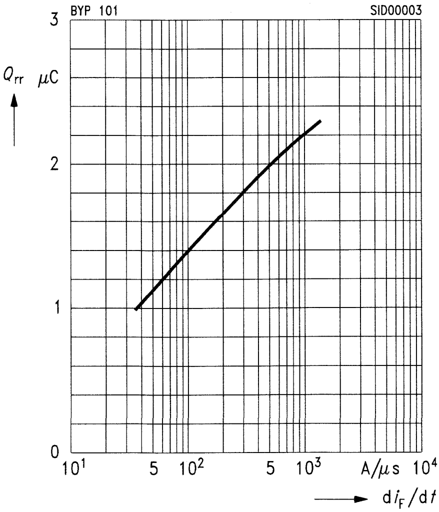
Typ. reverse current

$I_{RRM} = f(di_F / dt)$
parameter: V_{CC} = 300 V, I_F = 15 A, T_j = 100 °C



Typ. reverse recovery charge

$Q_{rr} = f(di_F / dt)$
parameter: V_{CC} = 300 V, I_F = 15 A, T_j = 100 °C

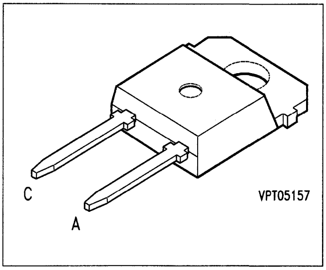


SIEMENS

FRED Diode

BYP 102

- Soft recovery characteristics



Type	V_{RRM}	I_{FRMS}	t_{rr}	Package [1]	Ordering Code
BYP 102	1000 V	50 A	130 ns	TO-218 AD	C67047-A2071-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Mean forward current $T_C = 90$ °C, $D = 0.5$	I_{FAV}	**28**	A
RMS forward current	I_{FRMS}	**50**	
Surge forward current $T_j = 100$ °C, 50-Hz sine halfwave, aperiodic	I_{FSM}	**125**	
Repetitive peak forward current $T_j = 100$ °C, $t_p \leq 10$ µs	I_{FRM}	**280**	
i^2t value $T_j = 100$ °C, $t_p = 10$ ms	$\int i^2 dt$	**78**	A^2s
Repetitive peak reverse voltage	V_{RRM}	**1000**	V
Surge peak reverse voltage	V_{RSM}	**1000**	
Power dissipation $T_C = 90$ °C	P_{tot}	**75**	W
Operating and storage temperature range	T_j , T_{stg}	**– 40 ... + 150**	°C

Thermal resistance Chip-case Chip-ambient, without heat sink	 $R_{th\ JC}$ $R_{th\ JA}$	 **≤ 0.8** **≤ 46**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**40/150/56**	

FRED = **F**ast **R**ecovery **E**pitaxial **D**iode

[1] See chapter Package Outlines.

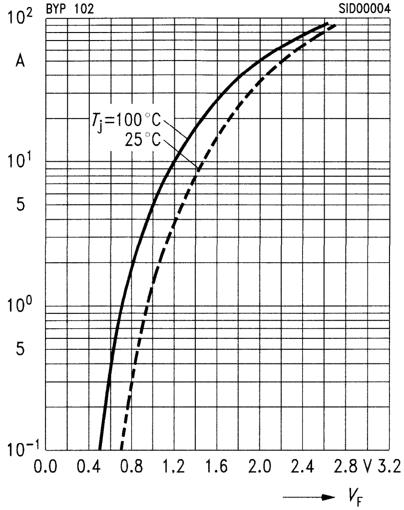
Electrical Characteristics
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Forward voltage drop	V_F				V
T_j = 25 °C, I_F = 20 A		–	1.65	–	
I_F = 30 A		–	1.9	2.35	
T_j = 100 °C, I_F = 20 A		–	1.5	–	
I_F = 30 A		–	1.7	–	
Reverse current V_R = 1000 V	I_R				mA
T_j = 25 °C		–	0.01	–	
T_j = 100 °C		–	0.05	–	
T_j = 150 °C		–	0.15	–	
Max. forward characteristic T_j = 100 °C	V_F	$1.2 + 0.021 \times I_F$			V
Forward power dissipation T_j = 100 °C	P_F	$1.2 \times I_{FAV} + 0.021 \times (I_{FRMS})^2$			W
Dynamic characteristics					
Reverse recovery charge I_F = 28 A, V_{CC} = 300 V di_F / dt = – 1000 A / µs, T_j = 100 °C	Q_{rr}	–	4.5	–	µC
Peak reverse recovery current I_F = 28 A, V_{CC} = 300 V di_F / dt = – 1000 A / µs, T_j = 100 °C	I_{RRM}	–	50	–	A
Reverse recovery time I_F = 28 A, V_{CC} = 300 V di_F / dt = – 1000 A / µs, T_j = 100 °C	t_{rr}	–	130	–	ns
Storage time I_F = 28 A, V_{CC} = 300 V di_F / dt = – 1000 A / µs, T_j = 100 °C	t_s	–	65	–	
Soft factor I_F = 28 A, V_{CC} = 300 V di_F / dt = – 1000 A / µs, T_j = 100 °C	S	–	1	–	–

Characteristics

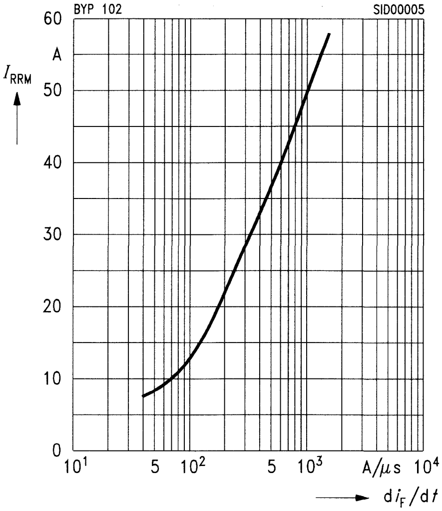
Typ. forward characteristics

$I_F = f(V_F)$
parameter: T_j



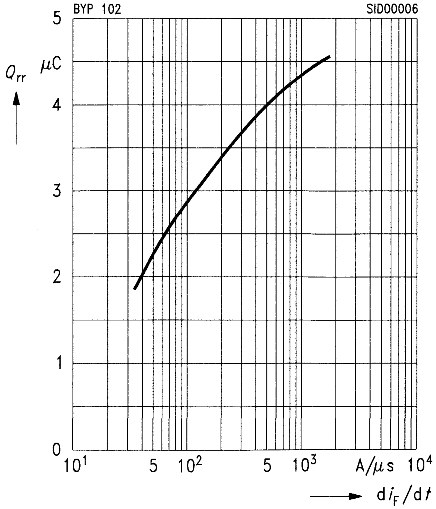
Typ. reverse current

$I_{RRM} = f(di_F / dt)$
parameter: V_{CC} = 300 V, I_F = 30 A, T_j = 100 °C



Typ. reverse recovery charge

$Q_{rr} = f(di_F / dt)$
parameter: V_{CC} = 300 V, I_F = 30 A, T_j = 100 °C

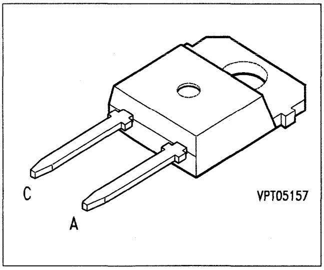


SIEMENS

FRED Diode

BYP 103

- Soft recovery characteristics



Type	V_{RRM}	I_{FRMS}	t_{rr}	**Package** [1]	**Ordering Code**
BYP 103	1000 V	75 A	140 ns	TO-218 AD	C67047-A2066-A2

Maximum Ratings

Parameter	**Symbol**	**Values**	**Unit**
Mean forward current $T_C = 90$ °C, $D = 0.5$	I_{FAV}	**45**	A
RMS forward current	I_{FRMS}	**75**	
Surge forward current $T_j = 100$ °C, 50-Hz sine halfwave, aperiodic	I_{FSM}	**180**	
Repetitive peak forward current $T_j = 100$ °C, $t_p \leq 10$ µs	I_{FRM}	**400**	
i^2t value $T_j = 100$ °C, $t_p = 10$ ms	$\int i^2 dt$	**162**	A^2s
Repetitive peak reverse voltage	V_{RRM}	**1000**	V
Surge peak reverse voltage	V_{RSM}	**1000**	
Power dissipation $T_C = 90$ °C	P_{tot}	**115**	W
Operating and storage temperature range	T_j , T_{stg}	**– 40 ... + 150**	°C

Thermal resistance Chip-case Chip-ambient, without heat sink	 $R_{th\,JC}$ $R_{th\,JA}$	 **≤ 0.5** **≤ 46**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**40/150/56**	

FRED = **F**ast **R**ecovery **E**pitaxial **D**iode

[1] See chapter Package Outlines.

Electrical Characteristics

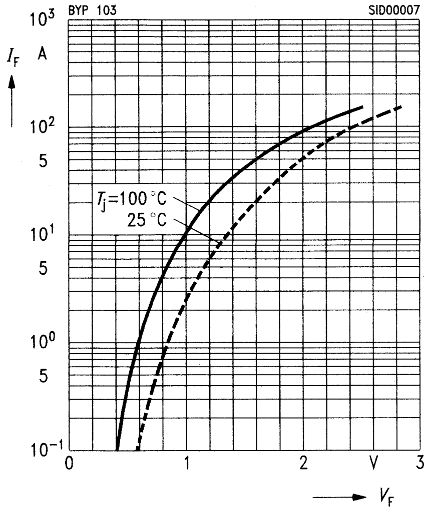
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Forward voltage drop	V_F				V
T_j = 25 °C, I_F = 30 A		–	1.7	–	
I_F = 45 A		–	1.9	2.35	
T_j = 100 °C, I_F = 30 A		–	1.3	–	
I_F = 45 A		–	1.5	–	
Reverse current V_R = 1000 V	I_R				mA
T_j = 25 °C		–	0.01	–	
T_j = 100 °C		–	0.05	–	
T_j = 150 °C		–	0.15	–	
Max. forward characteristic T_j = 100 °C	V_F	1.34 + 0.011 x I_F			V
Forward power dissipation T_j = 100 °C	P_F	1.34 x I_{FAV} + 0.011 x $(I_{FRMS})^2$			W
Dynamic characteristics					
Reverse recovery charge I_F = 45 A, V_{CC} = 300 V di_F / dt = – 1000 A / µs, T_j = 100 °C	Q_{rr}	–	6.0	–	µC
Peak reverse recovery current I_F = 45 A, V_{CC} = 300 V di_F / dt = – 1000 A / µs, T_j = 100 °C	I_{RRM}	–	60	–	A
Reverse recovery time I_F = 45 A, V_{CC} = 300 V di_F / dt = – 1000 A / µs, T_j = 100 °C	t_{rr}	–	140	–	ns
Storage time I_F = 45 A, V_{CC} = 300 V di_F / dt = – 1000 A / µs, T_j = 100 °C	t_s	–	70	–	
Soft factor I_F = 45 A, V_{CC} = 300 V di_F / dt = – 1000 A / µs, T_j = 100 °C	S	–	1	–	–

Characteristics

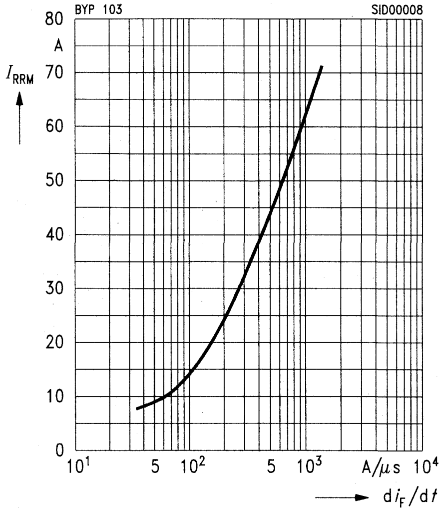
Typ. forward characteristics

$I_F = f(V_F)$
parameter: T_j



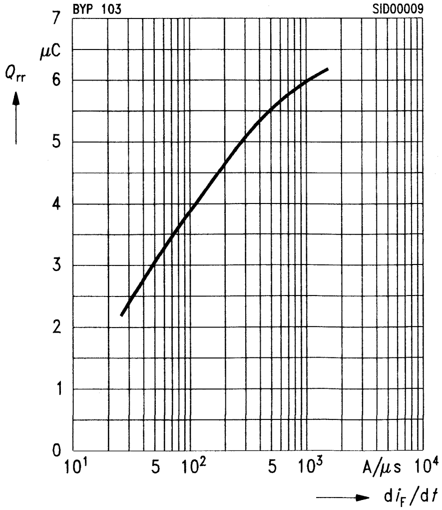
Typ. reverse current

$I_{RRM} = f(\mathrm{d}i_F / \mathrm{d}t)$
parameter: $V_{CC} = 300$ V, $I_F = 45$ A, $T_j = 100$ °C



Typ. reverse recovery charge

$Q_{rr} = f(\mathrm{d}i_F / \mathrm{d}t)$
parameter: $V_{CC} = 300$ V, $I_F = 45$ A, $T_j = 100$ °C



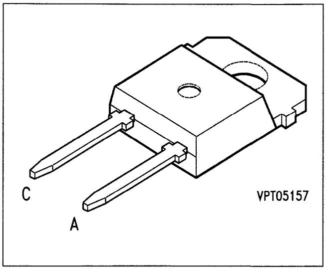
SIEMENS

FRED Diode

BYP 300

Preliminary data

- Soft recovery characteristics



Type	V_{RRM}	I_{FRMS}	t_{rr}	Package 1)	Ordering Code
BYP 300	1200 V	6.5 A	55 ns	TO-218 AD	C67047-A2250-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Mean forward current $T_C = 90\ ^\circ C$, $D = 0.5$	I_{FAV}	**4.0**	A
RMS forward current	I_{FRMS}	**6.5**	
Surge forward current $T_j = 100\ ^\circ C$, 50-Hz sine halfwave, aperiodic	I_{FSM}	**15**	
Repetitive peak forward current $T_j = 100\ ^\circ C$, $t_p \leq 10\ \mu s$	I_{FRM}	**40**	
i^2t value $T_j = 100\ ^\circ C$, $t_p = 10$ ms	$\int i^2 dt$	**1.1**	A^2s
Repetitive peak reverse voltage	V_{RRM}	**1200**	V
Surge peak reverse voltage	V_{RSM}	**1200**	
Power dissipation $T_C = 90\ ^\circ C$	P_{tot}	**15**	W
Operating and storage temperature range	T_j, T_{stg}	**– 40 ... + 150**	°C

Thermal resistance Chip-case Chip-ambient, without heat sink	 $R_{th\ JC}$ $R_{th\ JA}$	 **≤ 3.8** **≤ 46**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**40/150/56**	

FRED = **F**ast **R**ecovery **E**pitaxial **D**iode

1) See chapter Package Outlines.

Electrical Characteristics

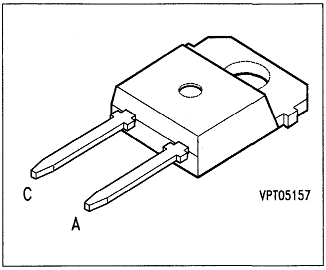
at T_j = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Forward voltage drop I_F = 4.0 A	V_F				V
T_j = 25 °C		–	2.3	3.0	
T_j = 100 °C		–	2.0	–	
Reverse current V_R = 1200 V	I_R				mA
T_j = 25 °C		–	0.01	–	
T_j = 100 °C		–	0.05	–	
T_j = 150 °C		–	0.15	–	
Dynamic characteristics					
Reverse recovery charge I_F = 4.0 A, V_{CC} = 300 V di_F / dt = – 800 A / µs, T_j = 100 °C	Q_{rr}	–	0.8	–	µC
Peak reverse recovery current I_F = 4.0 A, V_{CC} = 300 V di_F / dt = – 800 A / µs, T_j = 100 °C	I_{RRM}	–	22	–	A
Reverse recovery time I_F = 4.0 A, V_{CC} = 300 V di_F / dt = – 800 A / µs, T_j = 100 °C	t_{rr}	–	50	–	ns
Storage time I_F = 4.0 A, V_{CC} = 300 V di_F / dt = – 800 A / µs, T_j = 100 °C	t_s	–	30	–	
Soft factor I_F = 4.0 A, V_{CC} = 300 V di_F / dt = – 800 A / µs, T_j = 100 °C	S	–	0.8	–	–

FRED Diode

BYP 301

- Soft recovery characteristics



Type	V_{RRM}	I_{FRMS}	t_{rr}	Package [1]	Ordering Code
BYP 301	1200 V	20 A	80 ns	TO-218 AD	C67047-A2251-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Mean forward current T_C = 90 °C, D = 0.5	I_{FAV}	**12**	A
RMS forward current	I_{FRMS}	**20**	
Surge forward current T_j = 100 °C, 50-Hz sine halfwave, aperiodic	I_{FSM}	**50**	
Repetitive peak forward current T_j = 100 °C, $t_p \leq 10$ µs	I_{FRM}	**110**	
i^2t value T_j = 100 °C, t_p = 10 ms	$\int i^2 dt$	**13**	A^2s
Repetitive peak reverse voltage	V_{RRM}	**1200**	V
Surge peak reverse voltage	V_{RSM}	**1200**	
Power dissipation T_C = 90 °C	P_{tot}	**40**	W
Operating and storage temperature range	T_j , T_{stg}	**– 40 ... + 150**	°C

Thermal resistance Chip-case Chip-ambient, without heat sink	 $R_{th\ JC}$ $R_{th\ JA}$	 **≤ 1.5** **≤ 46**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**40/150/56**	

FRED = Fast **R**ecovery **E**pitaxial **D**iode

[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 °C, unless otherwise specified.

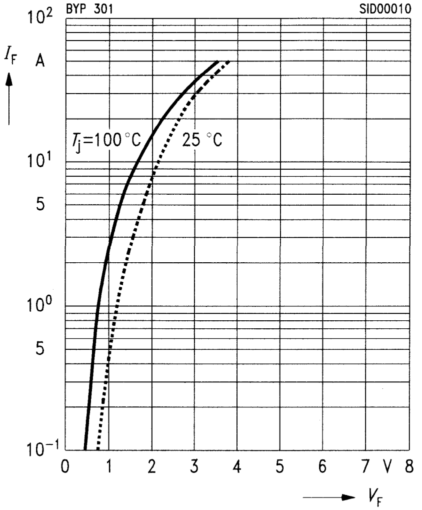
Parameter	**Symbol**	**Values**			**Unit**
		min.	**typ.**	**max.**	
Static characteristics					
Forward voltage drop I_F = 12 A T_j = 25 °C T_j = 100 °C	V_F	 – –	 2.2 1.8	 – 2.75 –	V
Reverse current V_R = 1200 V T_j = 25 °C T_j = 100 °C T_j = 150 °C	I_R	 – – –	 0.01 0.05 0.15	 – – –	mA
Max. forward characteristic T_j = 100 °C	V_F	$1.4 + 0.059 \times I_F$			V
Forward power dissipation T_j = 100 °C	P_F	$1.4 \times I_{FAV} + 0.059 \times (I_{FRMS})^2$			W
Dynamic characteristics					
Reverse recovery charge I_F = 12 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 °C	Q_{rr}	–	2.2	–	µC
Peak reverse recovery current I_F = 12 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 °C	I_{RRM}	–	35	–	A
Reverse recovery time I_F = 12 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 °C	t_{rr}	–	80	–	ns
Storage time I_F = 12 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 °C	t_s	–	45	–	
Soft factor I_F = 12 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 °C	S	–	0.8	–	–

Characteristics

Typ. forward characteristics

$I_F = f(V_F)$

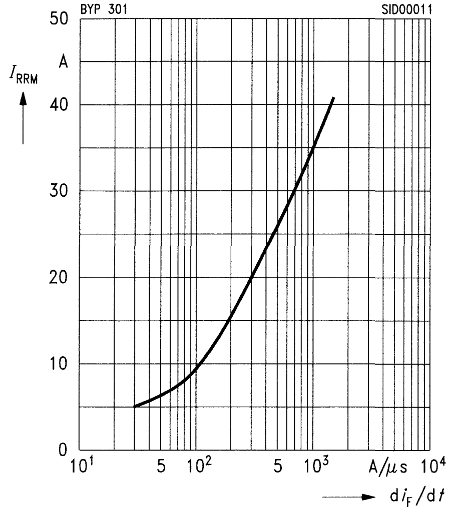
parameter: T_j



Typ. reverse current

$I_{RRM} = f(di_F / dt)$

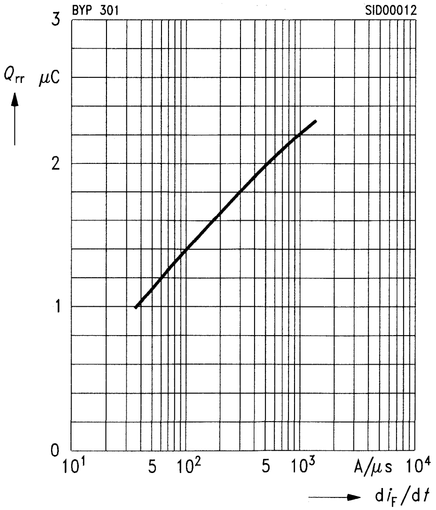
parameter: V_{CC} = 500 V, I_F = 12 A, T_j = 100 °C



Typ. reverse recovery charge

$Q_{rr} = f(di_F / dt)$

parameter: V_{CC} = 500 V, I_F = 12 A, T_j = 100 °C

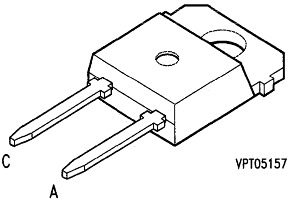


SIEMENS

FRED Diode

BYP 302

- Soft recovery characteristics



Type	V_{RRM}	I_{FRMS}	t_{rr}	Package [1]	Ordering Code
BYP 302	1200 V	40 A	130 ns	TO-218 AD	C67047-A2252-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Mean forward current $T_C = 90$ °C, $D = 0.5$	I_{FAV}	**25**	A
RMS forward current	I_{FRMS}	**40**	
Surge forward current $T_j = 100$ °C, 50-Hz sine halfwave, aperiodic	I_{FSM}	**115**	
Repetitive peak forward current $T_j = 100$ °C, $t_p \leq 10$ µs	I_{FRM}	**260**	
i^2t value $T_j = 100$ °C, $t_p = 10$ ms	$\int i^2 dt$	**66**	A^2s
Repetitive peak reverse voltage	V_{RRM}	**1200**	V
Surge peak reverse voltage	V_{RSM}	**1200**	
Power dissipation $T_C = 90$ °C	P_{tot}	**75**	W
Operating and storage temperature range	T_j, T_{stg}	**– 40 ... + 150**	°C
Thermal resistance			K/W
Chip-case	$R_{th\,JC}$	**≤ 0.8**	
Chip-ambient, without heat sink	$R_{th\,JA}$	**≤ 46**	
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**40/150/56**	

FRED = **F**ast **R**ecovery **E**pitaxial **D**iode

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[1] See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

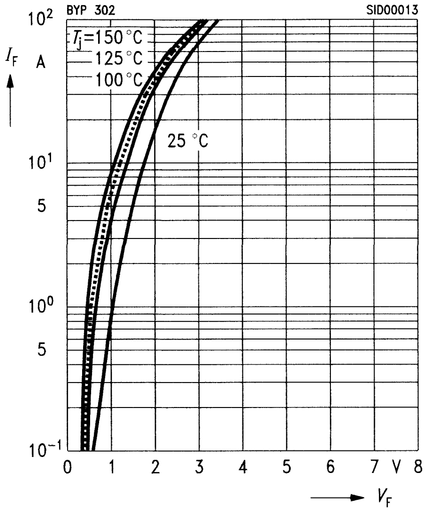
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static characteristics					
Forward voltage drop	V_F				V
T_j = 25 ˚C, I_F = 15 A		–	1.9	–	
I_F = 25 A		–	2.2	2.7	
T_j = 100 ˚C, I_F = 15 A		–	1.5	–	
I_F = 25 A		–	1.8	–	
Reverse current V_R = 1200 V	I_R				mA
T_j = 25 ˚C		–	0.01	–	
T_j = 100 ˚C		–	0.05	–	
T_j = 150 ˚C		–	0.15	–	
Max. forward characteristic T_j = 100 ˚C	V_F	$1.4 + 0.025 \times I_F$			V
Forward power dissipation T_j = 100 ˚C	P_F	$1.4 \times I_{FAV} + 0.025 \times (I_{FRMS})^2$			W
Dynamic characteristics					
Reverse recovery charge I_F = 25 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 ˚C	Q_{rr}	–	4.5	–	µC
Peak reverse recovery current I_F = 25 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 ˚C	I_{RRM}	–	50	–	A
Reverse recovery time I_F = 25 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 ˚C	t_{rr}	–	130	–	ns
Storage time I_F = 25 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 ˚C	t_s	–	65	–	
Soft factor I_F = 25 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 ˚C	S	–	1	–	–

Characteristics

Typ. forward characteristics

$I_F = f(V_F)$

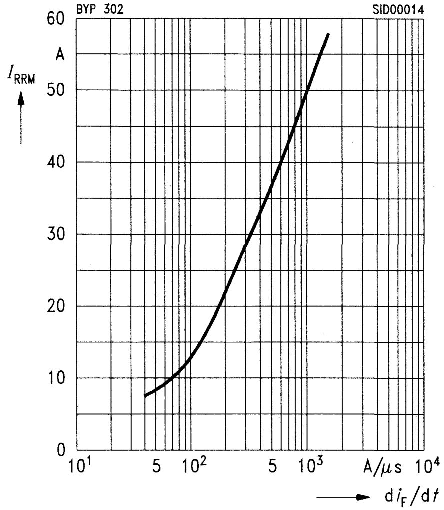
parameter: T_j



Typ. reverse current

$I_{RRM} = f(di_F / dt)$

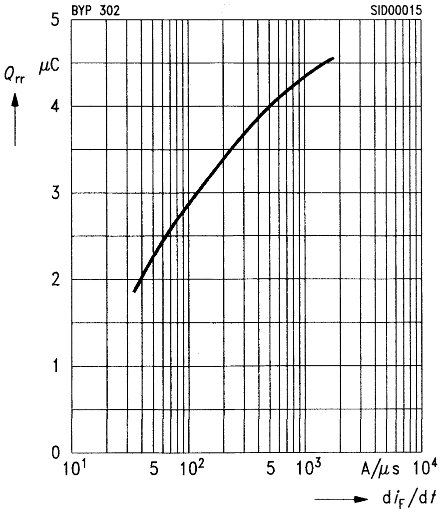
parameter: V_{CC} = 500 V, I_F = 25 A, T_j = 100 °C



Typ. reverse recovery charge

$Q_{rr} = f(di_F / dt)$

parameter: V_{CC} = 500 V, I_F = 25 A, T_j = 100 °C

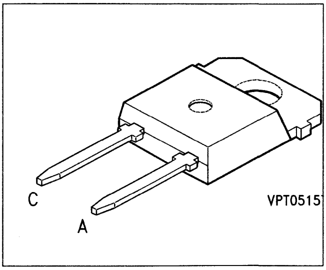


SIEMENS

FRED Diode

BYP 303

- Soft recovery characteristics



Type	V_{RRM}	I_{FRMS}	t_{rr}	Package [1]	Ordering Code
BYP 303	1200 V	65 A	140 ns	TO-218 AD	C67047-A2253-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Mean forward current T_C = 90 ˚C, D = 0.5	I_{FAV}	**40**	A
RMS forward current	I_{FRMS}	**65**	
Surge forward current T_j = 100 ˚C, 50-Hz sine halfwave, aperiodic	I_{FSM}	**170**	
Repetitive peak forward current T_j = 100 ˚C, $t_p \leq 10$ µs	I_{FRM}	**370**	
i^2t value T_j = 100 ˚C, t_p = 10 ms	$\int i^2 dt$	**145**	A²s
Repetitive peak reverse voltage	V_{RRM}	**1200**	V
Surge peak reverse voltage	V_{RSM}	**1200**	
Power dissipation T_C = 90 ˚C	P_{tot}	**120**	W
Operating and storage temperature range	T_j, T_{stg}	**– 40 ... + 150**	˚C

Thermal resistance Chip-case Chip-ambient, without heat sink	 $R_{th\,JC}$ $R_{th\,JA}$	 **≤ 0.5** **≤ 46**	K/W
DIN humidity category, DIN 40 040	–	**E**	–
IEC climatic category, DIN IEC 68-1	–	**40/150/56**	

FRED = **F**ast **R**ecovery **E**pitaxial **D**iode

1) See chapter Package Outlines.

Electrical Characteristics

at T_j = 25 ˚C, unless otherwise specified.

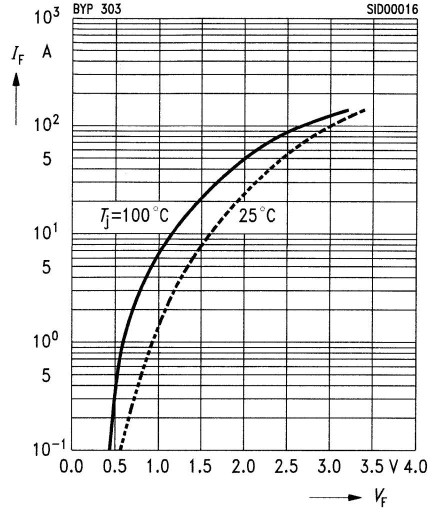
Parameter		Symbol	Values			Unit
			min.	typ.	max.	
Static characteristics						
Forward voltage drop		V_F				V
T_j = 25 ˚C	I_F = 25 A		–	2.0	–	
	I_F = 40 A		–	2.2	2.8	
T_j = 100 ˚C	I_F = 25 A		–	1.6	–	
	I_F = 40 A		–	1.8	–	
Reverse current V_R = 1200 V		I_R				mA
T_j = 25 ˚C			–	0.01	–	
T_j = 100 ˚C			–	0.05	–	
T_j = 150 ˚C			–	0.15	–	
Max. forward characteristic T_j = 100 ˚C		V_F	$1.4 + 0.016 \times I_F$			V
Forward power dissipation T_j = 100 ˚C		P_F	$1.4 \times I_{FAV} + 0.016 \times (I_{FRMS})^2$			W
Dynamic characteristics						
Reverse recovery charge I_F = 40 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 ˚C		Q_{rr}	–	6.0	–	µC
Peak reverse recovery current I_F = 40 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 ˚C		I_{RRM}	–	60	–	A
Reverse recovery time I_F = 40 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 ˚C		t_{rr}	–	140	–	ns
Storage time I_F = 40 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 ˚C		t_s	–	70	–	
Soft factor I_F = 40 A, V_{CC} = 500 V di_F / dt = – 1000 A / µs, T_j = 100 ˚C		S	–	1	–	–

Characteristics

Typ. forward characteristics

$I_F = f(V_F)$

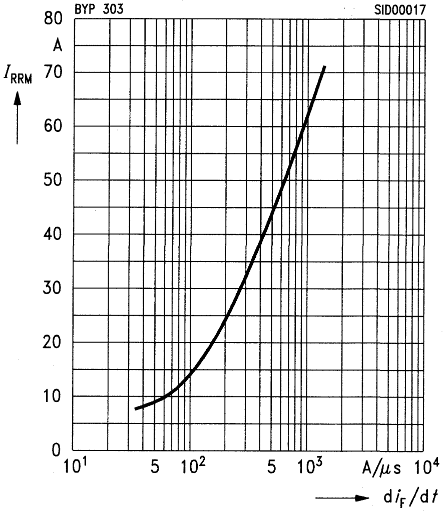
parameter: T_j



Typ. reverse current

$I_{RRM} = f(di_F / dt)$

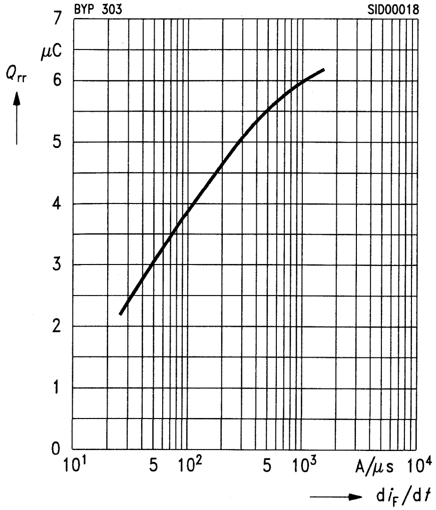
parameter: V_{CC} = 500 V, I_F = 40 A, T_j = 100 °C



Typ. reverse recovery charge

$Q_{rr} = f(di_F / dt)$

parameter: V_{CC} = 500 V, I_F = 40 A, T_j = 100 °C



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